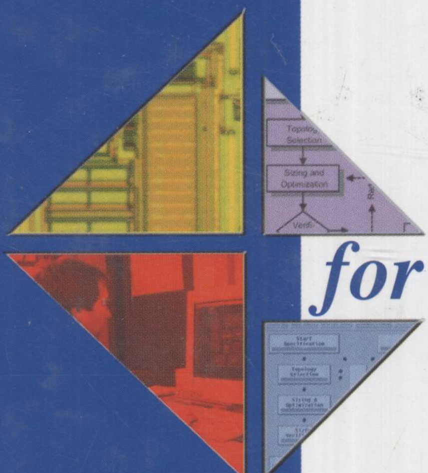
A Computer-Aided Design and Synthesis Environment



for

Analog Integrated Circuits

Geert Van der Plas
Georges Gielen
Willy Sansen

Kluwer Academic Publishers

A COMPUTER-AIDED DESIGN AND SYNTHESIS ENVIRONMENT FOR ANALOG INTEGRATED CIRCUITS

by

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Abstract

Due to the ever decreasing feature size of silicon technology the complexity that can be integrated on a single chip has reached the system level. Soon, as much as 100 million transistors will be integrated on one ICs. We have truly entered the System-on-a-Chip (SoC) era. The existing design methodologies are insufficient for handling these designs, hence a growing design productivity gap develops: design productivity can not keep up with the design needs created by SoCs. Although these SoCs are primarily digital, they interface to the real world, which is analog. Analog building blocks thus become increasingly more important in a world dominated by digital techniques. In this work, research into design automation for analog circuits has been carried out. Two complementary approaches have been investigated.

Firstly, an automatic analog synthesis system, **AMGIE**, has been built. The **AMGIE** system is targeted towards the automatic synthesis from specifications down to layout of moderate-complexity analog circuits (device count lower than 100) that have a high reuse factor. It uses a performance-driven, hierarchical top-down refinement, bottom-up assembly design methodology. Two libraries are required for its operation: (1) a cell (topology) library containing a set of alternative implementation templates and (2) a technology library containing technology parameters. Five design tools automate the different design tasks. Topology selection selects among the topologies in the library the most likely candidate using a sequence of three filters. The sizing and optimization tool determines the sizes and biasing of the selected schematic by using a (modified) equation-based optimization methodology. The derivation of the sizing plan has been automated using a setup environment supported by design tools. The layout tool LAYLA [Lam 99] uses a direct performance-driven macro-cell place & route methodology to generate the layout of the sized schematic. Verification steps after sizing and layout extraction verify the design. Potential design problems are dispatched to the redesign wizard. The redesign wizard provides corrective design procedures to help the designer resolve the detected problem.

A comparison experiment between different sizing approaches indicates that the implemented *modified equation-based optimization* approach is the most appropriate when a high reuse factor is to be expected. A second experiment, the design of an OTA circuit by EE Master students, indicates that the **AMGIE** system creates a new breed of analog designers: system-level designers or less experienced analog designers that are capable of successfully designing moderate-complexity analog circuits in a few hours. The **AMGIE** system can however also handle more complex circuits, as has been demonstrated by the design, fabrication and measurement of an analog signal processing building block: a charge-sensitive amplifier – pulse-shaping amplifier combination.

The design automation approach used in the **AMGIE** approach, however, relies on accumulated design expertise under the form of a cell library which is reused by less experienced designers. Sometimes, the performance specifications of an analog block can not be obtained using existing analog design knowledge and techniques: these are high-challenge designs that require design creativity. In this case full automation is not possible, but the designer can still be supported. The systematic design methodology that is presented in this work is targeted towards the design of these high-performance analog blocks. It leaves room for analog design creativity: coming up with new ideas to solve hard design problems. The methodology steers this creativity to be productive, by linking every design choice that has to be made to the requested specifications. The design productivity is further increased by support through analog CAD tools.

The **Mondriaan** tool presented in this work is such a tool. It automates the layout generation of the highly-regular analog blocks often found in high-speed converter architectures. It automates the back-end process of routing and technology mapping while giving the designer a more abstract view of the layout problem: a floorplan which determines the final position and connectivity of the cell array.

The presented systematic design methodology has then been applied to the design of high-speed current-steering D/A-converters. The first phase in the design flow is the specification phase. Using behavioral modeling and simulation the specification of the D/A-converter functionblock have been derived. The second phase in the design flow is the synthesis of the converter. A top-down refinement, bottom-up, mixed-signal design strategy has been adopted. In the bottom-up path, **Mondriaan** was used to generate the layout of the analog modules, while a standard cell place & route tool was used to create the digital layout. In the last phase of the design a behavioral model is extracted that mimics the actual silicon part. This research has resulted in the first 14-bit accurate current-steering D/A-converter in CMOS technology that does not require trimming or tuning. This performance was obtained by creating the novel Q^2 random walk switching scheme.

Both presented approaches increase analog design productivity. This is demonstrated in the text with design time reports for all the experiments that have been carried out.

List of Abbreviations

1P2M	single poly, double metal
1P3M	single poly, triple metal
2P2M	double poly, double metal
AC	alternating current
A/D-converter	analog to digital converter
ADSL	asymmetric digital subscriber line
AHDL	analog hardware description language
AMS	analog and mixed-signal
A/MS	analog / mixed-signal
ASIC	application-specific integrated circuit
ASSP	application-specific standard parts
AWE	asymptotic waveform evaluation
BC	boundary checking
BiCMOS	bipolar complementary metal-oxide semiconductor
CAD	computer-aided design
CD	compact disc
CMOS	complementary metal-oxide semiconductor
CNN	cellular neural network
CPU	central processing unit
CSA	charge-sensitive amplifier
CSA-PSA	charge-sensitive amplifier – pulse-shaping amplifier
CUD	cell under design
D/A-converter	digital to analog converter
dB	deciBel
DC	direct current *or* design controller
DIFF	differentiator
DLL	delay-locked loop
DNL	differential non-linearity
DRC	design rule check
DRI	data representation interface
DSP	digital signal process(ing/or)
DVD	digital versatile disc
EDA	electronic design automation
EE	electrical engineering
ERC	electrical rule check

ET	extraction tool
GaAs	Gallium-Arsenide
GCM	geometrical calculation model
GP	geometric program(ming)
GUI	graphical user interface
HDL	hardware description language
IC	integrated circuit
INL	integral non-linearity
INT	integrator
IP	intellectual property
ITRS	international technology roadmap for semiconductors
LC-VCO	inductor-capacitor tank VCO
LNA	low-noise amplifier
low-IF	low intermediate-frequency
LSB	least significant bit
LSI	large-scale integration
LT	layout generation tool
LVS	layout versus schematic
MMPRE	mismatch preprocessor
MOS	metal-oxide semiconductor
MSB	most significant bit
NMOS	n-type MOS transistor
OPAMP	operational amplifier
OTA	operational transconductance amplifier
OTA-C	operational transconductance amplifier - capacitor
PC	personal computer
PCA	principal components analysis
PDFE	particle detector front-end
PLL	phase-locked loop
PMOS	p-type MOS transistor
PSA	pulse-shaping amplifier
PSRR	power-supply rejection ratio
PWL	piecewise-linear
Q^2	quad quadrant
RC	resistor-capacitor
RF	radio-frequency
RGB	red green blue
ROM	read-only memory
S/H	sample-and-hold
S&O	sizing and optimization tool
SFDR	spurious-free dynamic range
SIA	semiconductor industry association
SiGe	silicon-germanium
SNDR	signal-to-noise-and-distortion ratio
SNR	signal-to-noise ratio

SoC	system-on-a-chip
SQP	sequential quadratic programming
SVD	singular value decomposition
SWITCAP	switched-capacitor
TS	topology selection
VCO	voltage-controlled oscillator
VFSR	very fast simulated re-annealing
VGA	variable-gain amplifier
VLSI	very large-scale integration
VSI	virtual socket interface
VT	verification tool
xDSL	any type of digital subscriber line
zero-IF	zero intermediate-frequency

List of Symbols

Notation:

∞	infinity
$\emptyset$	the empty set
$\propto$	proportional to
$=$	equal to
$\neq$	not equal to
$\approx$	approximately equal to
$a_0, a_1, \ldots, a_n$	coefficients of polynomial
$i, j, \ldots$	integer counters
$f, g, \ldots$	scalar functions
$x, y, \ldots$	scalar variables
$\mathbf{f}, \mathbf{g}, \ldots$	vector functions
$\mathbf{x}, \mathbf{y}, \ldots$	vector variables
$f_i, g_i, \ldots$	scalar subfunctions of vector function
$x_i, y_i, \ldots$	scalar subvariables of vector variable
α_{ij}	exponent
$E\{x\}$	expected value of x
$\overline{x}$	average value of x

List:

A	context dependent parameter
$\mathbf{A}$	set of design parameters, input specs and technology parameters
A_{glitch}	the amplitude of the glitch

A_{v0}	low-frequency gain
A_{V_T}, A_β	MOS mismatch model parameters [Laksh 86, Pel 89]
β	scaling parameter for scalar cost function
$\beta()$	beta function
BW	bandwidth
C_d	detector capacitance
C_f	(CSA) feedback capacitance
$cgs, cgd, \ldots$	gate source, gate drain, etc. capacitance of transistor
C_{load}	load capacitance
C_{out}	output capacitance
C_p, C_{pk}	statistical indices for design centering
C_{par}	parasitic capacitance
ΔP	performance specification margin or range
DNL	differential non-linearity
$\epsilon^{(i)}$	ith order error profile
E_{glitch}	glitch energy
ENC	equivalent noise charge
ENC_{tot}	total equivalent noise charge
$\Phi(\mathbf{x})$	scalar cost function
f_{in}	input signal frequency
$f_{p\|z}$	frequency of pole or zero
$f_{routing}$	routing overhead factor
f_s	sampling frequency
γ	scaling parameter for scalar cost function
GBW	gainbandwidth
$gm, go, \ldots$	transconductance and output conductance of MOS transistor
$i_n(f)$	noise spectral density
INL	integral non-linearity
IR	input range
I_{gm}	MOS DC current generating transconductance
I_{LSB}	LSB current
I_{tot}	total DC current
I_{out}	full-scale output current
k	Boltzmann's constant (1.38e-23 J/K)
KP	transistor transconductance factor, μC_{ox}
l	loop counter or number of binary bits in a D/A-converter
λ_i	ith eigenvalue
Λ	eigenvalue matrix
L_{m1}	length of transistor $m1$
$level_i$	output value of code level in a D/A-converter
$LMIN, LGRID, LMAX$	length related technology parameters
$logL, logW$	process independent values of length and width of transistors
m	number of unary bits in a D/A-converter
n	PSA order, number of bits
OR	output range

P	performance specification
PM	phase margin
$\psi_{lb,ub}$	topology performance region lower- or upperbound
q	elementary electron charge (1.602e-19 C)
rf	reuse factor
R_f	(CSA) feedback resistance
R_{gnd}	ground line resistance
R_{load}	load resistance
ro	output resistance of MOS transistor
R_{output}	output resistance of a D/A-converter
R_{par}	parasitic resistance
rv	topology ranking value
S	subblock specification set (estimators)
$\sigma(x)$	standard deviation of a quantity x
Σ	singular value decomposition matrix
S_b^a	sensitivity of a to variable b
SNR	signal to noise rate
SR	slew rate
S_{V_T}, S_β	MOS mismatch model parameters [Laksh 86, Pel 89]
T	Temperature
τ	time constant
Θ	technology parameter set
τ_p	peaking time constant
τ_{pz}	pole zero time constant
τ_r	rise time constant
t_{glitch}	glitch duration time
$u()$	step function
V_{dd}, V_{ss}	power supply voltages
V_{gs}, V_{ds}, V_{bs}, ...	device terminal voltage differences
V_{gst}	transistor overdrive voltage, $V_{gs} - V_T$
V_{off}	offset voltage due to random and systematic effects
V_{out}	full-scale output voltage
V_T	threshold voltage
$\sharp\, wires$	number of wires
w_j	weight of constraint in cost function
W_{m1}	width of transistor $m1$
$WMIN$, $WGRID$, $WMAX$	width related technology parameters

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