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TABLE OF CONTENTS

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A 20 KW ULTRASONIC MOSFET PWM INVERTER OPERATED FROM A 550 VOLT DC LINK

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ABSTRACT

Using a novel power circuit arrangement, a 20 kW MOSFET PWM inverter is proposed for noiseless power conversion in ac drive applications. The inverter is directly fed from a three-phase supply and operates at high dc link voltage. This eliminates a voltage stepdown transformer. Instead, series connected power MOSFETs of medium voltage rating are used to handle the high dc-link voltage. A symmetrical voltage distribution across the power semiconductors is forced from the dc link potentials without the use of snubbers. The circuit inherently decouples the internal body-drain diodes of the MOSFETs without employing additional components.

INTRODUCTION

Power MOSFET transistors are majority carrier devices which do not exhibit the problem of stored charges at turn-off. This results in very low switching losses and permits the application of power MOSFETs in PWM inverters at switching frequencies in the ultrasonic range. The specific advantages of such drive systems are very low harmonic distortion of the motor currents and noiseless operation of the power converter.

PWM inverter fed drive systems using MOSFETs are presently manufactured in a limited power range up to only a few kilowatts /1/. Such drive systems are usually supplied by the single phase 230 V mains through a bridge rectifier and hence operate at a dc link voltage of about 325 V. This matches the blocking capability of high-current power MOSFET devices, the maximum blocking voltage of which is practically limited to about 500 V. This value reflects the dependency of the on-resistance of a MOSFET on its drain-source voltage rating according to the relationship $R_{DS\ ON} \approx U_{DS}$ exp (2.5 ... 2.7) /2/.

In view of the advantages of ultrasonic PWM inverters, it appears desirable to expand the range of application to higher power levels. This necessitates to supply the dc link circuit of the inverter from the three-phase mains, since the power capabi-

lity of a single-phase supply is usually limited to a few kilowatts. It is an advantage of a three-phase supply that a six-pulse diode bridge rectifier can be used to feed the dc link circuit. A six-pulse bridge produces less voltage ripple at the rectifier output, while the ripple frequency increases from 100 to 300 Hz. Hence, the filter components in the dc link can be considerably reduced in size.

The concept of operating a MOSFET inverter from a three-phase supply normally requires the installation of a three-phase input transformer in order to reduce the resulting dc link voltage to a value which can be handled by the power MOSFETs. A transformer is an expensive and bulky component which does not match the lightweight construction of a MOSFET inverter. Although having the advantage of ultrasonic switching frequency, it is obvious that such drive concept cannot compete with the standard bipolar transistor PWM inverters with respect to weight, volume, and cost.

HIGH-VOLTAGE MOSFET INVERTER

The above problem is solved using a classical 550 V dc link circuit, while composing each power switch of the inverter by two high-current, medium voltage power MOSFETs connected in series. The link circuit is directly supplied from the 380 V three-phase mains through a diode bridge rectifier.

Fig. 1 shows the circuit diagram of one inverter leg. Two 400 V MOSFET elements are used in a series connection to represent one power switch. During the blocking state, the voltages across the two MOSFETs are controlled from the center tap of the dc link capacitor through one of the clamping diodes D3 and D4. This ensures a symmetric distribution of

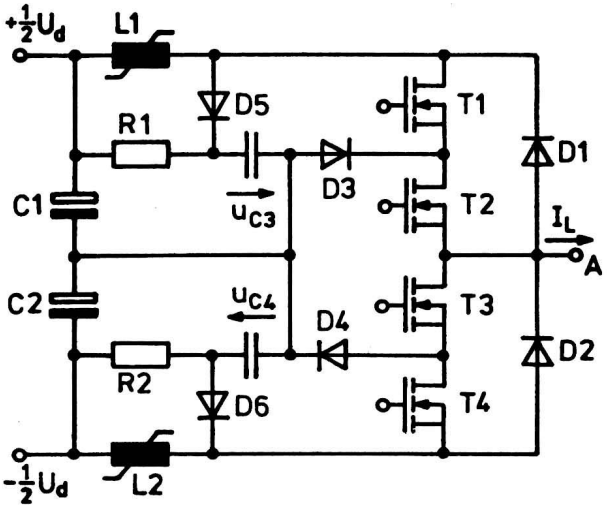


Fig. 1: Circuit diagram of one leg of a high-voltage MOSFET inverter

the blocking voltages across each of the series connected MOSFET transistors during switching. The clamping diodes are chosen to replace the parallel snubber capacitors that are conventionally employed in order to balance the voltage distribution across a pair of series connected power switches. Snubber capacitors would have to be periodically discharged and their energy dissipated in resistors when the switches are turned on again. In contrast, the proposed arrangement is much more efficient, since there are no discharge resistors. The clamping diodes D3 or D4 are turned off at zero voltage which nearly eliminates their switching losses.

Each pair of series connected MOSFETs is bridged by a common flyback diode. As a consequence, the internal body-drain diodes of the two MOSFETs will never come to a state of conduction since the forward voltage drop of one flyback diode is always less than the sum of the forward voltages of the two internal MOSFET diodes. This is advantageous since it permits the use of external fast-recovery diodes in the flyback path without any additio-

nal measures.

Such measures are usually employed with the aim of decoupling the internal diodes and to prevent an unintended turn-on of the parasitic npn transistor of the MOSFET /3/. The decoupling is normally achieved by providing additional diodes arranged either in series with each MOSFET /1,4/ or between each MOSFET and the flyback diode of the opposite bridge arm on one side and the ac output connection of the bridge leg on the other /4/. In a different approach, the problem has been overcome by providing an additional intermediate commutation loop and using the turn-off delay of an auxiliary diode to prevent the turn-on of the parasitic npn transistor /6/.

The solution proposed here offers the advantage that external flyback diodes of the fast recovery type can be used without requiring additional components for the decoupling of the internal body-drain diodes. The philosophy avoids high dv/dt slew rates of the drain-source voltage of the paralleled MOSFETs at the end of the conduction period of the internal diodes which generally leads to the destruction of the device /7/.

In order to reduce the switching losses of the flyback diodes, saturable inductors are located in the positive and the negative connection to the dc link. These elements are designed for minimum residual inductance at saturated core. This way the magnetic energy stored at full current is kept low. The design avoids the unnecessary transfer of energy to the inductor which results in a reduction of energy recovery losses.

As the transition times during turn-on and turn-off of the MOSFET devices are very short, the currents are rapidly transferred between the various loops of the inverter circuit during

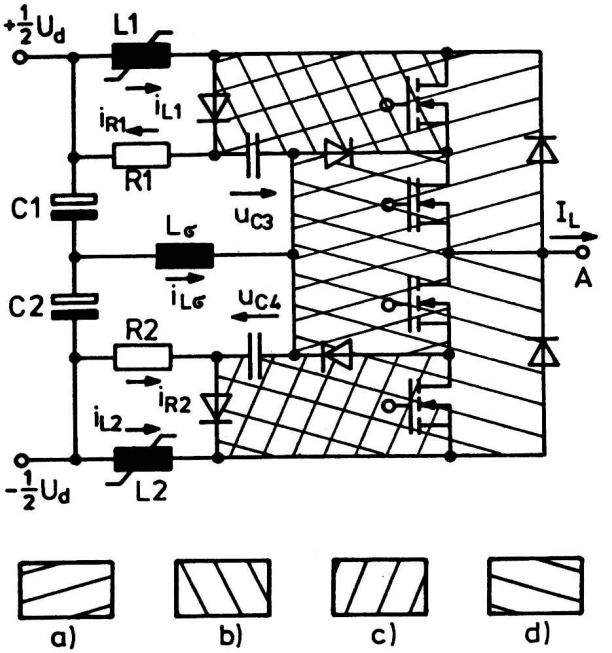


Fig. 2: The four critical commutation loops of the inverter leg marked by different hatching patterns a) ... d)

commutations. This gives rise to induced voltages in the stray inductances of the wiring. Under normal conditions, these voltages can assume the order of several hundred volts. The induced voltages add to the voltage stress of a device at turn-off and hence must be reduced to a minimum. This is achieved by incorporating all critical electric connections of the power circuit in a single multilayer conductor sheet, in which the individual conductor layers are separated from each other by thin films of insulating material. The magnetic field which is produced by the currents in the conductors is basically concentrated to the small volume between the respective conductors and the resulting flux linkage is very low.

The critical part of an inverter leg circuit which requires a low leakage inductance is indicated by the hatched areas of **Fig. 2**. Different hatching patterns are used to visualize

the individual commutation loops. The critical commutation circuits include the MOSFET switches, the flyback diodes, and the two clamping circuits D5 - C1 - D3 and D4 - C2 - D6. These components are closely mounted to the multilayer conductor sheet.

CIRCUIT ANALYSIS

The stray inductance of the multilayer structure can be neglected in the analysis of the circuit of Fig. 2. However, the stray inductances of the electrical connections between the power circuit and the storage capacitors of the dc link must be taken into account. They are represented as part of the inductors L1 and L2 as well as an additional inductance L_σ located between the center tap of the link capacitor and the clamping diodes D3 and D4.

The waveforms of the commutations during a turn-off sequence of the switches T1 and T2 in Fig. 1 are shown in **Fig. 3**. Before the commutation, the load current flows through L1 - T1 - T2. The voltage clamping capacitors C3 and C4 are held charged at a level of Ud/2 by the resistors R1 and R2, respectively.

At $t = t_1$, MOSFET T1 is turned off. This causes the load current to commutate rapidly from T1 to D5 - C3 - D3 - T2. An oscillation is started between the residual inductance of the saturated core L1, connected in series with the leakage inductance L_σ, and the clamping capacitor C3. The large storage capacitor C1 forms part of this resonant loop without really affecting the oscillation, while R1 performs as a damping resi-

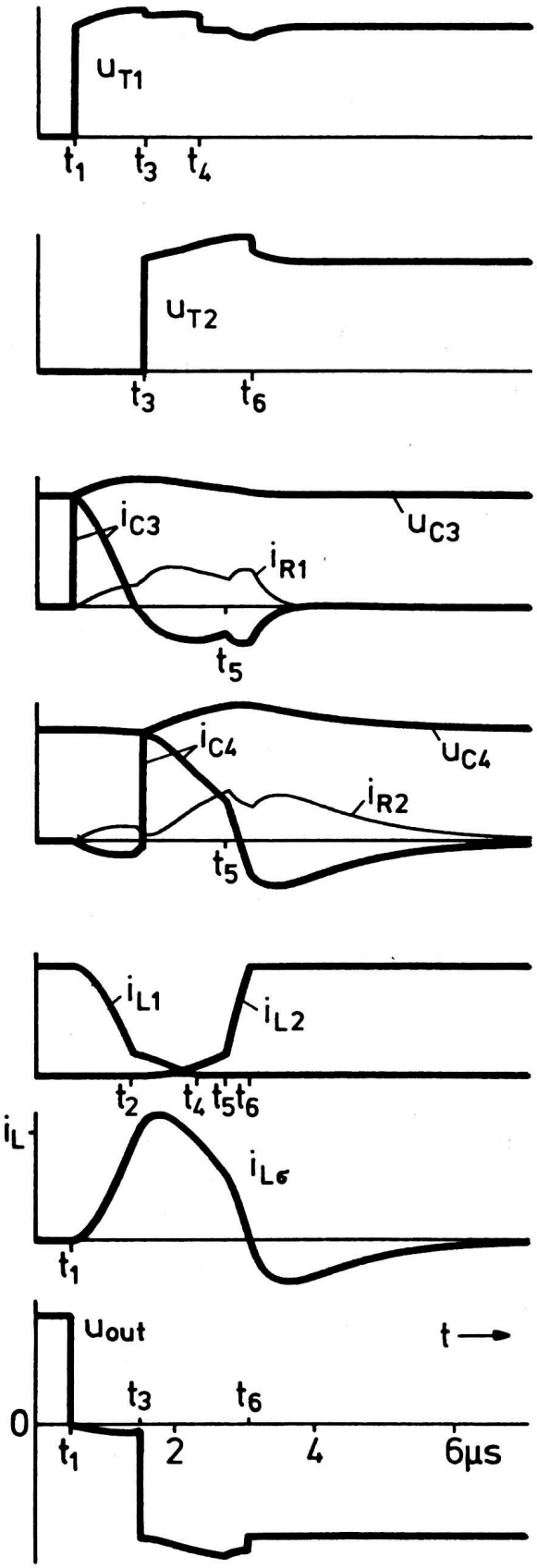
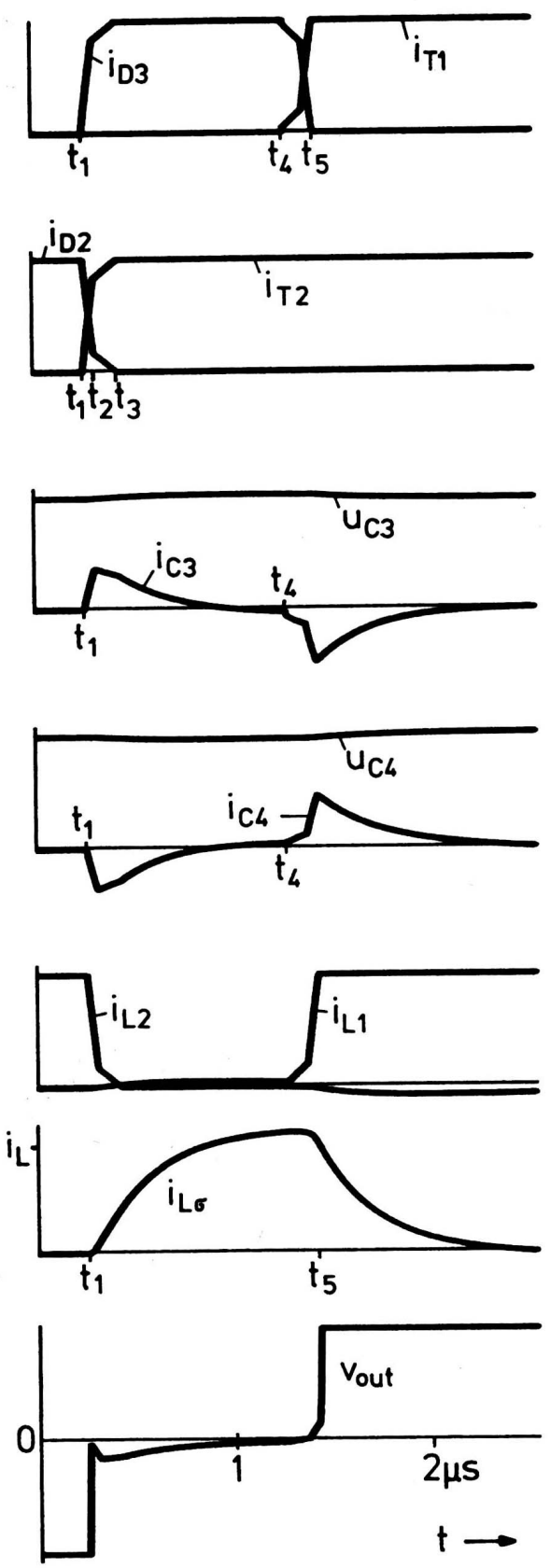


Fig. 3 (right): Computed waveforms of the commutation of a positive load current from T1 to D2



stor. During the oscillation, a major portion of the current through L1 commutates to L_σ, while the clamping capacitor voltage u_{c3} increases. Owing to the voltage across L_σ, the clamping capacitor C4 is getting slightly discharged through C2 and R2.

After a short delay time of about 1 µs, the second MOSFET T2 is turned off at t_3. The low stray inductance of the multilayer wiring permits a fast commutation between T2 and D2. This commutation being performed, part of the load current through C4 - D6 - D2 flows through L1 - D5 - C3, and another part through L_σ, while a gradually increasing portion is supplied through L2. The voltage u_{c4} starts rising over its initial value Ud/2 and increases exponentially.

At $t = t_2$, the current through L1 has reduced to the saturation level of the core. From here onwards, both inductors L1 and L2 are desaturated and hence their currents change only slowly: While i_{L1} decreases, the current through L2 increases. The current through L_σ also increases, mainly because of the changing currents through R1 and R2.

The inductor L2 desaturates at $t = t_4$ and its low residual inductance permits a steep rise of its current. When the load current level is reached at $t = t_5$, the diode D6 starts blocking. During the remaining time $t > t_5$, the decaying discharge current of C4 circulates in the loop C4 - L_σ - C2- - R2.

The waveforms of the reverse commutation are shown in **Fig. 4**. The MOSFET T2 is turned on at $t = t_1$. The load

Fig. 4 (left): Computed waveforms of the commutation of a positive load current from D2 to T1

current then commutates from L2 and the flyback diode D2 to the electrically symmetric parallel branches R2 - C4 and C2 - C1 - R1 - C3, from where it continues to flow through D3 - T2, while the current through L_σ rises a little later in the fashion of a second order response. L2 desaturates at $t = t_2$, reducing the di/dt of the current through the flyback diode D2 for improved turn-off. With the low di/dt of the commutating current prevailing at $t > t_2$, the parallel currents through R1 - C3 and R2 - C4 decrease, while the current through L_σ increases.

The MOSFET T1 receives a gate signal at $t = t_4$. During the commutation overlap between D3 and T1, the commutation current passes mainly through C3 - R1 and C4 - R2 - C2 - C1. This commutation terminates at $t = t_5$. In the remaining time $t > t_5$, C3 is discharged and C4 is charged, both to the level of Ud/2, the sum of their currents passing through the leakage inductance L_σ.

Note that the curves in Fig. 3 and Fig. 4 are shown in different time scales.

THE GATE DRIVE CIRCUIT

The isolated gate of a MOSFET transistor does not draw current during the on-state. Even so, the gate-source capacitance requires to be periodically charged and discharged at the rate of the inverter switching frequency. The internal impedance of the gate drive circuit must be low so as to ensure fast charging and discharging at the instants of switching. Furthermore, the circuit must be able to maintain the off-potential at the gate even in the presence of displacement currents flowing into the gate through the drain-gate capacitance, which occur at rising drain-source potential, so as to prevent the device from turning on unintentionally. Finally, the MOSFET must be protected against short circuits and overload.

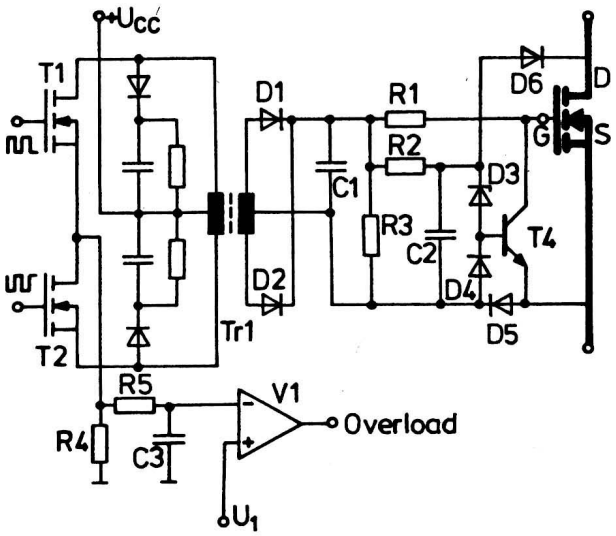


Fig. 5: The gate drive circuit

The gate drive circuit shown in **Fig. 5** was designed to meet the above requirements. It uses a 1 MHz push-pull converter to transfer the turn-on energy to the potential of the MOSFET switch /9/.

The push-pull converter is operated during the on-state interval of the MOSFET. Its output voltage is rectified and filtered by a very small capacitor C1. At the beginning of the on-state interval, the gate source capacitance is getting charged through R1, while the capacitor C2 charges through R2. The time constant $R2 \cdot C2$ is larger than the time constant $R1 \cdot C_{GS}$ of the gate circuit. Hence, the MOSFET is turned on before the voltage u_{c2} has built up to the level necessary to turn on T4 through the zener diode D3. Once turned on, the MOSFET discharges the capacitor C2 through D6.

The transistor T4 forms part of a protection circuit against overload and unintended turn-on. At overload

and short-circuit conditions, the MOSFET limits its drain current by increasing the drain-source voltage. The current through R2 is then no longer by-passed through D6 which permits the capacitor voltage u_{C2} to rise. The transistor T4 is turned on. It discharges the gate-source capacitance and turns the MOSFET off. The maximum drain current capable of triggering this protection circuit depends on the junction temperature of the MOSFET in such a way that the thermal storage capacity of the device can be utilized to extend the overload interval.

An overload or short-circuit condition is detected on the primary side of the transformer Tr1. Since the secondary is then shorted by T4 and R1, the primary current increases, giving rise to a higher voltage across R4. The comparator V1 outputs an overload signal with respect to the ground potential of the electronic control circuit. The overload signal is delayed by R5 - C3 in order to suppress the effect the initial charging current of the gate-source capacitance at normal turn-on.

An unintended turn-on of the MOSFET may occur at a positive dv/dt of the drain-source voltage, which produces a displacement current through the internal capacitances between the drain-gate and the gate-source layers. The gate potential rises, driving a current through R1 - R3 - D4 - T4. The transistor T4 is turned on and discharges the input capacitance of the MOSFET. However, when the gate-source capacitance is charged through the push-pull converter, the charging current passes through R1 - C_{GS} - D5 and the transistor T4 is blocked by the voltage drop across D5.

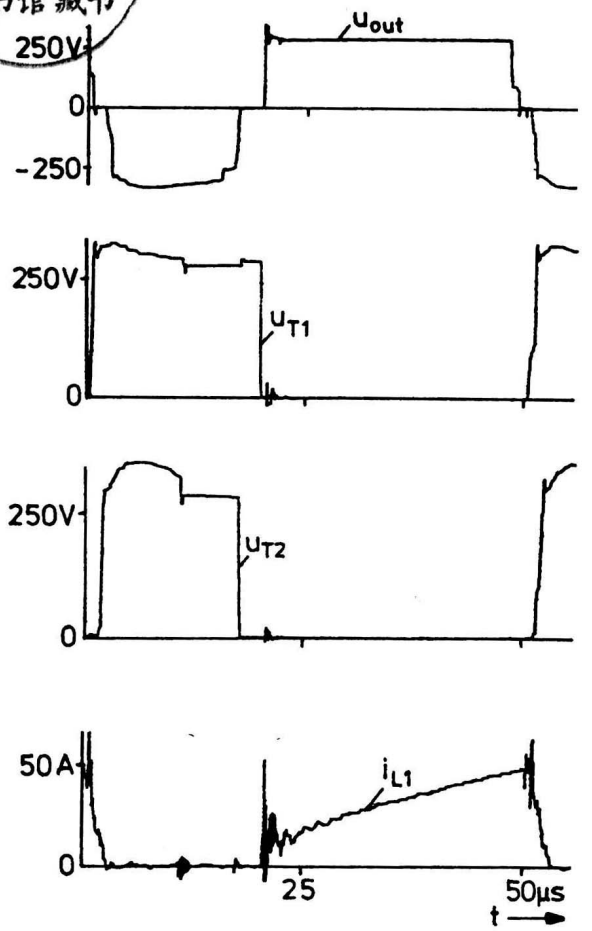


Fig. 6: Waveforms of a switching cycle at 20kHz
a) output voltage
b) forward voltage of T1
c) forward voltage of T2
d) inductor current i_{L1}

EXPERIMENTAL RESULTS

The operation of the MOSFET inverter bridge leg was tested at 550 V dc link voltage, 20 kHz switching frequency and 50 A load current. The waveforms of a full switching cycle are shown in **Fig. 6**. This oscillogram starts when both MOSFETs T1 and T2 are conducting. The output voltage u_{out} = 275 V.

A reversal of the output voltage takes place when first T1, and after a

short time delay, T2 are turned off. The forward voltages of both MOSFET transistors are limited by the respective clamping capacitors C3 and C4. Owing to the extreme low leakage inductance of the multilayer conductor, the turn-off overvoltages amount to less than 50 V. The corresponding spikes are lower than the clamping overvoltages.

For the reverse commutation, T2 and T1 are turned on in a proper time sequence. The reverse recovery peak current of the diode D5 is visible in the waveform of i_{L1}. Its high magitude of 40 A underlines the necessity of using saturable cores in high-current MOSFET inverters in order to assist the turn-off process of the diodes.

During operation at the maximum load current of 35 A rms the losses in the resistors R1 and R2 have been found as 32 W/phase when the time delay between the switchings of the MOSFETs T1 and T2 is 1 µs. The losses reduce to 27 W/phase with a time delay of 0.5 µs.

SUMMARY

The paper describes a high-power MOSFET PWM inverter which is operated from a 550 V dc link circuit with a direct connection to the three phase mains through a diode bridge rectifier. Each inverter switch is composed of two medium blocking voltage MOSFETs in series connection, bridged by a common flyback diode. During the blocking state, the voltage distribution between the two MOSFETs is controlled from a center tap of the dc link capacitor. This avoids dynamic voltage unsymmetries even in the complete absence of snubber circuits. The internal parasitic body-drain diodes of the two MOSFETs are not activated owing to the low forward voltage drop of the parallel flyback diode. This way the usual decoupling diodes are eliminated which leads to reduced cost and improved efficiency. Saturable core inductors serve to reduce the switching losses of the flyback diodes. The power circuit is wired employing a multilayer conductor arrangement which minimizes the switching overvoltages.

An analysis of the operation and the experimental results obtained from a 50 A PWM inverter bridge operated from 550 V dc link voltage are presented.

ACKNOWLEDGEMENT

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RECENT DEVELOPMENTS IN PWM SWITCHING STRATEGIES FOR MICROPROCESSOR-CONTROLLED INVERTER DRIVES

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Abstract

This paper surveys recent research into the development of new optimal PWM techniques for both voltage source inverter (VSI) and current source inverter (CSI) drives.

It is shown how optimised PWM for VSI drives can be generated "on-line" in "real-time" using modified regular sampling techniques, without resorting to the laborious, time-consuming, main-frame computer minimisation techniques normally associated with optimised PWM techniques. Using these optimal regular-sampling PWM techniques it is possible to produce a PWM drive performance which closely approximates the optimised PWM performance up to quasi-square wave operation.

In addition, a survey of a number of new high pulse number harmonic-elimination, harmonic minimisation, and optimal PWM techniques for CSI drives will be presented which minimise rotor speed ripple and positional error, and provide smoother rotor motion at low speeds.

Introduction

Historically, the most popular and widely used PWM generation technique in the early 1960's involved the direct comparison of a sinusoidal "modulating" signal with a triangular "carrier" signal to produce the PWM switching edges [1-4]. This technique was widely used because of its simplicity and ease of implementation using analogue techniques. The essential feature of this seemingly relatively simple "modulation process" is the continuous "real-time" comparison of the sinusoidal modulating and triangular carrier signals. The instantaneous intersection of these two signals is used to determine the PWM switching instants by a process of "natural" selection or "sampling", hence the terminology "natural-sampled" PWM [3,4].

It has been shown earlier [3-5] that as a result of the natural-sampling process, which is non-linear, the PWM pulse-widths are defined by a transcendental equation, which can only be solved using Bessel function series or numerical techniques. This can create difficulties both in computer-aided design (CAD) analysis [5-7] and also digital or microprocessor implementation [8,9].

These difficulties and disadvantages of natural-sampled PWM result directly from the analogue nature of the non-linear sampling modulation process, making it inappropriate for efficient discrete digital hardware or microprocessor software implementation [8,9].

These difficulties can be completely eliminated using "regular-sampled" PWM techniques.

The essential features and detailed characteristics of regular-sampled PWM techniques are surveyed in the next section and used as a basis for developing "Optimal" regular-sampled PWM techniques.

As will be demonstrated, the most significant advantage of regular-sampled PWM is the inherent linear sampling process which allows samples of the modulating wave to be taken at regularly spaced intervals [4,5].

This results in the PWM pulse positions being regularly spaced and the pulse widths precisely defined, such that it is possible to derive a simple trigonometric equation to calculate the PWM pulsewidths [4,5].

This is in complete contrast to natural-sampled PWM where both the pulse positions and pulse-widths can only be defined using a nonlinear transcendental equation [3-5].

Thus regular-sampled PWM overcomes all the disadvantages of natural-sampled PWM, and can be used to generate PWM "on-line" in "real-time" using an extremely efficient microprocessor-based software algorithm [8,9].

Both natural-sampled PWM [1-4] and regular-sampled PWM techniques [4-9] are based on well-defined modulation processes and as a result can be directly implemented using either analogue, digital or microprocessor techniques.

More recently harmonic elimination [10,11] and the so-called optimised [12] PWM techniques have been developed which do not rely upon defining a recognisable modulation process. As a result of the absence of a definable modulation process these optimised PWM strategies can only be implemented using numerical characteristics, which requires a memory-based look-up table (LUT) implementation, typically requiring a microprocessor.

Whilst it is generally recognised that these optimised PWM techniques [10-12] have distinct advantages, allowing the PWM harmonic spectrum to be "tailored" to minimise the harmonic distortion resulting in much improved performance specifications, they are significantly more complex to generate as a result of the off-line main-frame numerical minimisation search techniques involved [10-12].

This complexity has in the past prevented the use of these optimised PWM techniques in many practical drive applications. To promote wider application of these optimised PWM techniques it is necessary to develop an "optimised modulation process" which will allow optimised PWM to be generated on-line, in real-time, without the need to resort to the usual time-consuming, computationally onerous, off-line mainframe numerical optimsation techniques. The possibility of achieving this goal, using new optimal regular-sampled PWM techniques, has recently been demonstrated [13,14].

This paper reviews recent research into developments of optimal PWM switching strategies for both voltage source (VSI) and current source inverter (CSI) drives.

It is shown how, using well established regular-sampling techniques with suitable modifications, it is possible to produce a VSI drive performance which closely approximates the optimised PWM performance over a wide voltage/frequency range up to, and including, quasi-square wave operation.

In addition, it is shown that as a result of the well defined and relatively simple modulation process involved in the regular-sampled PWM, the potential for "on-line", "real-time" microprocessor-based PWM generation exists.

Finally, a number of new high pulse number harmonic-elimination, harmonic minimisation, and optimal PWM techniques for CSI drives will be reviewed which minimise rotor speed ripple and positional error, and provide smoother rotor motion at low speeds. These new PWM techniques have been applied to the conventional, series-connected and parallel-connected CSI induction motor drive.

Brief Survey of Regular-Sampled PWM Techniques

Regular-sampled PWM is based on a well defined modulation process. A typical practical implementation illustrating the general features of double-edge two-level "asymmetric" regular-sampled PWM [4,5] is shown in Figure 1.

As illustrated in Figure 1, a triangular carrier (or sampling) wave 'b' is used to sample the sinusoidal modulating wave 'a' twice every carrier cycle at regularly spaced intervals, corresponding to the positive and and negative peaks of the triangular wave, to produce the sampled-hold or amplitude-modulated wave 'c'. Comparison of the sampled modulating wave 'c' with the carrier wave 'b' defines the points of intersection used to determine the switching instants of the width-modulated pulses 'd'. As a result of this modulation process the "sampled-hold" modulating signal has a finite number of constant levels (samples) which remain constant during the intersections (comparisons) of the modulating and carrier signals defining the PWM switching instants. As a result the "real-time" comparisons between modulating and carrier signals, which caused the difficulties in natural-sampling have been eliminated.

The above description of regular-sampling has been given in terms of an analogue implementation simply to provide a geometric interpretation of the process, and also to provide a basis for direct comparison with the natural-sampling process.

An alternative and more informative interpretation, particularly for microprocessor implementation, is to consider regular-sampling as a digital process of sampling a sinusoidal modulating wave 'a', at regularly spaced intervals, to produce sinusoidally weighted digital samples of the modulating wave, represented by 'd' in Figure 1. These digital samples are subsequently stored in microprocessor memory (ROM) and used to generate regular-sampled PWM on-line using either a software algorithm or a hardware comparator