Analog Circuit Design

Scalable Analog Circuit Design, High-Speed D/A Converters, RF Power Amplifiers

Edited by
Johan H. Huijsing
Michiel Steyaert
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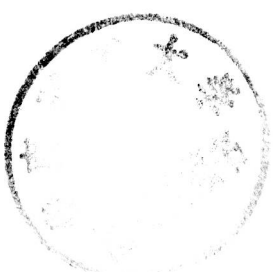

KLUWER ACADEMIC PUBLISHERS
BOSTON / DORDRECHT / LONDON

A C.I.P. Catalogue record for this book is available from the Library of Congress.

ISBN 0-7923-7621-8

Published by Kluwer Academic Publishers,
P.O. Box 17, 3300 AA Dordrecht, The Netherlands.

Sold and distributed in North, Central and South America
by Kluwer Academic Publishers,
101 Philip Drive, Norwell, MA 02061, U.S.A.

In all other countries, sold and distributed
by Kluwer Academic Publishers,
P.O. Box 322, 3300 AH Dordrecht, The Netherlands.

Printed on acid-free paper

Printed in the Netherlands.

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Preface

This book contains the revised contributions of the 18 tutorial speakers at the tenth AACD 2001 in Noordwijk, the Netherlands, April 24-26.

The conference was organized by Marcel Pelgrom, Philips Research Eindhoven, and Ed van Tuijl, Philips Research Eindhoven and Twente University, Enschede, the Netherlands.

The program committee consisted of:

Johan Huijsing, Delft University of Technology
Arthur van Roermund, Eindhoven University of Technology
Michiel Steyaert, Catholic University of Leuven

The program was concentrated around three main topics in analog circuit design. Each of these topics has been covered by six papers. The three main topics are:

Scalable Analog Circuit Design
High-Speed D/A Converters
RF Power Amplifiers

Other topics covered before in this series:

2000 High-Speed Analog-to-Digital Converters
Mixed Signal Design
PLL's and Synthesizers

1999 XDSL and other Communication Systems
RF MOST Models
Integrated Filters and Oscillators

1998 1-Volt- Electronics
Mixed-Mode Systems
Low-Noise and RF Power Amplifiers for Telecommunication

1997 RF A-D Converters
Sensor and Actuator Interfaces
Low-Noise Oscillators, PLL's and Synthesizers

1996 RF CMOS Circuit Design
Bandpass Sigma Delta and other Converters
Translinear Circuits

1995 Low-Noise, Low-Power, Low-Voltage
Mixed Mode with CAD Trials
Voltage, Current and Time References

1994 Low-Power Low Voltage
Integrated Filters
Smart power

1993 Mixed-Mode A/D Design
Sensor Interfaces
Communications Circuits

1992 OpAmps
ADC's
Analog CAD

We hope to serve the analog design community with these series of books and plan to continue this series in the future.

Johan H. Huijsing

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Part I: Scalable Analog Circuit Design

Industry has a need to transfer circuit designs from older integrated-circuit processes into newer processes, which have lower device dimensions. This may be relatively simple for digital circuits. But, for analog circuits this is not straight forward at all because the requirements for noise, offset and dynamic range may resist sealing to smaller dimensions. Therefore, redesigns of analog circuits take a lot of effort. The purpose of these first six papers in this book is to help designers with designs, that can be transferred to future processes with smaller dimensions, or to guide in the process of transferring already existing circuit designs.

In the first four papers the design for scalability is treated in four special areas:

A first paper by Maarten Vertregt of Philips Research, Eindhoven, the Netherlands, presents basic issues of scalable high-speed analog circuit design.

A second paper by Bob Brewer, Analog Devices, Newbury, UK, evaluates scalable high-resolution mixed-mode circuit design.

A third paper by Dominico Rossi, ST Microelectronics, Italy, discusses solutions for scalable "high-voltage" integrated circuit design for XDSL.

The fourth paper by Klaas Bult, Broadcom, Bunnik, the Netherlands, describes scalability issues of wire-line front-ends.

The last two papers are of general help on scaling:

The fifth paper by Jörg Hauptmann, Infineon Technologies, Villach, Austria, discusses aspects of reusable IP analog circuit design.

The sixth paper by George Gielen, Catholic University of Leuven, Belgium, helps designers on "porting" CAD analog circuit design.

Johan H. Huijsing

Scalable high-speed analog circuit design

Maarten Vertregt and Peter Scholtens

Philips Research Eindhoven, The Netherlands
maarten.vertregt@philips.com

Abstract

The impact of scaling on the analog performance of MOS circuits was studied. The solution space for analog scaling was explored between two dimensions: a "standard digital scaling" axis and an "increased bandwidth and dynamic-range" axis. Circuit simulation was applied to explore trends in noise and linearity performance under analog operating conditions at device level and for a basic circuit block. It appears that a *single* scaling rule is not applicable in the analog circuit domain.

1 Introduction

The two-year cycle of successive technology generations [1] has enabled an ever increasing amount of system integration per chip. For a long time, this increase in integration density was satisfied by adding extra digital functions and memory. Nowadays, interfaces to the analog world (both base-band and RF) are also packed onto these systems-on-chip.

In addition to the dominant "constant field" CMOS scaling trend, and the associated continuous decrease of the power supply voltage, there are other major hurdles for system integration. Increasing demands for extended dynamic range and signal bandwidth of modern integrated systems must also be met (Figure 1, dynamic range is plotted in the resolution in bits of an A/D converter).

J. H. Huijsing et al. (eds.), Analog Circuit Design, 3-21.

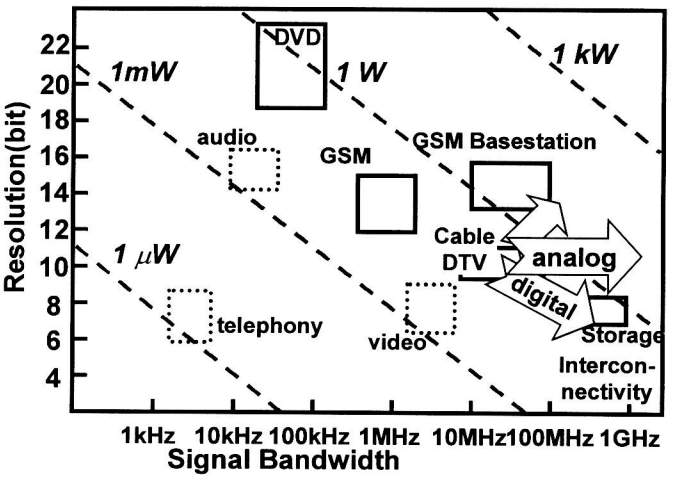

Figure 1 Application domains mapped in a resolution vs signal bandwidth plane (with a dashed "equal-power line" overlay)

It is not necessarily true that the most advanced technology generation will have the highest value for the product of the dynamic range and signal bandwidth (scaling towards the upper right-hand corner of the graph in Figure 1) [2]. Additional devices (highly linear capacitors, 2nd gate-oxide for MOS transistors) can facilitate system-on-chip integration, since those "high quality" passives enable a performance increase, and "previous generation" analog blocks can easily be re-used (voltage levels are maintained).

The combination of doing a trend analysis and having additional devices available creates two problems. Firstly (when the total function remains in a previous technology generation, because of the time needed to create and characterize high quality passives), the digital part of the system-to-be-integrated suffers from a lack of function-density and an elevated supply voltage. This has a quadratic effect on the dynamic power dissipation through $P \propto f_{clk} CV^2$. Secondly (with combined use of state-of-the-art MOS transistors for digital functions, and previous-generation MOS transistors for analog functions), the potential of the new technology is not exploited for these analog functions. The approach of adding devices is therefore useful for porting functions, but is not interesting when identifying scaling issues.

2 Scaling goals

Scaling of digital functions is directly coupled to feature size reduction. Per function, this yields a combination of continuous area reduction, speed increase and dynamic power reduction (see [3] for an example). Static power dissipation becomes a major limitation with the integration of more functions at an increased density. Speed and power improvement for digital functions is then done concurrently by selecting the optimum On/Off ratio of the MOS transistor for a certain application domain. The scaling space basically narrows down to two dimensions: on/off ratio vs feature size [4].

For analog functions, the goals of scaling are diverse. The focus can be on area efficiency, with the continued availability of a function at a fixed power dissipation, bandwidth and dynamic range. Alternately, the focus can be on the exploration of the ultimate bandwidth capability, without limiting the power or area. It could also be on pushing the combined limits of dynamic range, bandwidth and power. The preferred scaling scenario heavily depends on the goal, and we must sacrifice the performance in directions that have a lower priority to obtain a feasible solution.

The basic quadratic MOS current/voltage relationships (see [5] for example) are used to *choose the relative change* of the operating points across technology generations, as well as to *approximate* (for a limited bias range only) the analog scaling rules of Table 1:

$$I_{ds} = \frac{1}{2}\frac{W}{L}\beta^{[]}(V_{gs}-V_t)^2(1+\lambda_{(\frac{1}{L})}V_{ds}) = \frac{1}{2}\frac{W}{L}\beta^{[]}V_{gt}^2(1+\lambda_{(\frac{1}{L})}V_{ds}) \cdots (1)$$

To the first order, the quasi DC distortion is dependent on the variation across the signal amplitude through modulation of the first order derivatives g_m and g_{ds}:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \approx \frac{I_{ds}}{V_{gt}} = \frac{W}{L}\beta^{[]}V_{gt} = \sqrt{2\frac{W}{L}\beta^{[]}I_{ds}} \quad \cdots \quad (2)$$

$$g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}} \approx \lambda_{(\frac{1}{L})}I_{ds} \propto \frac{W}{L^2}\beta^{[]}V_{gt}^2 \quad \cdots \quad (3)$$

3 Scaling scenarios

We have applied several methods to explore analog scalability. The focus varies from general "power and SNR" considerations [6], to concurrent "power, SNR, and linearity" optimization for a fixed building block [7]. The focus also ranges from practical device artifacts, through compact model simulation [8, 9], to trend analysis at the functional block level [10, 11].

Here, the solution space for scaling (expressed in the well-known linear scaling factor s=0.7 from generation-to-generation) is explored using three different cases:

- Relaxed Dynamic Range (Digital scaling I)
  Standard digital scaling as in [3] for example. The focus is now on area and power reduction-per-function. The performance metrics being sacrificed are linearity [9], and the signal-to-noise ratio SNR_{pwr} (a power ratio, assumed to be dominated by thermal noise in the denominator). Neither linearity nor SNR degradation have to be a limiting factor when scaling a circuit, however, the fact that the SNR_{pwr} will degrade by a factor s^3 per generation under this scaling regime requires attention for wide-band circuits. The linearity degradation is consistent with the third harmonic intercept voltage V_{IP3} findings in [9]. In case of a dominant third harmonic, the expected signal-to-distortion ratio deteriorates by s^2 due to a combination of $\sqrt{s}$ loss of intrinsic MOS gain (g_m/g_{ds}) and insufficiently scaled V_{gt} ($\sqrt{s}$) with respect to the supply scaling (s).
- Relaxed area and power (Analog Scaling II)
  The major consideration is that analog circuits only occupy a minor portion of a system-on-chip. Area reduction is therefore not ranked as a top priority. Instead, with the application demands in mind, the focus during scaling is on the concurrent performance *increase* in terms of bandwidth and dynamic range *increase* at a fixed frequency. Maintaining the linearity part of the dynamic range requires the signal amplitude at least to scale with the supply voltage. The effect of the noise part of the dynamic range is treated

as follows, where Δf is the bandwidth of the circuit and V is the rms signal level:

$$SNR_{PWR} \propto \frac{V^2}{4kTR\Delta f} \propto \frac{g_m V^2}{4kT\Delta f} \propto \frac{V^2}{4kT/C} \quad \cdots \quad (4)$$

Thus, for constant SNR_{PWR}, CV^2 should remain constant, and the active "*Area*" is now the metric to be sacrificed:

$$\left\{ \begin{array}{l} \dfrac{const}{V^2} \propto C \propto \dfrac{Area}{t_{ox}} \\ t_{ox} \propto V \propto s \end{array} \right\} \Rightarrow Area \propto \frac{1}{V} \propto \frac{1}{s} \quad \cdots \quad (5)$$

Applying the g_m-based part of equation (4), we learn that a constant SNR requires a cubic increase of the transconductance, i.e. a cubic decrease of the impedance level, to compensate for the lower signal amplitude and the higher bandwidth. To reach this goal (bound by the feature-size scaling of L), equation (2) subsequently defines the I_{ds} to scale with $1/s$, and the W with $1/s^2$. From equation (3), it follows that the foremost sacrificed item is now g_{ds}, with $1/s^3$. For the signal carrying parts of the circuit, the overall decrease in the impedance level on the circuit nodes compensates for this sacrifice.

- Constant area and constant power (Analog Scaling III)
  The third scenario is a mixture of the previous two. A minor loss of SNR is accepted to avoid an increased area and power dissipation, whilst the linearity performance is maintained at the level of the "Analog Scaling II" scenario.

The results of these three scaling strategies were evaluated using circuit simulation (on both the device and the basic circuit block level). The use of circuit simulation safeguards the inclusion of higher-order impairments on performance (such as moderate inversion), and gives insight into the performance latitude (in signal amplitude, distortion and noise) of the scaled circuit. The scaling rules applied within these three strategies are summarized in Table 1:

Table 1 Three sets of scaling rule scenarios used to explore "analog scaling" vs "digital scaling"; sacrificed performance items are shaded.

	Item	Digital scaling I	Analog scaling II	Analog scaling III
Choices:	Length L	s	s	s
	Width W	s	$1/s^2$	$1/s$
	Supply voltage	s	s	s
	V_{signal}	s	s	s
circuit:	I_{ds} current	1	$1/s^2$	$1/s$
device:	V_{gt}	$\sqrt{s}$	s	s
Consequences:				
expected:	g_m	$1/\sqrt{s}$	$1/s^3$	$1/s^2$
$\approx\times\sqrt{s}$ found:	g_m	1	$1/s^{5/2}$	$1/s^{3/2}$
expected:	g_{ds}	$1/s$	$1/s^3$	$1/s^2$
$\approx\times 1/\sqrt{s}$ found:	g_{ds}	$1/s^{3/2}$	$1/s^{7/2}$	$1/s^{5/2}$
	$C_{active}=W\cdot LC_{ox}^{\square}$	s	$1/s^2$	$1/s$
	$C_{load}\propto C_{active}$	s	$1/s^2$	$1/s$
circuit:	Bandwidth ($\propto g_m/C_{load}$)	$1/s^{3/2}$	$1/s$	$1/s$
	SNR_{pwr} ($\propto C_{active}V^2_{signal}$)	s^3	1	s
expected:	Signal-Distortion ratio (@fixed frequency)	$\approx s^2$	$\approx 1/s$	$\approx 1/s$
found:	Signal-Distortion ratio (@fixed frequency)	$\approx s^3$	≈ 1	≈ 1
	Area	s^2	$1/s$	1
	Power	s	$1/s$	1

4 Results of scaling

4.1 Single device scaling

Compact model simulation of single MOS devices [9] was applied for various technology generations. This identifies the impact of higher-order impairments on these approximate relationships and checks for the validity of the selected operating range.

Figures 2 and 3 give an example how this validity check on the usable basic square-law model operating range is done. This is shown for an NMOS device with W/L=10/0.18µm in the 0.18µm generation. For the I_{ds} and the trans-conductance as function of gate-drive (Figure 2) and for the I_{ds} and the output conductance as function of source-drain voltage (Figure 3).

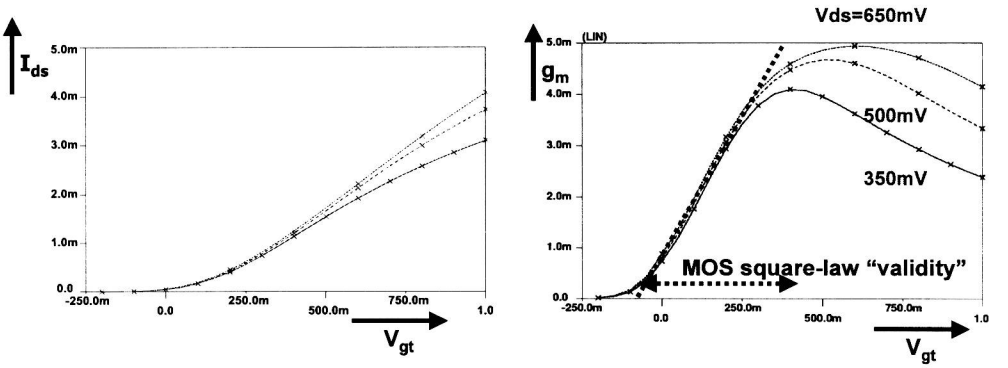

Figure 2: I_{ds} as function of V_{gt} (left) and its derivative $g_m=\delta I_{ds}/\delta V_{gs}$ (right) with an indication of the usable ("valid") operating range

We use the gate overdrive $V_{gt}=V_{gs}-V_{th}$ for all device biasing. By this choice we circumvent that variations in threshold voltage (for different device geometries, or for successive technology generations) will influence the actual analog operating point. At first glance we see for this 0.18µm example in Figure 2 a more or less linear relationship of $g_m(V_{gt})$ for the limited range of $\approx 0 < V_{gt} < \approx 350mV$ (and for the obvious condition of sustained saturation $V_{ds} > V_{gt}$).

At the edges of this range, part of the distortion caused by this deviation can be overcome by circuit design techniques such as a differential circuit topology and/or feedback. We will have a better look on the trans-conductance linearity behavior for successive technology generations later on, and first inspect the output conductance for an NMOS example in 0.18µm technology.