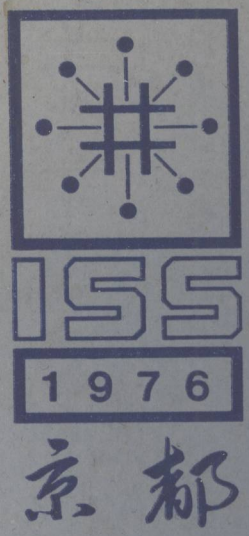

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: A. Pinet (France)
: J. Bohm (F. R. Germany)
: B. Bjurel (Sweden)
: L. R. F. Harris (U. K.)
W. O. Fleckenstein (USA)

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NO. 1A ESS – A NEW HIGH CAPACITY SWITCHING SYSTEM

John S. Nowak
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Naperville, Illinois, U.S.A.

ABSTRACT

The No. 1A ESS (Electronic Switching System) is a high capacity local switching system which combines the new 1A Processor and an expanded No. 1 ESS peripheral system. While maintaining a high degree of commonality with No. 1 ESS, No. 1A ESS has major enhancements in the areas of architecture, maintenance, installation, and administration. It also has more than twice the capacity of the older system. Fortunately, the controlled commonality in the design of the two systems makes it possible to retrofit the 1A Processor into the No. 1 ESS while the latter is in operation and with minimum cost in time and effort. The performances of the two systems are contrasted here and the design characteristics of the No. 1A ESS are discussed in text and illustrations.

1. INTRODUCTION

The success and wide-spread acceptance of the No. 1 Electronic Switching System[1,2,3] has created the need for a follow-up system which offers further cost effectiveness through increased capacity. This is being accomplished by combining the high-speed integrated circuit 1A Processor[4,5,6] with the existing No. 1 ESS peripheral equipment[7,8] to form a system called No. 1A ESS. This new system has a call-carrying capacity of approximately 240K peak-busy-hour calls, more than twice that of No. 1 ESS.

In addition to high capacity, there are other direct gains from the 1A Processor. Examples are: expanded memory capability, improved maintenance, a savings in space, and a processor which is independent from peripheral equipment. The latter allows the 1A Processor to be retrofitted into an in-service No. 1 ESS, replacing the No. 1 ESS Processor when additional capacity is needed.

The high-capacity No. 1A ESS will meet the metropolitan growth demand with fewer entities. This will result in a trunking savings as high as 25 percent in some buildings. In addition, with fewer entities there will be less double switching, and lower maintenance and administration costs. It was originally estimated that there would be more than 1600 No. 1 ESSs in operation by the year 1990. With the introduction of No. 1A ESS, however, about 20 percent fewer entities will be required to meet the same switching demands.

A simplified block diagram of a No. 1A ESS is given in Figure 1. The 1A Processor interfaces with the No. 1 ESS peripheral bus system at the peripheral interface frame. This frame contains special circuits which allow the 1A Processor to be installed and tested as a stand-alone system.

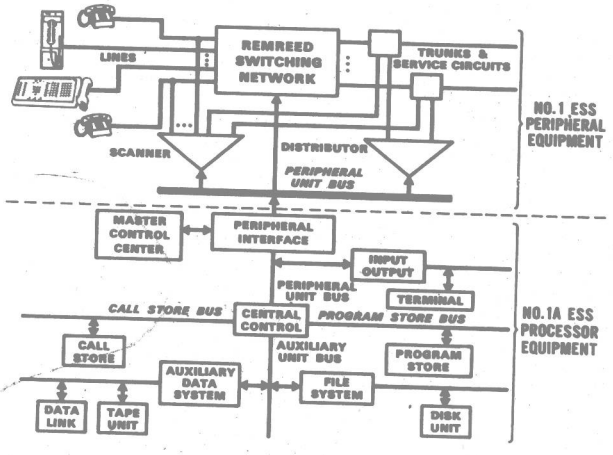

Fig. 1 No.1A ESS Block Diagram

In order to take advantage of the extensive features developed for No. 1 ESS, an off-line translator program was developed for converting existing No. 1 ESS call processing and peripheral maintenance programs into the 1A Processor language. This provides No. 1A ESS with the same features as No. 1 ESS without a major new software development and allows it to benefit from the years of experience and continued improvements made to the No. 1 ESS generic programs.

An important objective in developing the No. 1A ESS was to maintain commonality with No. 1 ESS. In a typical office, more than 90 percent of the frames are identical to those used in No. 1 ESS. All maintenance procedures and teletypewriter messages for the common frames are identical, and service order formats and procedures remain the same. Likewise, the traffic measurement input and output data is identical. The differences between the systems involve

only the 1A Processor. With this degree of commonality the No. 1A ESS can be rapidly integrated into the existing telephone network with less training for craftspeople.

To utilize the capacity of the 1A Processor, the existing limits to the size of the No. 1 ESS network must be expanded. Rearranging a No. 1 ESS network increases its capacity and allows the total system capacity to approach that of the 1A Processor.

The features of the No. 1A ESS are described in further detail in the text of this paper, followed by a discussion of the program organization, development techniques, and the status of the project.

2. NETWORK ARRANGEMENTS

There are numerous parameters which can affect system capacity. They range from peripheral address bus length limits to memory address spectrum constraints. Two basic parameters which affect the system capacity of the No. 1A ESS are the call handling capability of the processor and the network capacity. With the use of the high-speed 1A Processor, the existing No. 1 ESS network configuration would limit the system capacity to less than the 1A Processor call processing capability. Therefore, the No. 1A ESS development includes expanding the existing No. 1 ESS line and trunk networks to match the processor capacity.

Figure 2 compares the line terminal capacities for No. 1 and No. 1A ESS. The No. 1 ESS line link networks are limited to 16. The extended No. 1A ESS line link network arrangement allows for up to 32*. The extended network makes use of trunk link networks which are doubled in size. This is accomplished by merging two existing No. 1 ESS 1024 junctor terminal networks into a 2048 junctor terminal network. This combination of networks result in a switching capacity of about 10,000 ERLANGS.

	NO.1 ESS		NO.1A ESS	
CONCENTRATION RATIO	LINE LINK NETWORKS	LINES	LINE LINK NETWORKS	LINES
2:1	16	32K	28	57K
3:1	16	49K	28	86K
4:1	16	65K	28	114K
6:1	16	98K	21	129K

Fig. 2 Line Termination Capacities for No.1 ESS and No.1A ESS

The extension of the line link network and the doubling of the trunk link network is accomplished using existing frames. The major effort is in the reprogramming of the No. 1 ESS network path programs and in the development of engineering algorithms and support software tools to handle the extended configuration.

Figure 3 shows the system capacity limit as a function of network capacity. The processor capacity of 240,000 peak-busy-hour calls is adjusted to 185,000 engineered calls per hour in accordance with a typical peaking factor of 1.3 between peak busy hour and average busy season busy hour traffic. As illustrated, the processor capacity is not affected by the network usage and therefore remains constant and appears as a solid horizontal line. The existing No. 1 ESS network call-carrying capacity of 5800 ERLANGS shows that the network is the limiting factor and that for 0.055 ERLANG per call the system capacity exhausts at about 108,000 engineered calls or 140,000 peak-busy-hour calls. The extended No. 1A ESS network call carrying capacity of 10,000 ERLANGS illustrates that for the same 0.055 ERLANG per call the processor and network capacity are in reasonable balance at 185,000 engineered calls or 240,000 peak busy hour calls.

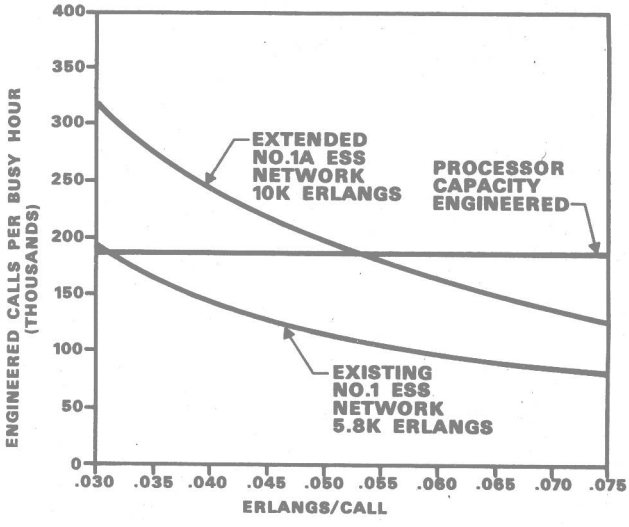

Fig. 3 Network Capacity

3. RETROFIT

The ability to increase the capacity of an existing No. 1 ESS by replacing its processor with the 1A Processor without any serious service interruption has significant economic value. This capability avoids adding a new entity when additional capacity is needed.

*For a typical traffic mix with concentration ratios of up to 4:1, the constraints on the line-to-trunk junctors limits the line networks to 28. A software constraint on terminal handling further limits the line networks to 21 for the 6:1 concentration ratio.

As mentioned earlier, the 1A Processor peripheral interface frame is the single point of contact with the No. 1 ESS peripheral system. Through this interface frame, the 1A Processor peripheral bus is made compatible with the No. 1 ESS peripheral bus system. The peripheral interface frame is designed with a bus loop-around feature which, combined with special programs, makes the 1A Processor a self-contained system. The bus loop-around feature is used for maintenance of the bus system and to verify the 1A Processor bus access without using a peripheral system. It is used extensively during retrofit installation.

During the retrofit installation interval, the 1A Processor is tested using generic maintenance programs as a stand-alone system. Through special test access equipment, the 1A Processor can obtain limited access to the No. 1 ESS peripheral bus system while the No. 1 ESS Processor is in control of the system. Upon completing this test sequence the special test access equipment is used as a signaling link between the two processors. Through this signaling link, data is transferred to the 1A Processor to establish a data base identical to that currently existing in the No. 1 ESS. This process continues until the 1A Processor is in the proper state to assume total control of the peripheral system, at which point the No. 1 ESS Processor is powered down and removed.

4. PROGRAM ORGANIZATION

The No. 1A ESS generic program is derived from three sources:

a. Maintenance and administrative programs related to the 1A Processor. These programs are common to all applications using the 1A Processor (150,000 instructions and 215,000 data words).

b. Call and peripheral maintenance programs converted from No. 1 ESS (215,000 instructions).

c. New application programs (30,000 instructions and data words).

Figure 4 illustrates the relative size of each of these program sources.

The 1A Processor common programs consist of processor recovery, diagnostic and administrative programs. The administrative functions include the control and data-handling features for units such as the disk, tape, and input-output. These programs are used in other systems using the 1A Processor, such as the No. 4 ESS[9,10,11].

The No. 1 ESS call and peripheral maintenance programs cannot be used in No. 1A ESS until they are converted into 1A code. Through this process the features in No. 1 ESS become transferable to No. 1A ESS quickly and without a major redevelopment. This process is described in the following section.

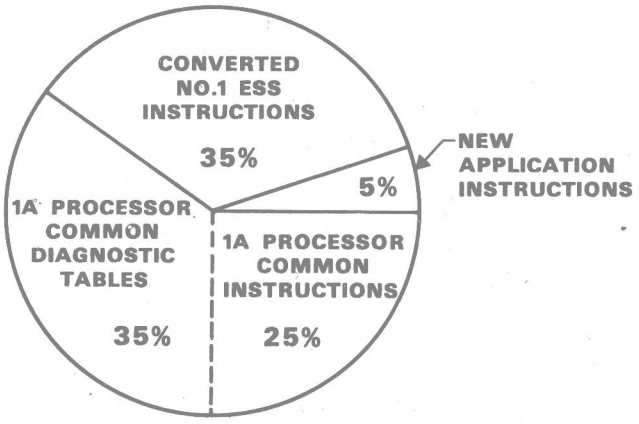

Fig. 4 No.1A ESS Program Organization

The third source, the new application programs, are of three types:

a. Software interface programs - programs to allow the converted and 1A Processor common programs to coexist.

b. Hardware interface programs - programs to resolve the operational differences between the No. 1 ESS Processor and the 1A Processor.

c. New program features unique to No. 1A ESS.

An example of the latter is the memory arrangement in the 1A Processor, which allows infrequently used programs to be resident only in the disk memory until needed. At execution time, the disk system pages the desired program into the primary core memory. A control structure using this facility was developed to allow for the execution of programs which are not part of the system generic program. Such programs are presently restricted to features like extended maintenance testing, frame growth tools, and administrative programs. This group of programs, called library programs, survives from one generic to the next and is not resident in the system. When the need for these programs arises they are loaded into the system from tape and can remain in the system for extended intervals.

5. CONVERSION PROCESS

The philosophy underlying the conversion process is that it is currently more efficient to convert No. 1 ESS programs into No. 1A ESS programs than to manually reprogram and document a new program. Our objective has been to automate the conversion process as much as possible to minimize manpower requirements and human error. Even so, the conversion process is only a first step in developing a No. 1A ESS program, and must be followed by program testing and system integration.

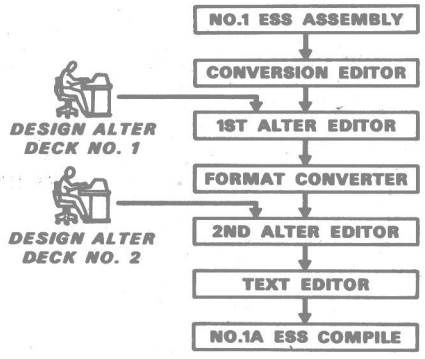

Fig. 5 No.1 to No.1A ESS Program Conversion

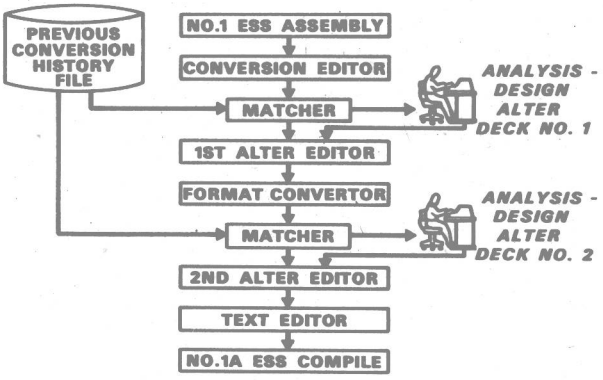

Fig. 6 No.1 to No.1A ESS Program Conversion with Matcher

The 1A Processor is architecturally enhanced by a more powerful order structure and an increased memory spectrum. These intentional technical differences made the 1A Processor order structure different from No. 1 ESS, which complicates the conversion process. The differences include: data word size (24-bit versus 23-bit), 1A Processor long and short instructions (48-bit and 24-bit), item processing instructions, register set differences, etc. As a result, a relatively complex off-line translator is required to effect the conversion. This translator automatically converts about 80 percent of the No. 1 ESS instructions and flags the remaining 20 percent for analysis by a program designer. Approximately one-third of these flagged instructions require manual changes to a portion of the program and in some cases a minor redesign. The programmer performs a flow analysis of the flagged program strings to resolve the problems.

Figure 5 illustrates the flow of events during the process of converting No. 1 ESS code into 1A code. The No. 1 ESS source is assembled to obtain a listing data set which is passed through the conversion editor program. The editor is basically a preprocessor that prepares the code for format conversion and flags certain problem areas. The editor output is analyzed by a programmer and changes are manually input to the alter program along with the editor data set. The alter program changes the data set and prints out a listing of the altered data set.

The format converter changes the No. 1 ESS code to No. 1A ESS code and outputs a flagged listing and a data set. The output of the format converter is analyzed by a programmer and corrected as required. These changes are input to a second alter program and the data set is prepared for the general purpose text editor.

The output of the translation process is a No. 1A ESS source program equivalent in function to the input No. 1 ESS source. Basically, the translator analyzes each No. 1 ESS instruction and develops the No. 1A ESS equivalent through a series of algorithms designed specifically for the input instruction and its particular set of options. In some cases the translator analyzes a string of instructions to derive an equivalent sequence. The conversion process maintains the state of most registers in No. 1A ESS as they were in No. 1 ESS, which minimizes interface problems between programs and subroutines. However, the state of certain No. 1 ESS registers cannot be maintained due to significant order code differences. For these cases, such registers are monitored by the translator to determine if they are in the correct state.

Conversion algorithms are based on all possible uses of an instruction. Where possible, the conversions will reproduce the exact conditions of the No. 1 ESS instruction. While this is not as efficient as selecting the optimum 1A instruction in some instances, the loss of efficiency in terms of processor real-time is estimated to be less than 5 percent.

The translation process described here has been used to convert three No. 1 ESS generic programs into 1A code for evaluation in a system test laboratory. Each conversion led to improvements in the translator programs. The first attempt to convert 140,000 No. 1 ESS instructions required ten programmers for 6 months. The most recent conversion of 215,000 No. 1 ESS instructions required ten programmers for 2 months. The major improvement in the process came from the introduction of a conversion matcher. Figure 6 illustrates the flow of events, including the conversion matcher steps. Basically, this step salvages previous conversion effort by identifying the strings of code that have not changed since the last conversion. The matcher process is complicated by additions and deletions made to the No. 1 ESS source which alter the identification of the old code. The matcher compares strips of code in the old and new files to arrive at reference points. These reference points are used to identify the changed areas.

In addition to the conversion matcher, the translator programs were modified to reduce the number of flags and to further optimize the results. While the conversion process results in the same number of instructions in No. 1A ESS as in No. 1 ESS, the smaller word size difference results in an overall bit savings in No. 1A ESS.

6. PROGRAM VALIDATION

Preparing the numerous tests to verify the programmed features of a large real-time system is a complicated job and requires a great deal of effort. Some of the problems are involved with test portability and completeness. Generally, tests are sensitive to address locations and become directly coupled to a generic program issue. During the development of the No. 1A ESS frequent program reloads, which often contained new features, were required. For each reload of the generic program the tests had to be redefined and adjusted to account for the new address locations and data differences. Also, completeness of these functional tests was difficult to evaluate, since the task of determining whether all program strings have been accessed is a time consuming one.

To manage these problems, an automatic test administration system was developed which makes the tests portable from one generic to another and includes methods to measure test completeness. This systematic regression test system not only tests for completeness, it also automatically adjusts each test to a newly reloaded generic program. Through this system, tests designed for off-line simulation are salvaged and made usable for the system test laboratory.

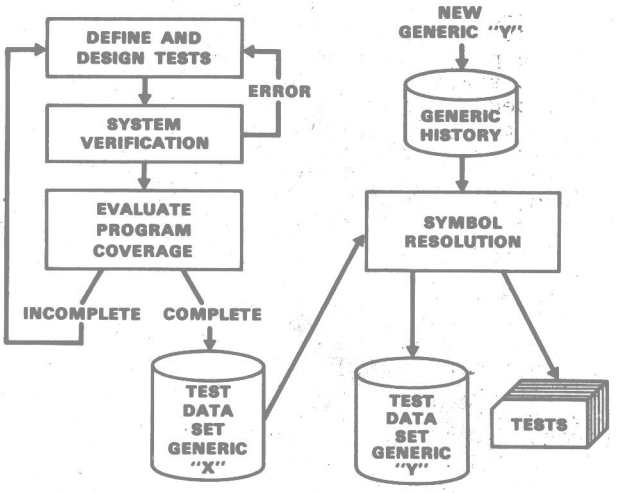

Fig. 7 Test Administration for Portability

Figure 7 is a simplified flow diagram that highlights these characteristics of the support system. The program coverage of the functional tests is determined by a system test laboratory tool which, during the execution of a test, flags instructions fetched from the program store. The flagged data is processed and a report is generated which identifies any strings of instructions not accessed within the particular program. Program designers review this report, examine the program, and design additional tests until the coverage is considered complete. These tests then become part of a test data set

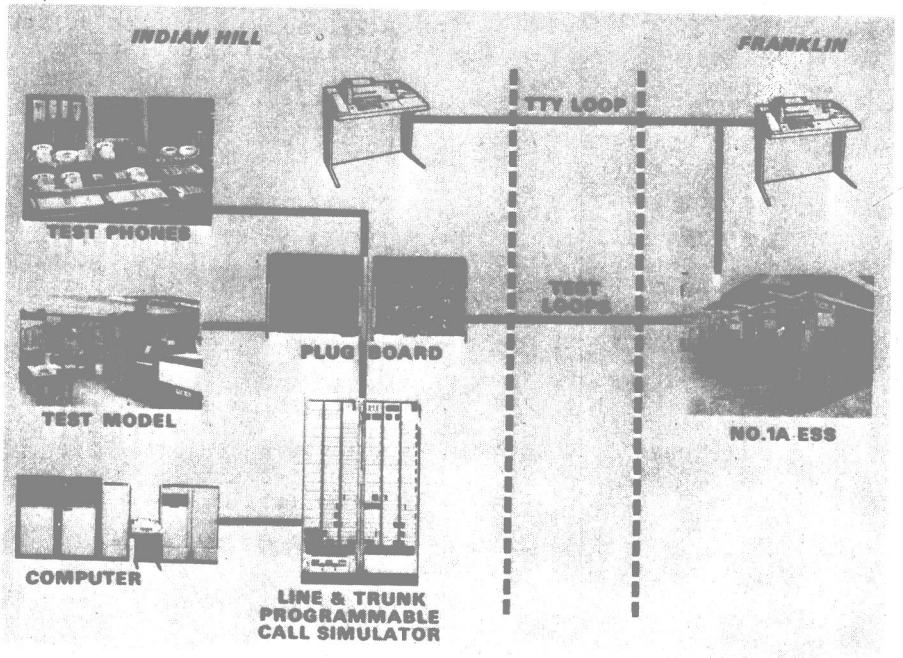

Fig. 8 Remote Testing

for that particular generic. When a new reloaded generic program is to be retested, the test data set and a history of the new generic program are processed by the support system. The symbol resolution is completed and a new test data set along with a test deck is produced. This test deck is then systematically applied to the system test laboratory through a utility system; a technique which allows rapid testing and verification of the previously tested functions in the new generic program.

At the Bell Laboratories Indian Hill system test laboratory, special equipment is available which allows sophisticated program and system testing. One of these test facilities, also used for No. 1 ESS, is the programmable electronic call simulator (PECS). This facility has access to the No. 1A ESS network at the line and trunk terminals where signals are applied and results monitored during each step of the call sequence. The PECS facility can be programmed to generate abnormal calls and monitor the system's reactions. The results of these tests along with teletypewriter messages verify the correctness of each call sequence.

This facility is also being used to test the first application office at the Franklin building in Chicago, Illinois. As shown in Figure 8, test loops interconnect the PECS facility in the Indian Hill laboratory with line terminals in the Franklin office. The test loops are arranged so that they can also be reconnected to normal station equipment located in the system test laboratory. This arrangement, in addition to a system teletypewriter which is also remoted to the test model, allows the design staff at Indian Hill to have direct access to the Franklin system (located some 30 miles away) to solve problems during the first office test period.

7. STATUS

The development of the No. 1A ESS has progressed as planned. The first No. 1A ESS is in its final system evaluation stage at the Franklin building in Chicago. Figure 9 is a photograph of the maintenance control center at the Franklin office. This system is scheduled to be placed into service in January, 1977. As of October, 1976, there are six additional systems being installed, five of which will be placed into service by the end of 1977. During 1978, 52 additional systems are scheduled to go into service. By the end of 1978, 28 different states in the United States will have at least one, and some as many as seven, No. 1A ESSs. These systems are primarily used to replace panel and step-by-step offices. In one installation the No. 1A ESS will be replacing six local step-by-step number groups.

The development plan for No. 1A ESS includes an Issue 1 program which has a feature content consistent with the early 1976 feature content of No. 1 ESS. The development of new No. 1A ESS programs

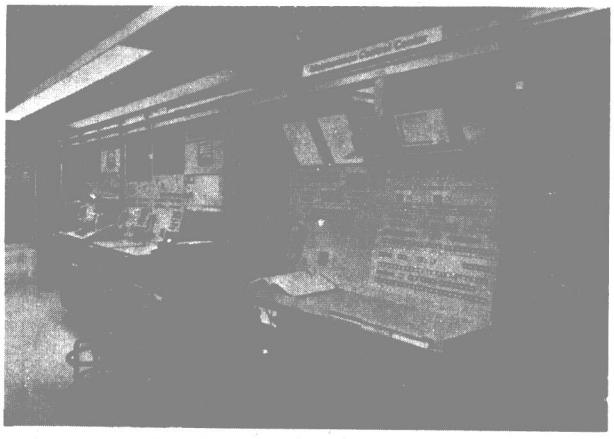

Fig. 9 Franklin Office

will track the release of No. 1 ESS programs, issue by issue. The 1A Processor retrofit into an operating No. 1 ESS is scheduled for a first application in early 1978.

8. CONCLUSION

The No. 1A ESS is a new member of the ESS family. The heart of the system is the 1A Processor, which is also used in the No. 4 ESS. The design of the No. 1 ESS network is inherently flexible and can therefore be extended for use in No. 1A ESS. This expanded network, along with the 1A Processor, forms a system which meets the large office metropolitan demand.

For the next few years the No. 1A ESS will provide the same customer features as does the No. 1 ESS plus administrative features which are unique to the No. 1A ESS. As ESS development progresses and new large-customer features are required, No. 1A ESS will become the most suitable vehicle for providing these features. Because of the large number of No. 1 ESS systems in operation, however, every effort will be made to have most features available in both systems.

The No. 1A ESS is a system which can grow to more than twice the call handling capacity of No. 1 ESS. This system has evolved from No. 1 ESS and, as a result, benefits from the years of experience and the improvements made to the No. 1 ESS. The additional capacity, along with the new features of the 1A Processor, results in a large economic value to the Bell System and, ultimately, to the customers it serves. This switching system has been quickly accepted by the operating telephone companies and is being introduced at a rapid rate.

ACKNOWLEDGMENT

The development of the No. 1A ESS required the cooperation and support of members of Bell Laboratories, Western Electric, and American Telephone and Telegraph. The author wishes to acknowledge the important contributions of all those who participated.

In addition, the author wishes to acknowledge the cooperation and effort of the people in the operating telephone companies who helped in the planning of the first seven No. 1A ESS installations.

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THE NEW PERIPHERAL SYSTEM FOR NO.1 AND NO.1A ESS

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ABSTRACT

A new peripheral system has been designed for No. 1 and No. 1A ESS. This paper describes this system and the objectives of its development.

1. INTRODUCTION

A new peripheral system has been developed for No. 1 and No. 1A ESS. The objective of this development was to modernize the peripheral system, reduce its size, enhance its potential for cost reduction, make it easier to engineer, install, and maintain, and to extend its flexibility for service. This system includes remreed line link and trunk link switching networks, miniaturized plug-in trunk and service circuits and HILO circuits which permit equivalent 4-wire toll-grade switching over the remreed trunk link networks. This new periphery is fully compatible with both the No. 1 and No. 1A Processors and existing and new software. At the time of the Kyoto Meeting (October 25 to 29, 1976), approximately 5.9 million line terminal pairs and 3.0 million trunk terminal pairs of remreed, 150,000 miniaturized plug-in trunk circuits (minitrunks) and 15,000 HILO circuits will have been shipped to the field.

2. REMREED NETWORKS[1,2]

The objective of the remreed development was to utilize new technology to design switching networks which are more economical and more flexible for the Operating Companies. These networks occupy one-fourth to one-third the space of ferreed networks. They also require less installation effort and offer the potential for significant cost reduction.

An equipment comparison between 4096 terminal regular traffic (4:1 concentration ratio) line link networks using ferreeds and the equivalent network using remreed and electronic control is shown in Figure 1. The ferreed network consisted of eight frames totaling 39 feet in length. The equivalent remreed network consists of three frames totaling 9 feet, 9 inches in length for a size reduction of four to one. A similar comparison is made for 2048 terminal high traffic (2:1 concentration ratio) networks in Figure 2. In this case, the size reduction achieved is three to one. The comparison between 1024 terminal (1:1 concentration ratio) trunk link networks is shown in Figure 3. In the case of the trunk link network a space reduction of four to one is achieved and there is but one remreed frame instead of eight ferreed frames. This has permitted the wiring of the trunk link network interframe links and rather complete trunk link network testing to be done in the factory and a marked reduction in installation effort. The percentage reductions in required installation effort for remreed networks over ferreed are given in Table 1.

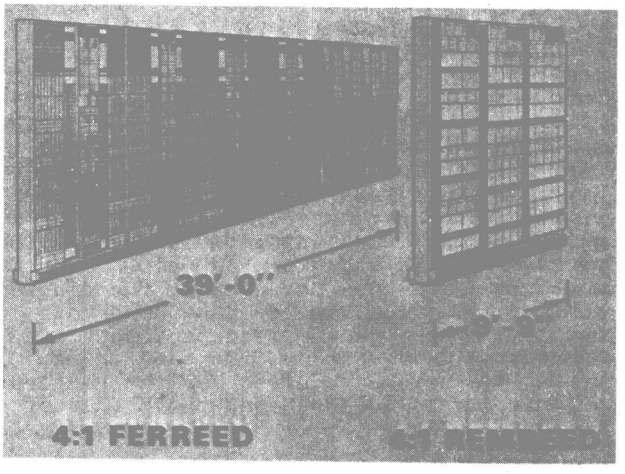


Fig. 1 Line Link Comparison

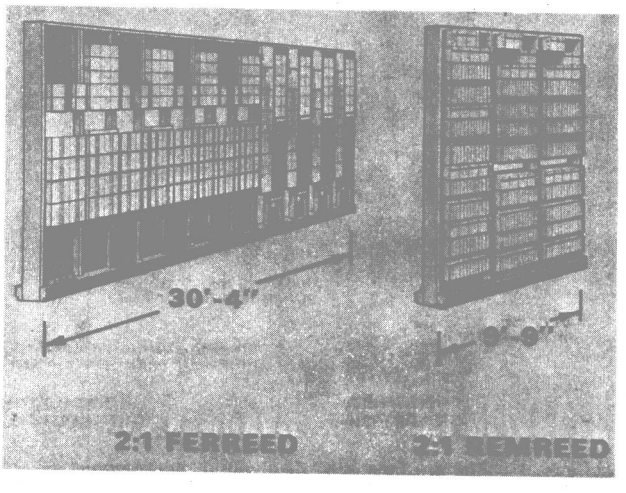


Fig. 2 Line Link Comparison

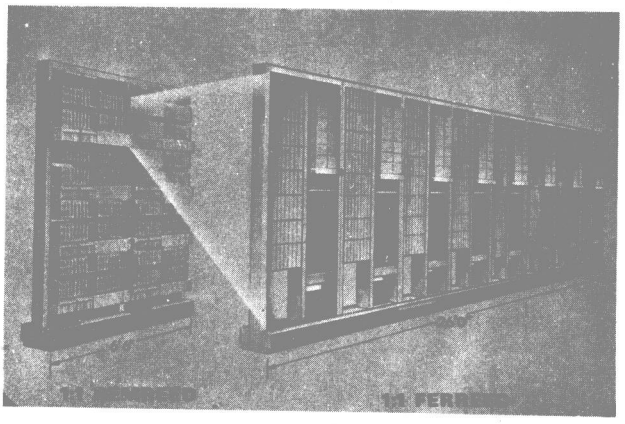


Fig. 3 Trunk Link Network Comparison

Table 1 Installation Effort

Link	Network	Percentage Reduction
1:1	TLN	50%
2:1	LLN (High Traffic)	31%
4:1	LLN (Regular Traffic)	25%

The remanent reed (remreed) crosspoint consists of self-latching reeds that are enclosed in sealed glass envelopes surrounded by control windings (Figure 4). The self-latching reeds act as electrical contact members of the crosspoint and are formed from remendur, a switchable magnetic material. This differs from the ferreed crosspoint where the switchable magnetic material is located outside of the glass envelope. A photograph comparing two ferreed 8-by-8 switch packages with one remreed switch package containing two 8-by-8 crosspoint arrays is shown in Figure 5. The mounting plate area occupied by the single remreed switch package is one-third that required by the two ferreed packages. Since both packages have the same frame depth, the volume required for the remreed network fabric is about one-third that of ferreed.

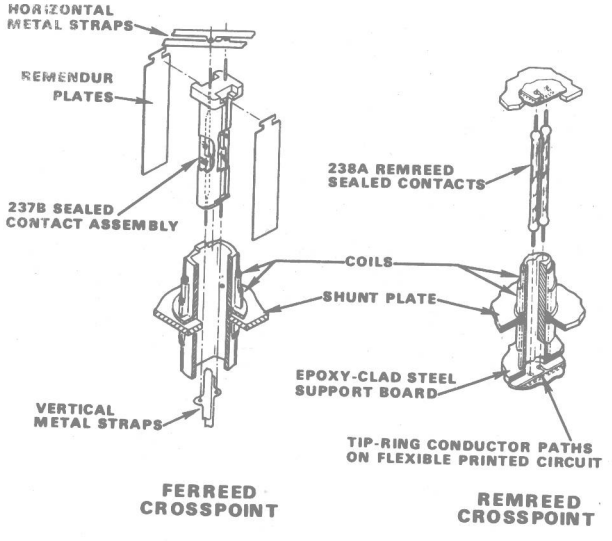


Fig. 4 Two Wire Crosspoint Assemblies

Fig. 5

The use of lower coercive force remendur and the improved magnetic efficiency of the remreed crosspoint reduces the required peak pulser current and voltage over that used to operate ferreed switches. A path through a 64-by-64 array called a grid, illustrated in Figure 6, requires a pulse of about 4 amperes peak at 100 volts to latch a pair of crosspoints as compared with a 9-ampere pulse at over 300 volts in a ferreed grid. The remreed controller uses discrete PNPN transistors and diodes to steer pulse current through the matrix in place of the wire spring relay contacts used in the ferreed design.

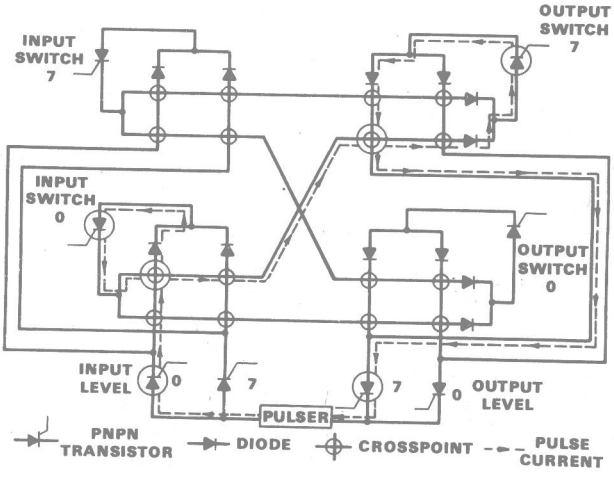
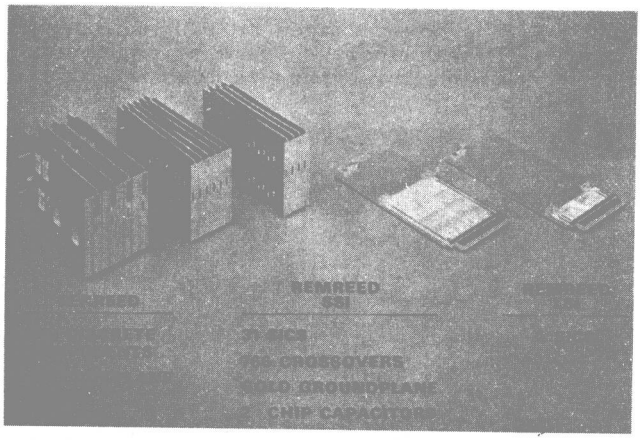


Fig. 6 Control Matrix

The PNPN transistors are controlled by integrated circuit logic and translators replacing the discrete logic and reed relay translators used in the ferreed network (Figures 7 and 8). The initial remreed network logic and translator design used small scale integration (i.e, six to eight gates per chip) Collector Diffusion Isolation (CDI) integrated circuit chips for logic and translation and Junctor Isolated Monolithic (JIM) integrated circuit chips for electrical interfacing with the PNPN transistors. In more recent design, the CDI and JIM chips have largely been supplanted with Injection Logic and



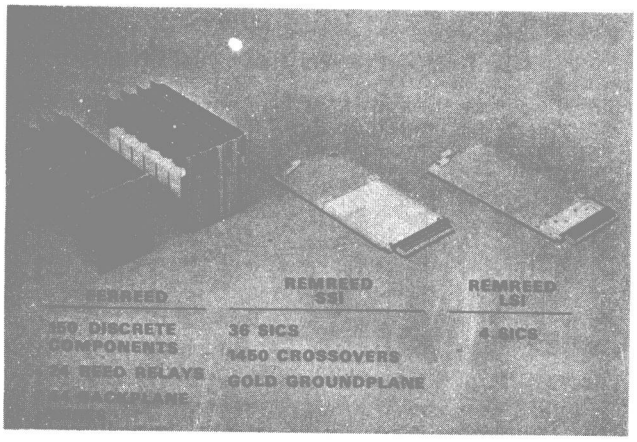


Fig. 8 Translator Comparison

custom buffer LSI chips (i.e., 40 to 60 gates per chip) for additional cost and power savings.

A single originating line scan point is associated with each line. Because of this fact and in order to maximize cost and space savings, a new originating line scanner was designed as part of the remreed line link network development. This scanner consists of a semiconductor controller using integrated circuits and ferrod scan elements. In order to save unit wiring and frame cabling and to maximize space savings the first stage switch packages (Figure 9) in the remreed line link network contain the line ferrods and their companion cut-off contacts as well as the first stage crosspoints. The scanning system has also been speeded up from 9.8 microseconds to 7.0 microseconds in order to increase the No. 1A ESS Processor capacity from 210,000 to 240,000 peak busy hour calls in order to more nearly match the capacity of the extended switching networks* available in No. 1A ESS.[3]

The remreed network was the first major No. 1 ESS peripheral system component to be redesigned under the software compatibility constraint. All call processing

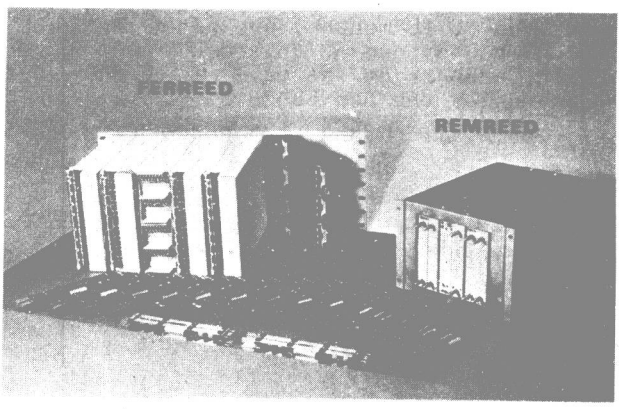


Fig. 9 32×16 Concentrator Comparison

and fault recognition programs control remreed and ferreed networks interchangeably. This permits the addition of remreed networks to the many No. 1 ESS machines already in service with ferreed networks. The same diagnostic programs, used to locate faults in ferreed networks, are used for remreed networks but with a new trouble locating manual.

The remreed switching networks have been designed for both balanced and HILO transmission. Some worst case grid transmission measurements are given in Table II. This performance meets or surpasses the transmission objectives for the development and is further discussed in Reference 1.

Table II Grid Transmission Performance

1. Single Disturber Equal Level Crosstalk

	Minimum Coupling Loss-dB		
Frequency-KHz	Balanced (a)	HILO Inter-Channel (b)	HILO Intra-Channel (c)
3.2	93	117	93
32	88	95	72
400	67	60	45
750	61	50	35

a. Between two T-R conductor pairs
b. Between two T or R conductors except mate conductors
c. Between T and mate R conductors

2. Impulse Noise

Less than 1 millivolt into 110 ohm termination.

3. Minimum 3 dB bandwidth (balanced mode)

Greater than 7 MHz.

Ease of maintenance and reliability of service were other design requirements. All controller circuitry and fabric modules (concentrators and grids) are plug-in for ease of maintenance. Some early in-service reliability data taken on 49 TLNs in seven central offices for varying lengths of

* Up to twenty-eight line link networks or sixteen 2048 terminal trunk link networks.

time (up to 18 months) are given in Table III. The purpose of this study was to get quick feedback on the early in-service performance of the new product.

Table III Trunk Link Network Study

Device	Number of Device Hours	Expected FIT Rates	Observed FIT Rates
238A Remreed Contact	3.1×10^{10}	1	1.6
446F Diode	5.4×10^{9}	2	0.2
59A PNPN Transistor	5.3×10^{8}	20	5.7
66S Transistor	8.6×10^{8}	30	14.0
137 CDI SICs	7.7×10^{8}	10	2.6

3. MINITRUNKS

The objective of the minitrunk development was to utilize new technology to design trunk switching and other associated circuitry which are more economical and more flexible for the Operating Companies. These circuits occupy one-seventh to one-third the space of their predecessors. They also require less engineering and installation effort and offer significant opportunity for cost reduction.

No. 1 and No. 1A ESS trunk circuits fall into two general categories: Universal Trunks (UTs) and Miscellaneous Trunks (MTs). A comparison between a minitrunk UT and an older-design UT is shown in Figure 10. As can be seen, the UTs came in relatively

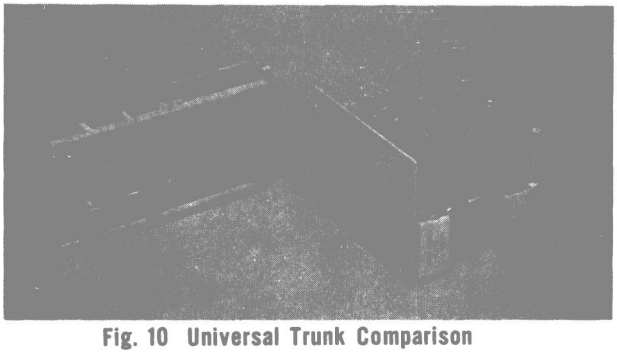


Fig. 10 Universal Trunk Comparison

large, pluggable units and the minitrunk UTs are one-third the size of their predecessors. A comparison between a minitrunk MT and an older-vintage MT is shown in Figure 11. The MTs were large hand-wired units mounted in individually job engineered and manufactured equipment frames. The minitrunks use cost and size reduced transmission and switching components such as small inductors, transformers, capacitors, and magnetically latching relays designed for printed circuit mounting. Small low-cost circuitry replaces large transformers previously used for lightning surge protection. Electronic circuitry replaces special purpose electromechanical components. Increased range is provided as are improved transmission and switching capabilities. It is a feature of the minitrunk development that both the MTs and the UTs are now packaged on plug-in circuit boards in standardized frame arrangements along with their scanners and signal distributors.

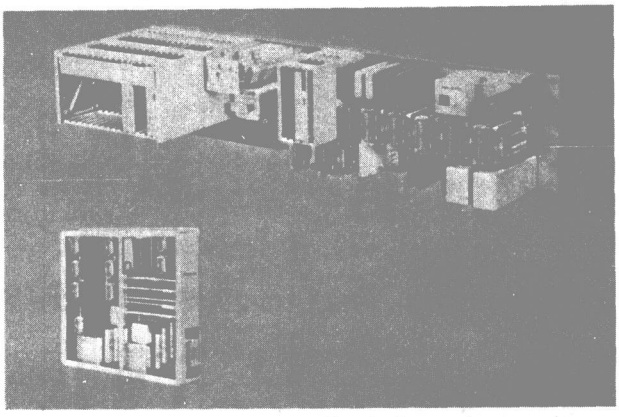


Fig. 11 Miscellaneous Trunk Comparison

An MT frame comparison is shown in Figure 12 and a UT frame comparison is shown in Figure 13. The center bays of the older

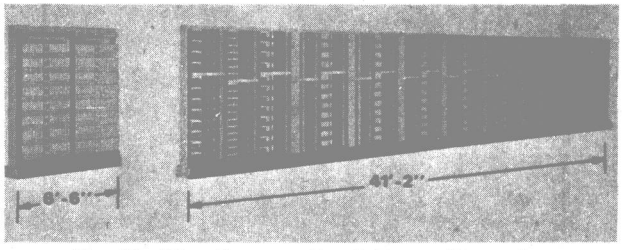


Fig. 12 Miscellaneous Trunk Frame Comparison

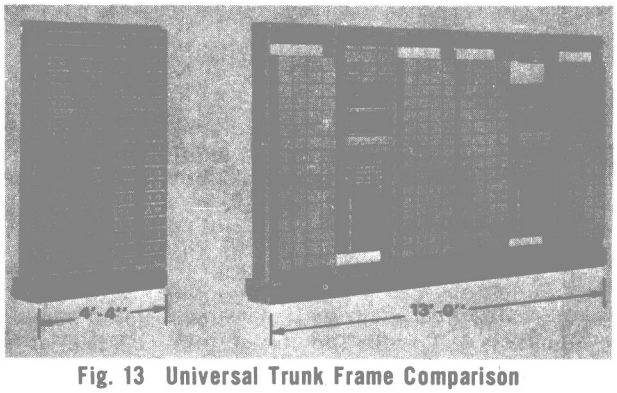


Fig. 13 Universal Trunk Frame Comparison

UT frames contain the trunk scanners and signal distributors. Different trunk circuit types have different numbers of associated scan and signal distributor points, typically from one to nine scan points and from zero to ten signal distributor points. Because of this fact and in order to maximize cost and space savings a new trunk scanner and a new signal distributor were designed as part of the minitrunk development.

In Figure 14, we see the portions of the old and new UT frames which are devoted to scanners. The new trunk scanner design is very similar to the design of the line scanner developed for the remreed line network. The differences are the distribution of the ferrods on circuit packs near their trunk units rather than in line concentrator packages and the greater sensitivity of the

trunk circuit ferrods.

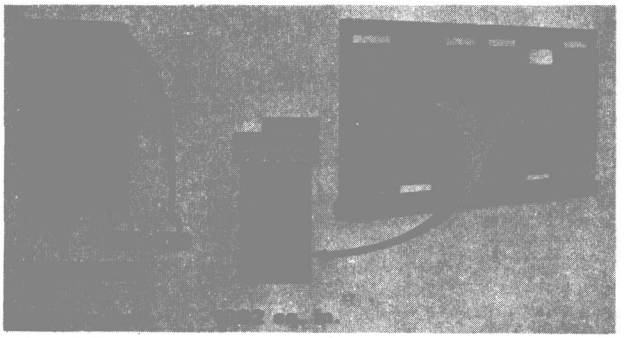


Fig. 14 Universal Trunk Scanner Comparison

In Figure 15, we see the portions of the old and new UT frames occupied by signal distributors. The new signal distributor is an all-electronic distributor in contrast to its relay predecessor. It consists of a semiconductor controller using integrated circuits and distributor points of discrete semiconductor TRIACs. The new distributor is used with both minitrunks and existing trunk circuits of earlier design.

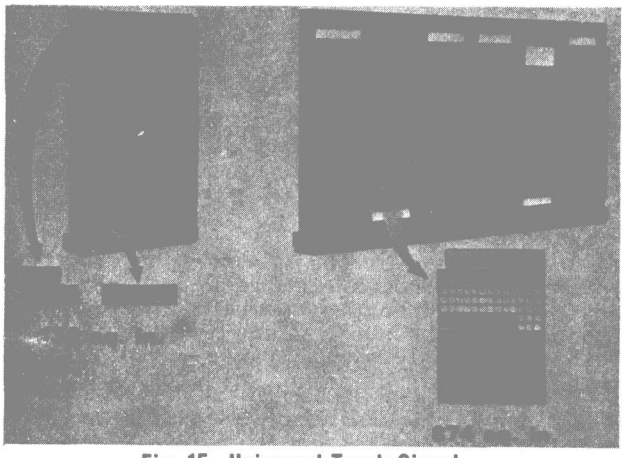


Fig. 15 Universal Trunk Signal Distributor Comparison

4. OFFICE IMPACT

Remreed networks and minitrunks result in significant space savings and installation interval and cost reduction potential (Table IV). Each development has the objective of reducing material costs by one-third.

Table IV No. 1 ESS Office Impact

	18,400 Line (3:1 CR) 4,400 Trunk (1:1 CR)		"Typical" 20,000 Line
	Space Reduction	Cost Reduction (at Objective)	Estimated Installation Interval Reduction
Remreed	30%	12%	9%
Minitrunk	26%	7%	9%
	56%	19%	18%

5. HILO

The objective of this development was to provide No. 1 and No. 1A ESS with a HILO 4-wire network for use in combined local/toll, small to medium size toll, and other applications which benefit from 4-wire switching. Such a network results in reduced first costs, reduced maintenance, improved transmission and other benefits to the Operating Companies.

The HILO 4-wire network makes use of an unbalanced transmission technique (Figure 16). This technique employs a single "wire" for the "east-going path" and another single "wire" for the "west-going"path. Thus, switching networks having two physical paths per connection are used for equivalent 4-wire transmission. The paths involved must be modestly short. The driving or modulating end is the equivalent of a voltage controlled current source while the receiving or demodulating end is the equivalent of a current controlled voltage source . As seen from the single "wire" link in between, the modulator is high impedance and the demodulator is low impedance. Hence the name HILO. This impedance relationship controls the noise and crosstalk impairments usually associated with unbalanced transmission. With regard to signaling, an inherent attribute of HILO is that it provides the capability to speed up cross-office supervision. The speed of passing answer supervision is reduced several fold to 8 to 12 milliseconds.

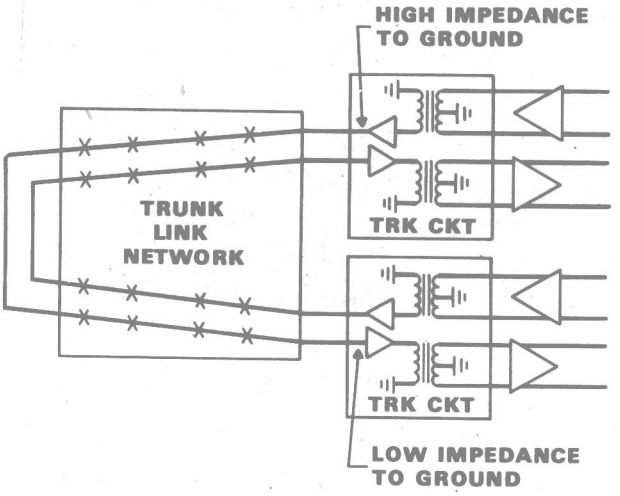


Fig. 16 Hilo 4-Wire Switching Complex

The modulator-demodulator and associated signaling circuit and transmission facility interface circuit are packaged together as trunk circuits. Plug-in trunk units each containing two HILO trunk circuits are shown in Figure 17. The modulator-demodulator and interface circuits are semiconductor circuits consisting principally of integrated circuits. The signaling circuit makes use of small components similar to, or the same as, those used in the minitrunk circuits.