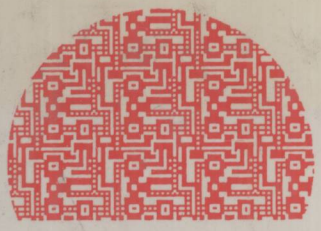

VLSI Video/Image Signal Processing

edited by
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VLSI VIDEO / IMAGE SIGNAL PROCESSING

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VLSI VIDEO / IMAGE SIGNAL PROCESSING

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Introduction

Due to the progress in VLSI technology, integrated circuit chips are now available that allow Video/Image signal processing to be performed with a single VLSI chip or small sets of VLSI chips. Recent standardizations on bandwidth compression schemes for still images (JPEG) and motion pictures (H.261, R723, MPEG) also encourage the development of VLSI Video/Image processors for cost effective solutions. Furthermore, recent trends suggest that the standardization on HDTV bandwidth compression for broadcasting and storage purposes is just around the corner.

In terms of device technology, however, the progress achieved in increasing speed is not as high as that achieved by integration. The development of high speed systems is due to architectural effort, rather than device technology. This is why high speed architectures, such as for special wired logic realization and for multi-processors, are of great interest to VLSI system designers.

This special issue reports current efforts in VLSI Video/Image signal processors. The articles concern recently developed chips, architectures for multi-processors, and methodologies used for implementing algorithms with general purpose processors. This special issue begins with an overview of VLSIs in picture coding by Tatsuo Ishiguro of NEC, who received the Emmy Prize last year for his pioneering work in video bandwidth compression. In the second article, Robert Forchheimer, Keping Chen, Christer Svenson and Anders Ödmark describe an interesting chip, which contains 256 A/D converters and bit-serial processors. Hiroyuki Nakahira, Masakatsu Maruyama, Hideshi Ueda and Haruyasu Yamada introduce a DSP with multi-processor capability for processing images. A JPEG chip, developed by Peter A. Ruetz, Po Tong, Daniel Luthi and Peng H. Ang, can process video signals in real time. A DCT chip, reported by Takashi Miyazaki, Takao Nishitani, Masato Edahiro, Ikuko Ono and Kaoru Mitsuhashi, can handle an HDTV signal. This chip was designed with the aid of an application specific silicon compiler developed by the authors.

Three articles concern multi-processor architecture for video signal processing. Klaus Gaedke, Hartwig Jeschke and Peter Pirsch report a parallel processor architecture, whose element processor is RISC with additional hardware for multiply-and-add operations. J.M. Engels, R. Lauwereins and J.A. Peperstraete developed a video signal processing board by which a multi-processor can be easily realized in a pipeline and/or parallel architecture. Another approach is to use neuroprocessors for image processing, as reported by Ji-Chien Lee, Bing J. Sheu and Rama Chellappa, using an interesting analog systolic architecture.

For ASIC approaches, J. van Meerbergen, P. Lippens, B. McSweeney, W. Verhaegh, A. van der Werf and A. van Zanten show a design method for ASIC, where the memory access bottleneck for locally arranged memories is relaxed. Toon Gijbels, Francky Catthoor, Luc Van Eycken, Andre Oosterlinck and Hugo De Man also describe the ASIC approach to relax memory access bottleneck using an RBN-coder example. C.V. Reventlow, M. Talmi, S. Wolf, M. Ernst and K. Müller design a high speed motion estimation chip set for HDTV signal process applications. Ravi Kolagotla, Shu-sun Yu and Joseph JáJá describe a Vector Quantization VLSI design method using a systolic approach.

The final class of articles concern algorithm mapping to specific processors. Robert L. Stevenson, George B. Adams, III, Leah H. Jamieson and Edward J. Delp evaluate the performance of an inverse operator approximation on a parallel machine. Frederico Buchholz Maciel, Yoshikazu Miyanaga and Koji Tochinai indicate an approach to lower the iteration bound in a DSP program.

We would like to express our thanks to all the contributing authors, the reviewers and the Editors-in-Chief for completing this special issue. Thanks also are due to Judy Kemp, Kluwer Academic Publishers, for her kind support.

Takao Nishitani
Peng H. Ang
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VLSI in Picture Coding

Invited Paper

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Abstract. Recent LSI technology development for motion video coding is described briefly. The standard coding algorithms discussed recently are based on interframe coding with motion compensation and DCT (Discrete Cosine Transform). LSIs for realizing the signal processing functions are shown as functions of integration scale and chip area. Custom design LSI chips for the interframe encoder and decoder, meeting the H.261 and MPEG standards, are shown. Also, progress of programmable video signal processors (VSP) are overviewed.

1. Introduction

Video signal interframe coding is becoming a key to not only digital transmission but also to video storage (figure 1) [1]–[5]. Digital data compression coding aimed first at long distance video signal transmission for teleconference and broadcast program transmission over satellite and optical fiber cable link [6], [7]. The technology is then being applied to motion video signal storage in package media such as optical disk and magnetic tape. Also, it is to be introduced into digital broadcasting through satellite and terrestrial radio channels to improve radio frequency spectrum use efficiency [8].

With the rapid progress, the standardization is discussed in international organizations, such as CCITT, CCIR, and ISO MPEG. As the application field expands, a variety of video signal formats are defined as shown in table 1, from Quarter-CIF to HDTV [9]–[12]. It is noted that the sample rates for video signal range from several hundred kHz to several tens of MHz. Video signal data compression coding technologies have been studied for more than twenty years, and are standardized [12]–[14], as shown in figure 2. The coding algorithms recently adopted as the standards are based on an interframe predictive coding with motion compensation (MC) and Discrete Cosine Transform (DCT). To realize the complex processing with a reasonable hardware size and cost, LSI chips for the codec have been developed.

This article briefly describes recent development in LSI technology, functional devices for picture coding, codec LSIs and video signal processors.

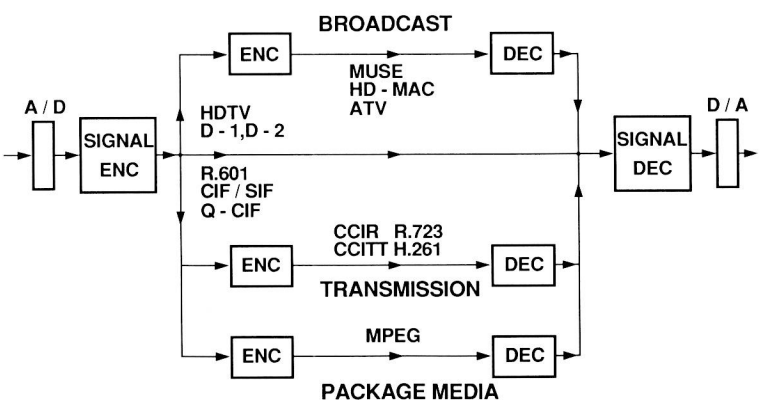

Fig. 1. Digital encoding in television systems.

Table 1. The standard video signal formats.

Format		Q-CIF[12]	CIF[12]	SIF (NTSC)[14]	R.601[9]	HDTV (E)[11]	HDTV (J)[10]
No. of Pel H × V	Y	176 × 144	352 × 288	352 × 240	720 × 483	1920 × 1152	1920 × 1035
	C	88 × 72	176 × 144	176 × 120	360 × 483	960 × 1152	960 × 1035
Progressive or Interlace		1:1	1:1	1:1	2:1	1:1 2:1	2:1
Frame Rate		29.97	29.97	29.97	29.97	25	30
		CCITT H.261	CCITT H.261	ISO/MPEG	CCIR Rec.601	CCIR Rep.801-3	CCIR Rec.709

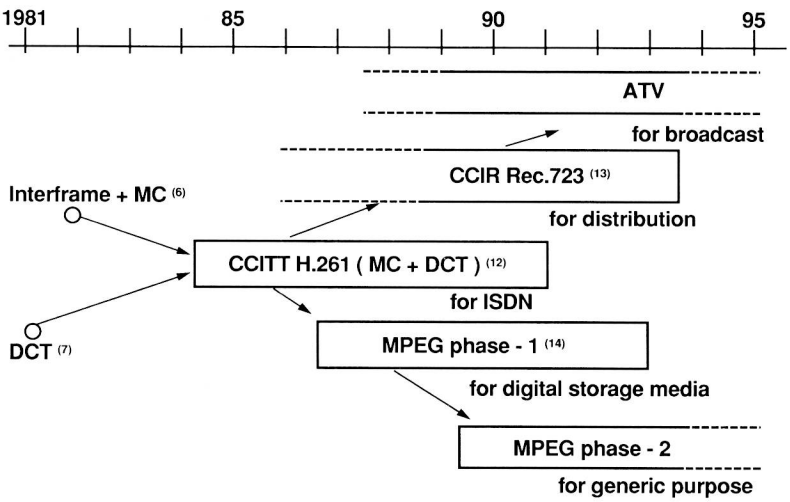

Fig. 2. Development of video signal coding algorithm.

2. LSI Technology Development

The integration scale is increasing at a well-known DRAM capacity increase rate of 4 times every 3 years, and will continue to reach a Gbit chip, or a level of SLSI (Super Large Scale Integration), in the 21st century. Figure 3 shows the decrease in device design rule and the increase in integration scale. A half micron device has been used for 16 Mb DRAM and made it possible to integrate a logic circuit with more than one million transistors on a chip. The operating speed of CMOS became sufficiently high to handle video signal processing.

For video signal processing, low power consumption as well as high speed operation are important factors to cope with the very large amount of computations required. Since the power consumption of CMOS circuit increases in proportion to operating frequency, it limits the integration scale as the operating frequency increases, even though CMOS circuits operate at a very high frequency. Therefore, custom design chips are mostly used for video signal processing in order to optimize the performance. On the other hand, as the integration scale increases, a gate array becomes a useful device to easily realize image processing logic circuit. CMOS gate arrays having 200K gates with a few hundreds pico second gate delay are commercially available. In addition, various macro standard cells, such as RAM, register file, arithmetic unit etc., are provided. Using these LSI technologies, various video signal processing LSIs have been developed.

Figure 4 shows typical video signal processing LSIs as functions of integration scale and chip area. With the CMOS integration scale increase, the function of a chip has been expanded from a single function to more complex functions. For example, in the mid 1980s, a chip could include such functions as digital filter, DCT, variable length coder, and so on. Now, a more complex signal processing for video codec, such as JPEG, H.261, and MPEG, is realized.

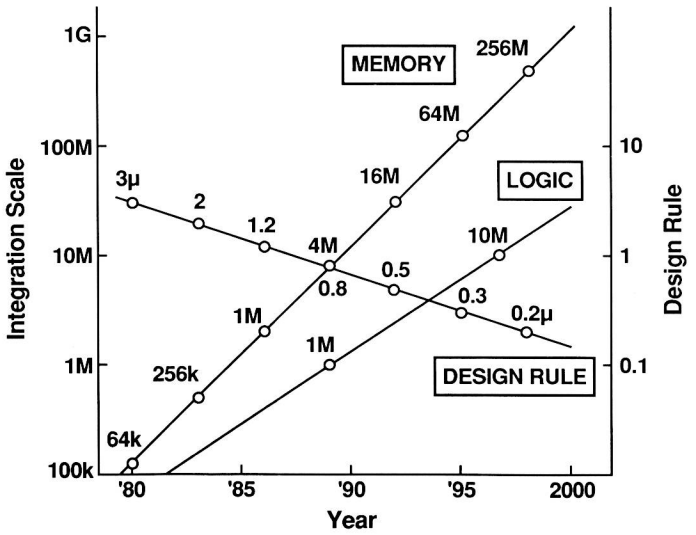

Fig. 3. LSI technology progress.

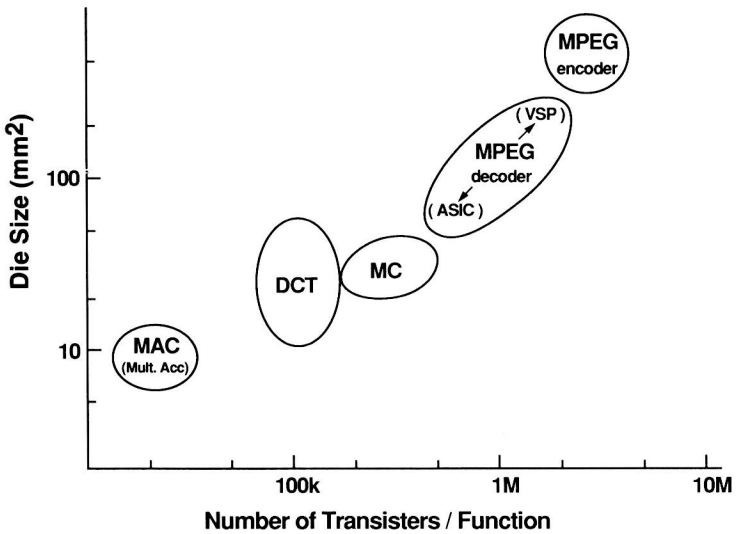

Fig. 4. DSP LSIs as functions of integration scale and die area.

3. Signal Processing LSI for Data Compression Coding

Motion compensation is a key function for improving the data compression ratio in interframe coding, and is adopted in most of the standard coding algorithms. For the motion estimation, a block matching algorithm is generally used to determine the best matched picture block in the previous frame picture in real time. For a standard television signal, a large amount of computation, on the GOPS (Giga Operation Per Second) order, must be done.

A multi-stage method, or tree search, could reduce the amount of computation by an order of magnitude compared with a full search method. The algorithm could be realized with a parallel processing circuit composed of standard LSIs [6]. Also, the motion compensated interframe coding algorithm could be implemented on a programmable video signal processor.

Although the full search method needs a larger amount of computation, the LSI integration scale increase made it easier to implement the full search algorithm by employing a systematic arrangement of processor elements. Several kinds of full search architecture

Table 2. Motion estimation LSIs.

Name	Block Match Algorithm	Device Technology	Clock MHz	Codec Chip Set
STV3220 SGS Thomson	Full Search	1.2 μm CMOS	18	H.261
L64720 LSI Logic	Full Search	CMOS	40	H.261
X64100 GCT[17]	Full Search	1.0 μm CMOS	30	H.261
COB-V NEC[30]	Two Step Search	0.8 μm CMOS	36	MPEG

have been proposed. An example is a parallel processor with 16 processor elements operating at about 20 MHz rate, corresponding to about 1.2 GOPS, providing a real time operation for CIF video signals [16]. The processors can be connected in cascade to expand the processing capability for higher resolution video signals. Typical examples of motion estimation LSIs are shown in table 2.

The motion video coding is expected also in the field of digital storage and playback applications [3]. Data compression algorithm standardization is being discussed in the ISO/IEC Motion Picture Expert Group (MPEG) [14]. For the purpose, interactivity with the stored data is mandatory. This necessitates additional features in the coding algorithm. Intraframe-coded picture is inserted in every several frames for fast start up and fast refresh of the bit error effect. Motion compensated interframe prediction is made from the frame either before or after the one to be predicted. These factors improve the coding performance, but increase coding process complexity.

Realization of a single board encoder/decoder has strongly been expected, since the codec cost should be reduced greatly for such applications as video telephone and multi-media PC or WS. For playback (read only memory) use, only the decoder function is implemented, while telecommunication use needs both encoder and decoder. The H.261 codec chip sets are listed in table 2 [17]. Table 3 shows a motion video MPEG decoder chip or chip set [18], [19]. The chip or chip set can handle a CIF/SIF video signal or 288 × 352/240 × 352 picture elements per frame with a frame rate of 30.

HDTV signal processing requires a very high speed operation, 50 MHz or higher. Although CMOS device can operate at the speed, the integration scale is limited due to power consumption increase with the operation

Table 3. MEPG (H.261) decoder LSIs.

Name	Number of Chip	External Memory	Number of Transistors	Clock MHz
CL450 C-Cube	1	4 Mb	300 k	40
MCD1450 Motorola	1	4 Mb	100 k	36
VP, VC IIT	2	4 MB	300 k	33
STI3240 SGS Thomson	2	8 Mb	220 k	40
AVP1400D ATT	1	8 MB	1 M	40
μpD72680 μpD72681 NEC[30]	2	8 Mb	1.25 M	27

speed increase. For example, a 2D-DCT chip has been developed, which operates at an HDTV sampling rate [15]. The motion estimation needs plural chips. The MUSE decoder (MUSE is a bandwidth compression for HDTV broadcast by DBS in Japan), which is basically composed of 2D (two dimensional) and 3D digital filtering for interpolation of sub-sampled pels, was implemented with 10–15 specially designed LSIs in a second generation chip set [20]. HDTV field memory can be a single chip with 8 Mbits DRAM.

4. Video Signal Processor

The programmable DSP (Digital Signal Processor) is, in general, very useful for early development of a signal processing algorithm, because of easy implementation by software program. DSP became a powerful means for voice/sound signal processing in the early 1980s, since it permitted carrying out 100–500 instructions in the signal sampling interval necessary to implement various signal processing fucntions. For video DSP, video signal processors (VSP) were developed [21], [22], and have been used for codec implementation. One drawback to the DSP approach in video signal processing is low processing capability, due to the high signal sampling rate, compared to that for the audio signal case. Therefore, a parallel operation with plural VSPs is needed [23]. For only a small sized picture, like Q-CIF with a lower frame rate, however, the full coding functions can be implemented on a single VSP [24].

One way to increase computation power is to increase device operating speed. As the Bi-CMOS technology

Table 4. Programmable video signal processors, VSP.

Name	Device Technology	Number of Transistors	Clock MHz	MOPS	Year
VISP[21] NEC	1.2 μm COMS	220 k	40	40	1989
DISP[22] Mitsubishi	1 COMS	538 k	20	20	1989
S-VSP[26] NEC	0.8 BiCMOS	1.1 M	250	500	1991
IDSP[23] NTT	0.8 BiCMOS	910 k	25	300	1991
MN195901[27] Matushita	0.8 BiCMOS	930 k	60	2000	1992

progresses, the VSP operation speed can be made as high as 200–300 MHz [25]. This means that the high speed VSP reaches a level corresponding to the first DSP for voice/sound in the early 1980s. The other way to increase the processing power is a multi-processor architecture having plural processing units to operate in parallel [26]. The parallel computation on vector/matrix operation is effective for motion estimation and DCT coding. Further, in order to increase the degree of parallel operation, a special function such as DCT is put into a VSP chip [27]. By introducing the parallelization of computation, as well as the high speed operation, VSP performance will be able to be increased by two orders of magnitude, high enough to handle standard television signals. Although a codec for standardized algorithm is realized with a custom design chip, the general purpose VSP may play an important role in developing new signal processing functions.

5. Future of Video Signal Processing

In the future, much more sophisticated signal processing will become necessary. For example, much research effort is being made for next generation coding algorithms, such as model based coding and intelligent coding [28], [29], which are expected to greatly reduce the data rate compared with the present standard algorithms. In these cases, a key technology is to derive a solid model of an object from two dimensional pictures taken by plural cameras. The algorithm will need much computation, far more than that required for present coding. Another example is stereo image transmission, which is expected as a means to provide more real image presentation. Also, in this case, the derivation of a solid image model is essential. The amount of information to be transmitted increases greatly, compared with conventional video signal, data compression being indispensable. These processings will require a vast amount of computation, which will be implemented on the SLSI chips.

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Single-Chip Image Sensors With a Digital Processor Array

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Abstract. The architectures, implementation and applications of two smart sensors, LAPP and PASIC, are described. The basic idea of these two designs is to integrate an image sensor array with a digital processor array in a single chip. The integrated camera-and-processor eliminates the bottleneck of sequential image read-out that characterizes conventional systems. They provide fast, compact and economic solutions for tasks such as industrial inspection, optical character recognition and robot vision.

1. Introduction

Embedding of parallel processors in a sensing chip, a smart vision sensor, is an emerging area of image sensor development. Smart sensors will play a significant role in industrial applications. However, commercially available image sensors today are developed mainly for television. Such sensors have excellent sensitivity, high resolution, can handle colors and have excellent reliability. Their pixel read-out architecture, fixed frame rate and fixed resolution have a number of drawbacks for many industrial applications. The *pixel-by-pixel* architecture limits the speed and flexible use of the sensor information.

High speed image processing can be achieved by line-by-line or frame-by-frame parallel processing. A single chip solution is necessary, otherwise a large number of pads will be needed in a line-by-line or *frame-by-frame* parallel image processor architecture. It is therefore desirable to incorporate the sensor array and the processor array on a single chip. This will provide a mechanism to concurrently perform computations previously intractable in real-time. The continuous progress of VLSI technology has provided this opportunity.

Some excellent work on photo-sensor arrays with analog processing inspired by biological retinas has been performed by Carver Mead [1]. The basic idea is to include a simple and dedicated analog signal processor for each sensor element in a single chip. This frame-by-frame analog signal processing provides very high speed. Yang and Chiang have recently designed a CCD image sensor array integrated with an linear array of CCD analog processors to perform a simple edge detection algorithm line-by-line in real time [2]. By utilizing the ability of CCD technology that can sum and split charge packages, parallel convolutions with fixed coefficients are realized. However, these analog implementations are too specialized and do not have the flexibility to be tailored for different applications.

An alternative approach is to integrate a sensor array with a programmable digital processor array on a single chip. An experimental chip has been developed using 3-D technology [3]. The device consists of a 5-by-5 photo sensor array, a 5-by-5 2-bit CMOS A/D converter array, a 2-bit ALU array and shift registers arranged in a 3-layer structure. The size of a pixel is 1.05×1.05 mm^2. Signals from the photo diodes are transferred to the 2-bit A/D converters. The quantized digital data is then transferred to the third layer, the ALUs. Finally, the processed signals are read out with shift registers. The image sensing, quantization and data processing of all pixels are operated simultaneously frame-by-frame. This frame-by-frame architecture allows extremely high speed image processing. However, the low area resolution, the low signal amplitude resolution and the very high I/O bandwidth demands in this design are severly limiting the applications.

This article will describe the architecture, implementations and applications of two smart sensors, LAPP and PASIC. They provide fast, compact and economic solutions to tasks such as industrial inspection, optical character recognition and robot vision. Section

2 will describe the LAPP system which is designed for fast binary image processing. A smart sensor, PASIC, whose architecture is an expanded version of LAPP to an enhanced bit-serial processor array with a resolution programmable A/D converter array, is described in Section 3. Sections 4 and 5 discuss their similarities and differences. Finally, further development and trends will be discussed in Section 6.

2. LAPP — Linear Array Picture Processor

The first attempt of integrating an image sensor array and a processor array on a single chip was made several years ago at Linköping University, LAPP, [4], [5]. Figure 1 shows the photograph of the LAPP1100, which is a commercial version and having 128 photo sensor elements, 128 threshold units for digitization and a 128 bit-serial processor in a single chip. The chip size is 5×7 mm^2 using a 3μm CMOS technology.

2.1. LAPP Architecture

The block diagram of LAPP is shown in figure 2. The linear photo diode array (PD) uses threshold circuitry to communicate image information to a 128 bit internal bus. The register array (R0–R13) stores images and intermediate results. The computing units GLU, NLU, PLU perform the image operations. Results are passed on to the accumulator. From there the result is either stored in a register, or used as the second operand in two-operand instructions.

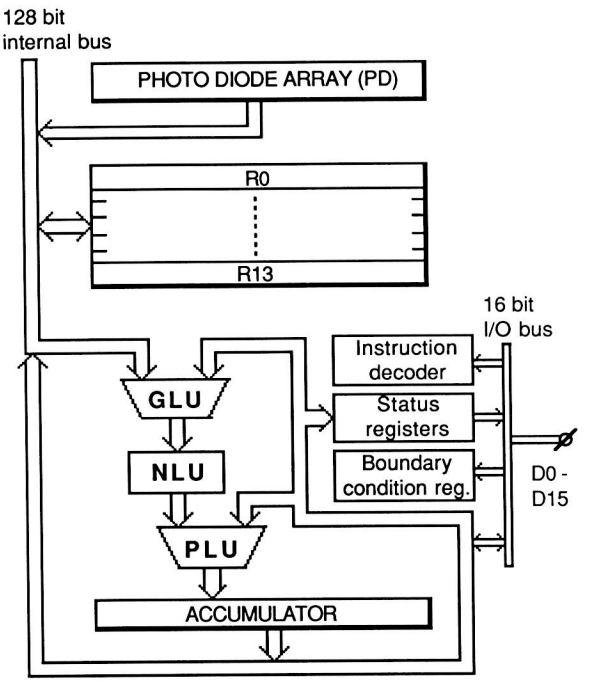

Fig. 2. The block diagram of the LAPP.

2.1.1. Photo-Diode and Comparator Array (PD). The photosensitive diode array consists of a linear set of diodes, pre-charge transistors and comparators as shown in figure 3. The active surface of each of the diodes is 35×35 μm^2 and the space between them is 50μm.

The diode is first reversely biased by pulsing the pre-charge transistor. The charged diode will then discharge

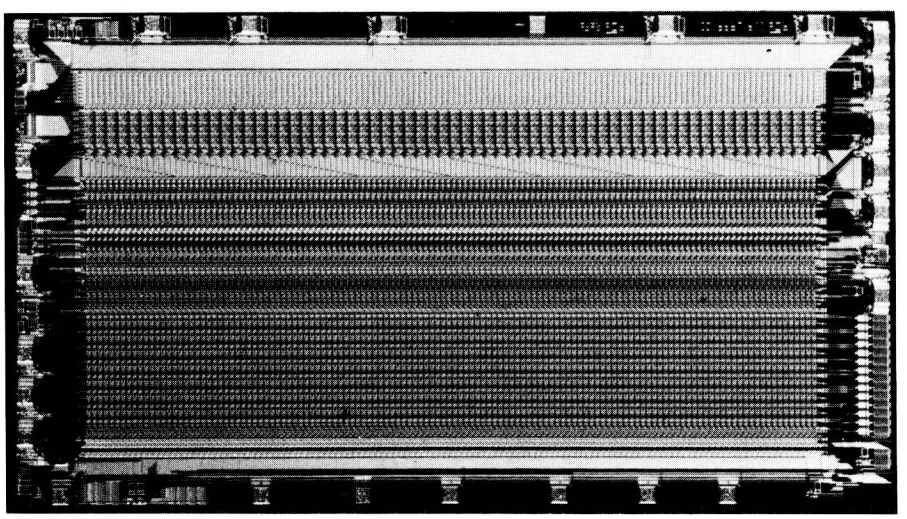

Fig. 1. LAPP chip photo-micrograph.

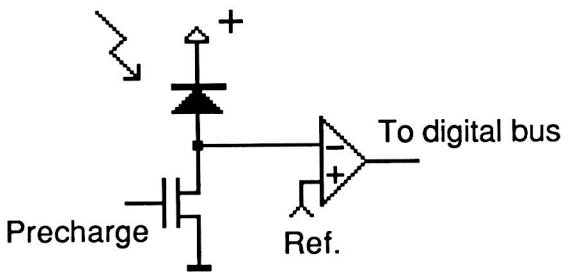

Fig. 3. Photo-diode and threshold unit.

proportionally to the amount of light falling onto its surface. The diode voltage is compared with an analog reference signal which is common to all the picture points. This results in a thresholded image line. Gray scale values of an image line can be obtained by changing the reference level and/or the exposure time.

2.1.2. Point Logical Unit (PLU) and Neighborhood Logical Unit (NLU). The PLU performs basic point operations like AND, OR and XOR. Its operands are the current value of the accumulator and the output from the NLU. The NLU is a general 3-element template matcher. Its operation is defined by a condition code (C_{-1}, C_0, C_{+1}) such that a new pixel state is related to the old state of the pixel itself and its neighbors.

$$q_i \Leftarrow (C_{-1} \oplus q_{i-1})' \cdot (C_0 \oplus q_i)' \cdot (C_{+1} \oplus q_{i+1})'$$

C takes the values 0, 1 and x (don't care), the last case meaning that the corresponding factor will be discarded. The operation is performed simultaneously over the entire set of pixels.

2.1.3. Global Processing Unit (GLU). GLU makes possible a set of operations which traditionally requires recursive processing. The most prominent feature of the GLU is that it is able to "fill" holes in one of its operands. A hole is pointed to by a mark bit in the second operand. Leftmost and rightmost mark bits can be controlled externally giving the special cases of "left scan" and "right scan" operations in one clock cycle.

The GLU is also useful in line-to-line processing by its ability to extract those objects in the first operand that are connected to object in the second operand. This is shown in figure 4 where an input register *X* contains three objects (marked in black). The leftmost two objects are *vertically connected* to objects stored in the accumulator (shown at the top of the figure). This means that there is an overlap of at least one black pixel

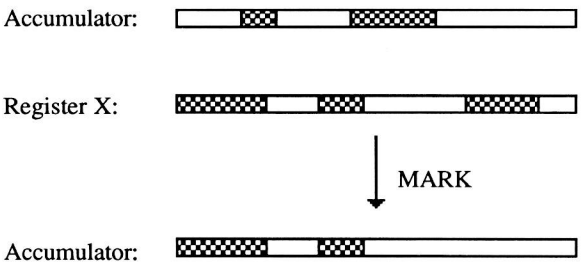

Fig. 4. Example of global instruction.

for each of these two objects. The third object does not have such a connection. When performing the MARK operation the two leftmost objects will be copied into the accumulator as a result of the operation.

2.2. *LAPP Instruction Set*

The 128-bit processor enables simultaneous processing of all pixels in an entire 128 binary-pixel line. The detector is composed of a 128-bit linear photo diode array whose brightness levels are read out once at a time and loaded into the available register positions. Two-dimensional picture processing is possible through internal image registers that store previously input lines. This procedure assumes that either the circuit device or the object moves perpendicular to the line to be processed.

The instructions are executed in a single clock cycle (1 μs) like in a Reduced Instruction Set Computer (RISC). All pixels in an addressed register are processed simultaneously. This characteristic is often referred to as Single Instruction, Multiple Data stream (SIMD) architecture. LAPP can be viewed as an array of bit-serial SIMD machines with its 128 parallel subprocessors. From programming point of view, it is easier to consider the system as a 128-bit processor with the traditional computer architecture as shown in figure 2.

Table 1 summarizes the basic instructions. As shown in figure 2, the three units GLU, NLU and PLU operate in tandem. In each instruction cycle, a sub-operation from each class can be executed in a named order. All together the total number of instructions will be 1734 (not counting the register variations). However, a programmer does not have to keep track of that many combinations since they are created from the few basic types, shown in table 1.

Table 1. LAPP instruction set.

PLU instructions	
LD	load acc with NLU output
AND	bitwise logical AND
OR	bitwise logical OR
XOR	bitwise logical XOR
LDI	invert NLU before LD
ANDI	invert NLU before AND
ORI	invert NLU before OR
XORI	invert NLU before XOR
NLU instructions	
DOT	detect isolated 1's
HOLE	detect isolated 0's
INV	invert
LEDGE	detect left edges
REDGE	detect right edges
LSHIFT	shift left
RSHIFT	shift right
GLU instructions	
MARK	mark connected objects
LMARK	mark left border object
RMARK	mark right border object
FILL	mark holes
LFILL	fill right form leftmost object
RFILL	fill right form leftmost object
LRFILL	fill from left and right

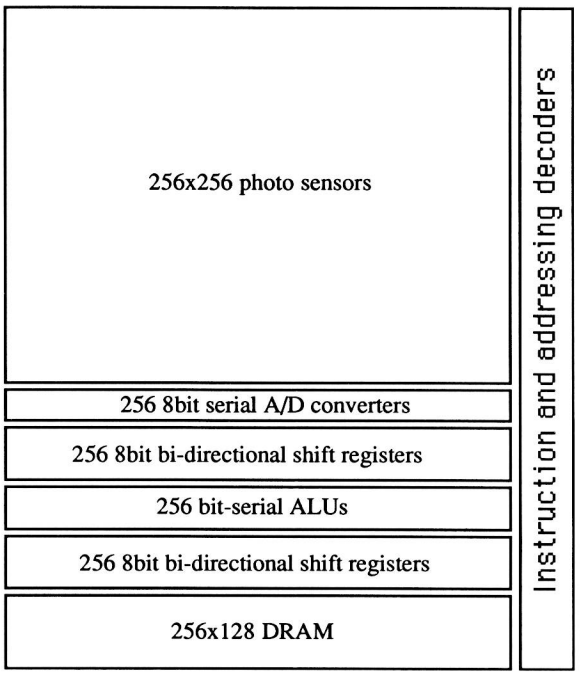

Fig. 5. PASIC architecture and floorplan.

3. PASIC: A Processor—A/D Converter—Sensor Integrated Circuit

3.1. PASIC Organization

PASIC can be considered as a second generation of the LAPP concept [6], [7]. The sensor array is extended to two-dimensions, the A/D converter is extended from 1 bit to 8 bit, the on-chip memory has been extended from 14 bits to 128 bits for each processor element and the ALU has been extended to a fully general purpose ALU. The current version of PASIC contains 256 bit-serial processors with a 256 × 128 bit memory, 256 8-bit A/D converters and a 256 × 256 photo sensor array as shown in figure 5. Two 256 × 8 bi-directional shift registers are used for communication between processor elements and I/O. A memory-bus organized architecture has been used, which has been proven as an efficient VLSI architecture for a SIMD bit-serial processor array. "GAPP Exercises" [8] has provided the background for the PASIC algorithm and software developments.

The 2-D sensor array is arranged in columns. Each column of sensors has an analog read-out bus. Thus, one row of sensors at a time is connected to A/D converter array. Each column of sensors is equipped with one A/D converter and one processor which is composed of two 8-bit shift registers, a bit-serial ALU and a 128-bit RAM. The two 8-bit shift registers can be operated independently in five modes, read, write, latch, shift right and shift left. The A/D converter, the shift registers, the ALU and the memory communicate over a single-bit bus. The two parallel shift registers provide the horizontal communication link between adjacent processors. Also, they serve as the input and output of the chip.

3.1.1. A/D Converter Array. In a conventional camera system, a single video rate A/D converter has to handle an entire frame of an image. In PASIC, there is one A/D converter for each column of sensors. The speed requirement on these A/D converters is therefore reduced to a "line-rate", which is two orders of magnitude lower than the video pixel rate. A serial ramp-type A/D converter can be used. The parallel A/D converter array consists of one common counter, one common ramp generator, 128 comparators and 128 8-bit RAM cells, as shown in figure 6.

3.1.2. Processor Array. Because of the large number of processor elements (PEs) involved, each PE has to be extremely simple. In particular, one PE has to be squeezed into the pitch of the photo sensor element