Analog Electronics with Op Amps

A Source Book of Practical Circuits

A.J. Peyton and V. Walsh

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This book presents a collection of analog electronic circuits based on the op amp, supported by a wealth of practical and technical detail which will enable the reader speedily to select, build and test a desired circuit.

The book is primarily intended to be a practical reference volume rather than a teaching text. Both students and professional engineers will discover in its pages an extensive and invaluable source of functional and established analog circuits, from integrators and differentiators to logarithmic amplifiers; from instrumentation amplifiers to filters. The circuits are conveniently grouped according to function, and the approach followed is to build up slowly from the basic textbook examples towards a series of practical, workable circuits.

Students who need to build and test particular types of analog circuitry as part of an assignment or project based activities will find this book invaluable. Professional engineers will also find the book useful for design and development work. The coverage is extensive and up-to-date, and provides a wealth of expert, technical advice on the selected circuits.

Analog Electronics with Op Amps

Preface

In recent years we have seen the emergence of a new subject in electronics, that of digital signal processing (DSP). In DSP, which is based on the computational power of the microprocessor, many new application areas have been pioneered and at the same time old ones have been given a fresh impetus. Results have been produced, through various software techniques, which would previously have been possible, if at all, only through the prohibitively extensive use of hardware. Over this same period, a new technology has also come to maturity centred around the creation of monolithic integrated circuits which combine both analog and digital operations on a single silicon substrate. These hybrid ics and powerful DSP systems have produced enormous benefits for the design engineer in terms of reduced costs, increased performance and greater flexibility. Analog electronics, however, tends to have been overshadowed, based as it is on the more mature technology of the op amp. Yet a sound grasp of analog electronics is probably more important now than ever since DSP has opened up so many new applications, all of which require an analog front-end for their operation. There will also continue to be a need for prototyping new designs in hardware in the early stages of development work, whether this prototyping is done in the industrial laboratory by the experienced design engineer or in the college or university laboratory by students who are just setting out on the engineering path. Useful as software simulations of analog circuits are to the engineer and student, there is still no substitute for the 'real-world' experience provided by a hands-on approach.

We are conscious, owing to limitations of space, of the absence of conversion electronics in these pages, especially in the use of digital to analog converters and analog to digital converters. Apart from this omission, readers will find that many practical circuits from analog electronics are usefully described and outlined. However, this book is not intended to be a textbook in analog electronics, nor is it an introduction to the fundamentals of the op amp. Many other works carry out this role perfectly well. Instead, it is offered as a source of practical circuits in analog electronics so that the reader can readily and speedily obtain information and advice on the particular task which needs to be carried out using that work-horse of analog electronics, the op amp. Using this superbly flexible building block, and a suitable addition of resistors, capacitors, diodes and discrete transistors, a remarkable range of operations can be carried out. If this volume is the first book which readers consult when they begin their task of designing, building and testing a particular analog circuit, then our work will have succeeded.

I wish to thank my wife, Denise, for her constant help and encouragement, and my daughters Lucy and Anna. With thanks also to my parents. [AP]

I wish to thank my wife Mary and my children, Katherine, Sean, Nicola and Daniel for their tolerance and support during the writing of this manuscript. [VW]

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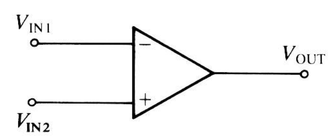
1

Instrumentation amplifiers

An instrumentation amplifier is a device with two balanced differential inputs. The amplifier is configured so that it accurately amplifies the differences between the voltages applied to its two input terminals ($V_{IN2} - V_{IN1}$) without being affected by the common mode voltage on both the inputs as shown here. For many typical instrumentation amplifier ics the voltage gain A_V is set between 1 and 1000.



$$V_{OUT} = A_v(V_{IN1} - V_{IN2})$$

Engineers are always contrasting real world devices with fictional devices, this is a useful approach for providing a 'feel' for the targets being aimed at. We may not hit dead centre but at least we will have a good idea of where the shots are landing. So, in the ideal case, an instrumentation amplifier will have the following characteristics amongst others: a constant and perfectly linear gain independent of time, frequency, load, temperature or humidity; an infinite common mode rejection ratio and power supply rejection ratio; zero input and output offsets and offset drifts and zero output impedance for maximum signal delivered to the load from the amplifier. You will usually find an instrumentation amplifier in the first stage of a measurement or instrumentation system where accurate measurement is the fundamental requirement for the application. In many cases, the input signal to an instrumentation amplifier will be derived from a bridge network or some form of transducer which has converted a physically varying quantity into an analog electrical signal. The main problems for the design engineer, in amplifying this signal for further processing by later stages, are concerned with restricting unwanted noise and controlling movements in the gain of the amplifier due to environmental changes.

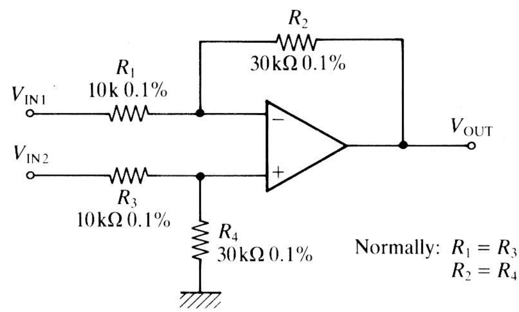


Fig. 1.1. Single op amp instrumentation amplifier circuit.

1.1 Single op amp instrumentation amplifiers

The configuration shown in Fig. 1.1 is the simplest and lowest-cost option for an instrumentation amplifier. R_3 and R_4 act as a potential divider for the non-inverting input of the op amp. The inverting input of the op amp is forced to the same voltage as the non-inverting input due to feedback through R_1 and R_2 and the very large gain of the op amp. The ratio R_2/R_1 sets the gain of the amplifier. When $R_1/R_2 = R_3/R_4$ the differential voltage gain will be much greater than the common mode voltage gain and the common mode rejection ratio (CMRR) will be maximized. For the resistor values shown here, you will get a differential gain of $\times 3$ and a CMRR of 1000, i.e. 60 dB.

Differential gain $= A_D = V_{OUT}/(V_{IN2} - V_{IN1}) = \dfrac{R_2}{R_1} \cdot \dfrac{1}{\left(1 + \dfrac{R_2}{R_1} \cdot \dfrac{1}{A_V}\right)}$

(A_V is the op amp gain)

$$\simeq R_2/R_1 \ (A_V \text{ very large})$$

Common mode gain $= A_{CM1} = \dfrac{R_1R_4 - R_2R_3}{R_1(R_3 + R_4)}$

(due to resistor mismatch)

Common mode gain $= A_{CM2} = \dfrac{R_2}{R_1 \cdot \text{CMRR}}$

(due to finite CMRR of op amp.)
(Note that CMRR is expressed as a ratio and not in dB)

$$\text{Common mode rejection ratio} = \text{CMRR} = \frac{A_D}{A_{CM1} + A_{CM2}}$$

Differential input resistance $= R_1 + R_3$

Common mode input resistance $= (R_1 + R_2)//(R_3 + R_4)$

(assuming CMRR $= \infty$)

Output offset voltage (worse case) $= \left(1 + \frac{R_2}{R_1}\right)V_{IO} + I_{OS}R_2$ if $R_1 = R_3$ and $R_1 = R_4$

where

V_{IO} = input offset voltage of op amp

I_{OS} = input offset bias current.

The circuit in Fig. 1.1 has a low input impedance (around 20 kΩ in this example) and is really only of use in applications which have a low source impedance. Driving the circuit from a high impedance signal source will result in attenuation of the input signal due to loading and a poor common mode performance. Increasing the values of the input resistors (R_1, R_3) will increase the input resistance but at the cost of increasing offset drift due to finite input offset current, reduction of the bandwidth due to stray capacitance and an increase in noise. The values of R_1 and R_3 need to be selected for a trade-off between input resistance and input offset current, input noise current and bandwidth.

A high CMRR is achieved by making $R_1/R_2 = R_3/R_4$ but do not forget that R_1 and R_3 must include the inverting and non-inverting input source impedances otherwise gain errors and common mode errors will be introduced. Similarly, changes in resistor values can cause problems: high-precision, high-quality resistors may be needed.

The bandwidth of this amplifier is going to be limited by either the finite bandwidth of the op amp or by stray capacitances. If the bandwidth is limited by the op amp, assuming that the op amp is fully compensated, then the bandwidth will be approximately $f_A \cdot R_1/(R_1 + R_2)$ where f_A is the gain–bandwidth product (equal to the unity gain crossover frequency for a fully compensated op amp) of the op amp. If the bandwidth is limited by stray capacitances, in particular the strays across R_2 and R_4, and assuming that $R_1 = R_3$, $R_2 = R_4$, then the 3 dB frequency is given approximately by $1/2\pi R_2 C_{STR}$ where C_{STR} is the capacitance across R_2 which is typically 10 pF or less (e.g. if $R_2 = 1$ MΩ, $C_{STR} = 10$ pF, then the bandwidth will be limited by this effect to only 16 kHz). So, if you want a wide bandwidth you must use a fast op amp and resistor values must be kept low.

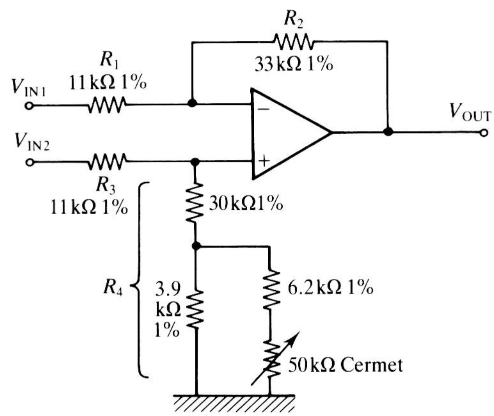


Fig. 1.2. Using a trimmer to maximize CMRR.

Note that the CMRR of the differential amplifier becomes very poor at higher frequencies due to the limitations of the op amp and mismatch of the impedance of R_1 and R_2, R_3 and R_4. In one-off applications, you can use a trimming pot to maximize CMRR. A very high CMRR at dc is possible by trimming since the CMRR of the op amp is cancelled by the common mode contribution of the resistor mismatch. The trimmed value will vary, however, due to drift and ageing of the circuit. The configuration shown in Fig. 1.2. allows you to use a higher value trimmer since low value trimmers tend to be less stable.

A good practice in instrumentation amplifier construction is to lay out the discrete components in a mirror-image fashion onto the board so that any stray capacitances are operating equally on both inputs, this practice is effective in maximizing the common mode frequency response. In some cases you may want to limit the bandwidth of the amplifier; to do this, identical capacitors must be added across both R_2 and R_4; be careful with the tolerances (use 1% if possible) otherwise the amplifier may have a poor high frequency performance.

If you want to increase the gain of the amplifier, the circuit in Fig. 1.3 could be used. This approach achieves high gains without the use of high value resistors. The buffer shown in this circuit will not be needed if R_5 and R_6 are sufficiently low in value compared to R_2 so that loading does not take place.

An increase in amplifier gain can also be obtained by using a T-network for the feedback resistors as shown in Fig. 1.4. This circuit allows you continuously to vary the gain without significantly affecting the CMRR of the circuit. This configuration also allows higher-value resistors to be used in other parts of the circuit to increase input resistance. Notice that the gain is not a linear function of K and the circuit requires three pairs of matched resistors; the four R_2 resistors,

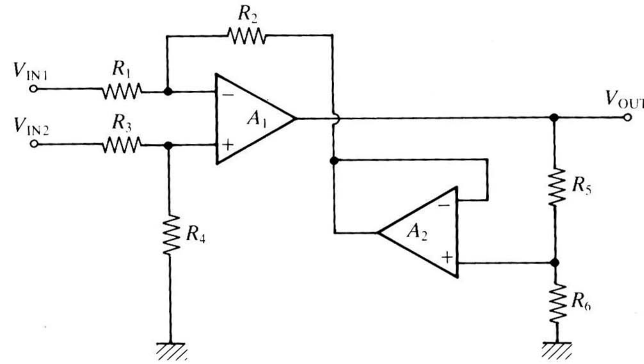


Fig. 1.3. Increasing amplifier gain without using high value resistors.

$$\text{Gain} = \left(1 + \frac{R_5}{R_6}\right)\frac{R_2}{R_1}$$

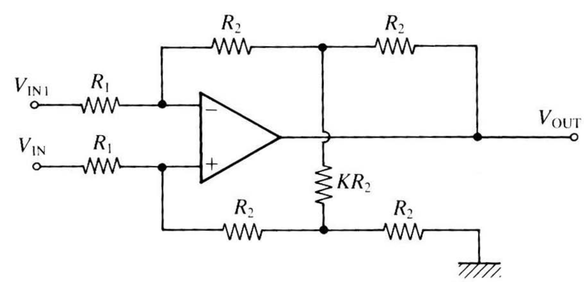


Fig. 1.4. Using a T-network to increase circuit gain.

$$\text{Gain} = \frac{2R_2}{R_1}\left(1 + \frac{1}{K}\right)$$

however, can be on the same package to increase temperature tracking.

One point to watch out for with higher gain (e.g. 1000 or more) differential amplifiers is the finite open loop gain of the op amp. If the open loop gain is not sufficiently high, an excessive differential gain error may result.

If you are expecting high common mode voltages beyond the supply rails, the circuit shown in Fig. 1.5 can be used. Note that A_2 nulls the common mode voltage at the input of A_1 through the action of R_5 and R_6. Since no common mode voltage is applied to either A_1 or A_2, this circuit gives good CMRR. The limits of the CMRR depend on how well R_1/R_5 can be matched to R_3/R_6. Usually $R_5 = R_6$, $R_7 = R_8$, $R_1 = R_3$ and $R_2 = R_4$.

Standard offset nulling techniques can be used for instrumentation amplifiers. The circuit shown in Fig. 1.6 is useful for instrumentation amplifiers since varying the reference level at the non-inverting input of the op amp offers quite effective offset nulling. This technique has the

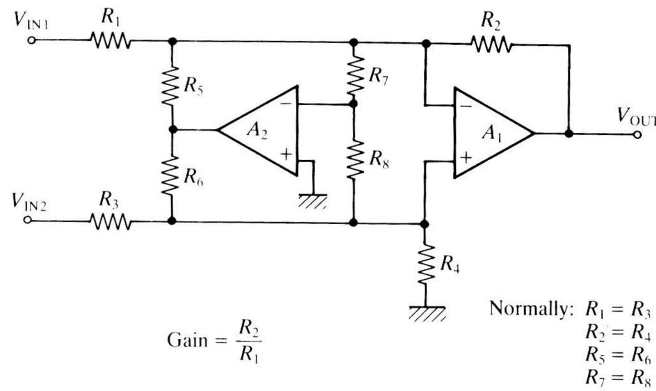


Fig. 1.5. High common mode voltage circuit.

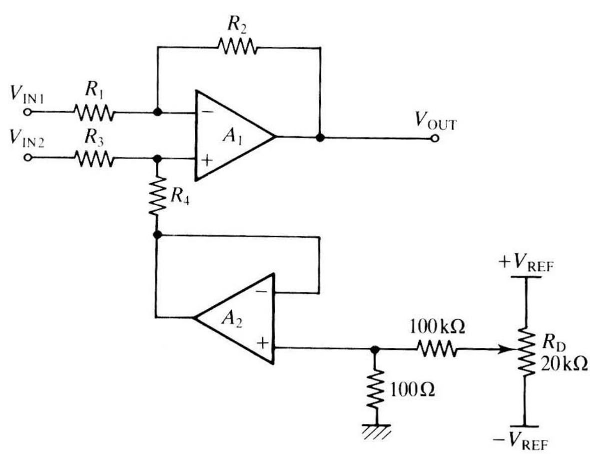


Fig. 1.6. Reference level nulling.

disadvantage of requiring a low output impedance reference, hence the use of a second op amp A_2. A lower value of divider R_D could be used, with A_2 omitted, but this may degrade the performance of the amplifier. Note that this circuit effectively nulls the offset voltage at the output. So, only small output voltage offsets well within the range of output swing of the op amp can be nulled.

1.2 Two op amp instrumentation amplifiers

In the configuration shown in Fig. 1.7 both op amps are connected together as non-inverting amplifiers where the first non-inverting amplifier (A_1) varies the reference level of the second, (A_2). The output of A_1 is fed to the inverting input so that A_1 amplifies the differential input signal ($V_{IN2} - V_{IN1}$). This circuit results in a much higher input impedance than is possible with the single op amp configuration.

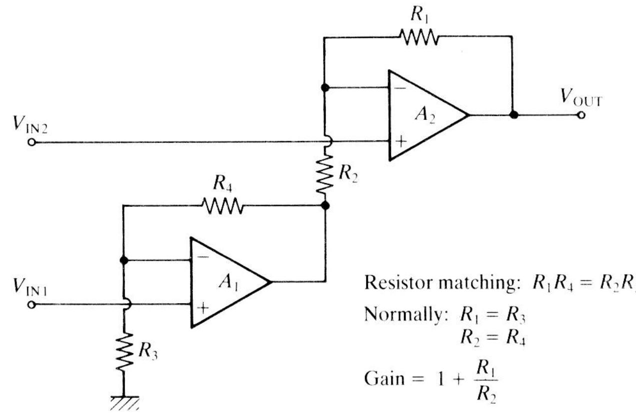


Fig. 1.7. Two op amp instrumentation amplifier circuit.

$$\text{Gain} = 1 + R_1/R_2$$

$$\text{Common mode gain} = (R_1R_4 - R_2R_3)/R_3R_2$$

$$= 1 - \frac{R_1}{R_2} \cdot \frac{R_4}{R_3}$$

$$\text{Therefore if } \frac{R_1}{R_2} = \frac{R_4}{R_3}, \quad \text{then the common mode gain} = 0$$

$$\text{Output offset} = 2(1 + R_1/R_2)V_{IO}$$

where

$$R_1/R_2 = R_3/R_4$$

and

$$V_{IO} = \text{input offset voltage of the op amp}$$

$$\begin{pmatrix}\text{Differential input impedance} \\ \text{Common mode input impedance}\end{pmatrix} \Rightarrow \begin{pmatrix}\text{dependent on the type} \\ \text{of op amp used in the circuit.}\end{pmatrix}$$

As before, the close matching of equal value resistors is essential for high common mode rejection.

Gain can be varied, if required, by adding an extra variable resistor as shown in Fig. 1.8. The gain in this circuit does not, however, vary linearly with R_3. Not shown on this circuit are the extra components needed to provide a path for input bias currents to flow (see later).

A further development of the previous configuration applies the input signal between the two inverting terminals of the op amp as shown in Fig. 1.9. Note, though, that this circuit has the disadvantage of a low input impedance (approximately equal to R_1); the gain, however, can be varied proportionally by R_2.