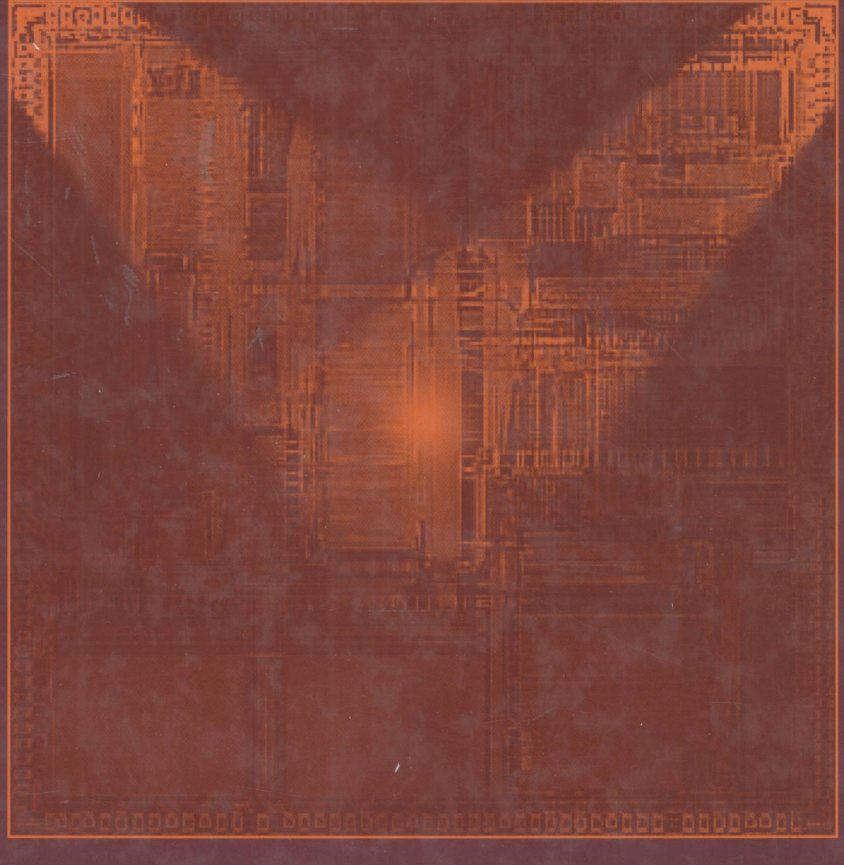
Signal Integrity Effects in Custom IC and ASIC Designs



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Foreword

From the Early Days of CMOS to Today

For the last two decades, digital designers have not been very concerned with Signal Integrity (SI) issues. While these issues always existed, they were either insignificant high-order effects or they were masked by conservative design rules and structures. Analog designers did concern themselves with some SI issues, such as substrate and power/ground noise, but integration of analog and complex digital design has been rarely done until recently. The SI issues, if there were any, were analog only issues. Now times have changed. As we move into ever-deeper submicron processes, all of those high-order SI effects are becoming significant. Digital designers can no longer ignore SI issues and expect to create complex, leading-edge designs that work. Analog designers cannot limit their SI analysis to the analog design; they now must be aware of the SI issues between the analog and digital sections of a design. Until EDA tools and systems of design can again successfully hide these new complexities of semiconductor design, it is an issue that must concern all digital and analog designers.

Much of the complacency of digital designers over the last two decades is a result of designing with CMOS logic, a low-power, high-gain, noise-insensitive, logic family. CMOS has been very forgiving. It continues to operate all the way down below 1 Volt. It has enjoyed large valid signal voltage ranges, allowing robust libraries of logic functions with a wide range of different thresholds. All of these features have kept CMOS the dominate digital semiconductor process for over an order of magnitude lithography reduction. Oddly enough, it did not start out that way. CMOS was originally a slow watch chip circuit design. It had too many SI issues to be considered useful in more complex systems. Latch-up was the most serious concern. Early CMOS chips easily latched up, due to insufficient power/ground distribution and lack of chip output isolation. These problems were better understood and solved about the time that interconnect began dominating two layer metal processes. Once the level of complexity caused the interconnect and not the added overhead of complimentary transistor pair design to be the area limiting feature, CMOS became a viable technology, but its advantageous speed-power product vaulted it onto the primary technology as TTL and N-MOS became too difficult to cool.

In those early days, CMOS was so forgiving that there were occasions when CMOS SRAMS would seem to work without their power connected. It was only necessary to keep enough Vdd levels on the input pins to charge up the power/ground structure through the protection diodes. The frequent well taps from a thoroughly connected set of power/ground grids meant the IR drop and 1+ Volts of internal power/ground noise still left more than a volt of noise margin on these 5 Volt devices. It was merely a matter of appropriately de-rating the devices. The process dimensions were so large that crosstalk was negligible, even with the fast switching speeds of CMOS. Indeed, as the technology was so forgiving, EDA could focus on the more pressing job of handling the ever increasing complexity of semiconductor devices.

We have now pushed the semiconductor lithography to the point where all these issues are returning. Today wires are an order of magnitude closer together than when we first started to use CMOS. Crosstalk issues become significant on wires that are even less than half the distance of the edge dimension of many of today's chips. At today's level of complexity and performance, even CMOS consumes too much power. To compensate we have moved to lower and lower operating voltages, which has made the power/ground distribution, once so easily over-designed, insufficient to consistently maintain adequate noise margins for all the devices on the chip. At the same time, this power issue has increased the need for more active on-chip power control, further aggravating the problem. Finally, the need to integrate analog and digital circuits and sophisticated I/O designs, while minimizing the spacing between them, has increased the need to control substrate noise.

Oddly enough the same features which made CMOS so attractive are now the source of our SI issues. Power/ground and substrate noise is largely a function of the capacitive-switching nature of CMOS, which gives it such a good speed-power product. Similarly, the high gain of CMOS, which provides such high performance also increases the dV/dt of the signals, which in turn contributes to aggressor nets. Until we come up with a better technology, we must attempt to solve the problems with the one we have.

The EDA industry has been very good at abstracting and hiding the complexity of the process of designing complex semiconductor chips. Until they have indisputably solved all the SI issues in deep submicron designs, analog and digital development engineers must be aware of, and deal with, these issues themselves. Unfortunately, these issues are not easily solved. Simple rules of avoidance for such issues as crosstalk and IR drop result in uncompetitive products due to excessive over-design. On the other hand simplistic detection and individual correction leads to excessive inspection of good devices if too conservative, or the existence of SI problems in the real silicon if too optimistic. While engineers find individual inspection of 1000s of good components of a complex system design both time consuming and tedious, the alternative is far worse. Real SI problems in silicon are hard to detect, and even harder to isolate. They are intermittent enough to escape normal testing, which means they are often found in system debug, not at chip test. They are not only intermittent, but they often manifest themselves with intermittently different signatures. This makes them extremely difficult to isolate. For example, a marginal power distribution problem would likely manifest itself as a lost cycle or state in one part of the chip during high activity of that part in conjunction with high activity in some but not all of the adjacent parts of the chip. It could then manifest itself on many different types of activity within that part of the chip, given there is sufficient activity around that part of the chip. The specific activity and the areas of activity can be different so long as the overall activity level lowers the operating voltage enough to cause a problem. Unless a power problem is suspected, the normal digital debug techniques will not lead to a consistent result. Take the old un-powered SRAM, mentioned above, as a specific example. It failed only occasionally when the address zero (00000) was left on the inputs for too long (because the part had no power). Normal testing saw intermittent failures around address 0, but not always on address 0 (since the discharge is activity dependent).

Given the inability to observe the internal states of today's complex System on Chip ICs (SoCs), some digital problems can take months of debug to isolate and correct, and SI problems in real silicon can take even longer. Ignoring the problem, or using optimistic checkers, is not an option. This leaves the need for more accurate modeling, detection and correction of today's SI issues. The need for better solutions to the SI issues is obvious, but as a result of past complacency, there has been little effort, until now, to provide a book, that serves as the starting point for such solutions. All digital and analog design engineers that plan on developing large complex SoCs, using deep submicron semiconductor technology, had well brush up on today's SI problems and their solutions, which this book covers.

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Foreword

Signal Integrity: A Problem for Design and CAD Engineers

The electronics revolution is built upon the idea of expressing information as electronic signals. Operations on these signals, when compared to the mechanical operations that proceeded them, are quick, accurate, and reliable. Moreover, the circuits that use these signals are very small, and can be built in enormous numbers at low cost by printing them on the surface of a silicon wafer. The electronics revolution of the past 50 years is a direct result of the advances in processing electronic signals.

These signals are generated, transported, and detected by nonideal physical structures, and hence are subject to various forms of distortion and corruption. Part of the engineering effort of chip design is making sure these distortions do not rise to the level where they adversely affect the chip function. This is the problem of signal integrity. This can be further divided into three parts—How do you get the raw data you need? How do you determine if you have a problem, and then how do you design so the problem is reduced to a tolerable magnitude? In this case, the raw data is obtained through parasitic extraction, analysis, and modeling operate on this data to find possible problems, and various design methods can be used to avoid and/or correct the problems when found.

Parasitic extraction is an important problem in its own right. Analysis and modeling are crucial, and form the bulk of the papers here. By and large the problem is one of efficiency and not of theory; field solvers and circuit simulators are widely believed to be sufficiently accurate, but are simply too slow and of too-limited capacity for use on modern chips containing millions of signals. Design techniques to minimize, prevent, work around, and fix signal integrity problems are limited only by the imaginations of engineers, and are well represented here.

In the digital domain, we can easily specify what we mean by Signal Integrity. We must not confuse a one and a zero, and the timing of the signal must lead to proper operation at the required speed. Analog criteria are more complex since many different aspects of the signal representations may be important. Furthermore, the allowed levels of corruption are usually much lower than those needed to prevent errors in digital logic.

The main signal integrity problems are crosstalk noise, crosstalk induced delay variations, power supply voltage drop, self and mutual inductance, and substrate coupling.

Crosstalk noise and crosstalk-induced delay variations are changes induced in a nominal signal by interference from neighboring nets. These effects have become steadily more important as interconnect lines have become thicker in proportion to their width, with the corresponding increase in the ratio of coupling to grounded capacitance.

Crosstalk noise can be treated on several levels—it can be analyzed either exactly through circuit simulation, or approximately by means of various simplifications. Purely digital effects (such as two lines that cannot switch in the same clock cycle because of their logical relationship) can be included or ignored. Ultimately, the objective is not to analyze these problems but to produce a chip that is free of them. Towards this end, changes in the design process, ranging from state assignment to global and detailed routing, can be used to reduce these effects.

Crosstalk induced delay variation was first ignored, then treated simply as a Miller-induced multiplier for coupling capacitance, then treated explicitly. Both approaches are covered here.

Voltage drops in the power supply network, either static or dynamic, are conceptually simple. Since the networks are huge, however, considerable effort has gone into computational simplifications. This also leads naturally into electromigration concerns (technically a design integrity problem, but closely related.

Inductance is another area that is well understood if efficiency is not a concern. Simulating the chip including a huge network of RLC's and including coupled inductors will give the right result—one that matches silicon. Unfortunately, this approach is computationally infeasible for all but the smallest chips. Thus, how inductance can be extracted, how it is modeled, and how it can be avoided are of prime concern.

Substrate coupling arises since all parts of the chip are built on a common, electrically conductive substrate, the silicon wafer. This is well-known among analog designers, especially those that must contend with large noisy digital circuits on the same chip. Unlike the other problems mentioned so far, it can still be ignored by purely digital designers working in CMOS. But as chips get bigger, and hence are more likely to implement systems with at least some analog portions, the problem cannot be ignored. It must certainly be considered during floorplanning, and verified after layout.

Chip designers do not need to be experts in each of these areas, which is fortunate since each problem is complex in its own right. Chip designers do, however, need to understand each of these problems well enough to know when a more detailed examination is warranted, or whether a simple approach to avoiding the problem will suffice. Even this limited understanding has been difficult to come by. Because these problems are highly technical, and because they have gradually appeared over the last decade, the relevant papers are widely scattered through the technical literature. They are found in the proceedings of many different conferences and in the journals of many different technical societies. It is highly unlikely for any one individual to have easy access to all this material, or to even know that some of it exists.

This book performs a valuable service by bringing these papers together. In addition to easy reference, it provides a good overview of the field, and a convenient way to compare different authors' approaches to the same problem. This book deserves to be on the shelf of modern chip designers, whether they are seeking detailed analysis methods or simply to reassure themselves that a particular problem is not critical on their chip.

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Preface

Signal Integrity is no longer an issue for microprocessor and radio frequency designers who designed high-end custom IC designs. As technology scales, clock frequencies rise, and the need for higher integration of analog and digital IP blocks increases, unwanted parasitic effects become more and more a gating factor to IC design project success. Many of these effects can be prevented or analyzed and fixed in isolation, but increasingly they are becoming highly dependent on each other. This all creates a lot of confusion and subjective opinion in the IC design world about how to deal with these new problems. The purpose of this book is to help clear these confusions, and offer a number of methods for IC designers and CAD engineers to model, and then solve, these problems.

This book has been structured to be useful to both new and advanced digital and mixed-signal IC engineers. To enable this, each part is carefully partitioned with one or two leading tutorial papers. Tutorial papers are followed by papers on issues such as analysis, extraction, and modeling techniques, as well as optimization/reduction and design methods. Finally, useful papers are presented from related topics.

The book begins with a paper presenting a Designer's Perspective to Signal Integrity Effects in System-on-Chip Design. This paper has been authored by hardware and software engineers from companies worldwide, and provides a real-life overview of the design issues faced.

In Part 1, a series of papers covering Interconnect Crosstalk are presented. Issues such as noise-aware static timing analysis, and post-layout routing optimization are discussed.

In Part 2, Inductance Effects are discussed. Issues such as when inductance is important, inductance extraction, and design techniques are covered.

In Part 3, Power Grid and Distribution Noise is presented. Issues such as floorplanning methods and electromigration are covered. Mixed-signal supply noise issues are also presented.

Finally, in Part 4, Substrate Noise issues are discussed. Issues such as extraction and design techniques are covered, as well as general noise issues in mixed-signal IC design.

With such a broad range of topics involved in Signal Integrity in IC designs, this book cannot possibly cover every topic of interest, and there are without doubt other books that offer more details in very specific areas. However, it is my hope that this book will act as a sufficient central reference point for Signal Integrity issues (both now and going forward), helping the reader both understand the various issues and offering practical methods for integrating the effects in design flows.

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R. S.

Contents

Signal Integrity Effects in System-on-Chip Designs - A Designer's Perspective

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Abstract - **In this paper, we present a designer's perspective to the signal integrity issues that affect authors and integrators of blocks used in System-on-Chip designs. In particular, after presenting typical process parameters used for such designs, we focus on signal integrity issues in the context of power grid noise, interconnect crosstalk and substrate coupling. In each case, we describe the problem from the point of view of System-on-Chip designers (both block authors and block integrators), and briefly discuss standard techniques that are used to alleviate the problem.**

1 INTRODUCTION

System-on-Chip (SoC) design has taken many meanings for IC designers. However, for all of them, the issues of Intellectual Property (IP) block integration and verification are important problems. As technologies scale, it becomes very difficult to both design (or "author") IP blocks and then integrate them. In this paper, a background is presented on the Signal Integrity (SI) problems that designers face and the overall need to tackle them in SoC designs.

It is important for the designer to understand the design process of IP block authoring to integration, and the processes that System-on-Chip Designers typically design within. The following subsections cover these topics. These are followed by sections on the issues of power grid noise, interconnect crosstalk, and substrate coupling. This paper complements the material presented in this book, and although much of the content in this paper involves a basic understanding of SI, advanced knowledge is not a prerequisite.

1.1 The Process of System-on-Chip Design

Today's semiconductor fabrication technology can manufacture chips containing tens of millions of gates, thus allowing full systems to be integrated onto a single semiconductor chip. Using current Electronic Design Automation (EDA) techniques, creating such SoCs from scratch would require an army of engineers. As a result, there has been considerable effort on the development of methodologies centered on design reuse in order to minimize the amount of re-engineering of each new chip. Most of these SoC methodologies involve the selection and integration of appropriate existing internal or third party IP blocks - called Virtual Components (VCs) - based on an architecture which meets the original product requirement.

This SoC methodology effort involves the specification of standard formats and interface requirements that will ensure the successful reuse and integration of such VCs. This allows the separation of VC creation and SoC integration, and has helped legitimize the emerging third party IP business. As a result, most SoC design methodologies focus on the creation of IP libraries containing appropriately collared VCs, along with the techniques to extract and integrate these existing, qualified VCs into an SoC. By the very nature of these methods, there is considerable data hidden within the VCs. The key to successful integration is the provision of sufficient information about each VC to the integrator to allow successful integration of these components. If the components are all *soft* (i.e., in an RTL format such as VHDL or Verilog), such data hiding is minimized and the blocks may be physically implemented together. On the other hand, if the VCs are *hard* (i.e., polygons in a layout in, for example, GDSII format), a form of block-based implementation must be used. In this case, the VCs are viewed as black boxes that must be physically integrated together. Their functional, clock, test and physical requirements must be sufficiently delineated to properly integrate such VCs with the rest of the SoC design.