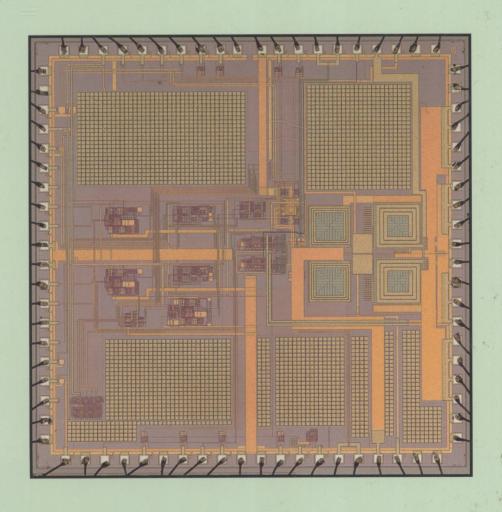
# Feedback Linearization of RF Power Amplifiers



Joel L. Dawson Thomas H. Lee

# FEEDBACK LINEARIZATION OF RF POWER AMPLIFIERS

JOEL L. DAWSON Stanford University

THOMAS H. LEE Stanford University







Kluwer Academic Publishers Boston/Dordrecht/London Distributors for North, Central and South America: Kluwer Academic Publishers 101 Philip Drive Assinippi Park Norwell, Massachusetts 02061 USA Telephone (781) 871-6600 Fax (781) 871-6528 E-Mail <kluwer@wkap.com>

Distributors for all other countries: Kluwer Academic Publishers Group Post Office Box 322 3300 AH Dordrecht, THE NETHERLANDS Telephone 31 78 6576 000 Fax 31 78 6576 474 E-Mail <orderdept@wkap.nl>



Electronic Services <a href="http://www.wkap.nl">http://www.wkap.nl</a>

#### Library of Congress Cataloging-in-Publication

Title: Feedback Linearization of RF Power Amplifiers

Author (s): Joel Dawson and Thomas H. Lee

ISBN: 1-4020-8061-1

ISBN: 1-4020-8062-X (eBook)

Copyright © 2004 by Kluwer Academic Publishers

All rights reserved. No part of this publication may be reproduced, stored in a retrieval system or transmitted in any form or by any means, electronic, mechanical, photo-copying, microfilming, recording, or otherwise, without the prior written permission of the publisher, with the exception of any material supplied specifically for the purpose of being entered and executed on a computer system, for exclusive use by the purchaser of the work.

Permissions for books published in the USA: <u>permissions@wkap.com</u>
Permissions for books published in Europe: permissions@wkap.nl
Printed on acid-free paper.

Printed in the United States of America

# Feedback Linearization of RF Power Amplifiers

To Mari

此为试读,需要完整PDF请访问: www.ertongbook.com

# Acknowledgments

It is with great pleasure that we acknowledge the many people who have supported the work described in this book. In particular, Professor Stephen Boyd deserves credit for originally proposing the investigation of Chapter 2, and for working closely with us to bring it to fruition. Professors Bruce Wooley and Donald Cox graciously read a draft of this entire manuscript, and provided valuable and insightful comments.

We would also like to thank a number of institutions for their support of this investigation. Lucent Technologies, the National Science Foundation, and the Hertz Foundation all provided fellowship support, as did Stanford University through its Stanford Graduate Fellows program. National Semiconductor continues to provide Stanford students with free use of its  $0.25\mu m$  CMOS process, an almost unbelievable luxury for students in our field. Agilent Technologies supported this work through the FMA program at CIS. This was largely due to the efforts of Dr. Jim Hollenhorst and Paul Corredoura, who in addition provided friendship and were sources of stimulating technical discussion.

Stanford's Center for Integrated Systems was a wonderful place to work, and this was due in large part to the presence of its graduate students. Dr. Dawson gladly acknowledges all members, past and present, of the Lee (SMIrC), Wooley, and Wong groups who have given their friendship and collaboration. Dr. David Su, formerly of the Wooley group, was particularly generous with his advice and insight during the hardware testing stages of this investigation.

Ann Guerra, the administrative assistant to Professors Lee and Wooley, has been a marvel at making administrative tasks run smoothly. She does this with a warmth, kindness, and humor that have greatly eased the passage of many students through the Ph.D. program. We take this opportunity to thank her for being a wonderful person to work with.

Dr. Dawson would also like to acknowledge his family, which was a source of unending love and support. They showed him that he is not, and never has been, alone in his endeavors. Finally, Marisol Negrón deserves a special

acknowledgment for her steadfast love and support during the toughest days of this investigation. It is only fitting that this book be dedicated to her.

# **Contents**

De	uicau	OII		v
Lis	t of F	igures		xi
Lis	st of T	ables		xv
Ac	know	ledgmei	nts	xvii
1.	INT	RODUC	CTION	1
	1.1	Motiva	ation	1
	1.2	Organi	zation	2
2.	OPT	IMAL A	ALLOCATION OF LOCAL FEEDBACK IN	
	MU	LTISTA	GE AMPLIFIERS	5
	2.1	Ampli	fier stage models	6
		2.1.1	Linearized static model	6
		2.1.2	Static nonlinear model	6
		2.1.3	Linearized dynamic model	8
		2.1.4	Static noise model	8
	2.2	Ampli	fier analysis	8
		2.2.1	Gain and output swing	9
		2.2.2	Sensitivity	10
		2.2.3	Nonlinearity	10
		2.2.4	Bandwidth	11
		2.2.5	Delay and rise-time	12
		2.2.6	Noise and dynamic range	12
		2.2.7	SFDR and IIP linearity measures	13
	2.3	Geom	etric programming	14
		2.3.1	Geometric programming in convex form	14
		2.3.2	Solving geometric programs	. 15
	2.4	Optim	nal local feedback allocation	16

		2.4.1	Closed-loop gain	10
		2.4.2	Maximum signal swing	10
		2.4.3	Sensitivity	1
		2.4.4	Bandwidth	1
		2.4.5	Noise and dynamic range	18
		2.4.6	Delay and rise-time	18
		2.4.7	Third-order distortion	13
		2.4.8	SFDR and IIP3	18
	2.5	Design	Examples	1
		2.5.1	Trade-offs among bandwidth, gain, and noise	19
		2.5.2	SFDR versus gain	2
		2.5.3	Stage selection	2
	2.6	Geome	tric programming summary	20
	2.7	An exa	mple application	2
		2.7.1	Linearized static model	28
		2.7.2	Static nonlinear model	2
		2.7.3	Linearized dynamic model	29
		2.7.3.1	An alternative formulation: open-circuit time constants	30
		2.7.4	Static noise model	3
	2.8	Local f	eedback allocation for power amplifier linearization	3
3.	THE	PROBI	LEM OF LINEARIZATION	3
	3.1	The tra	deoff between linearity and power efficiency	3
	3.2	Can no	onlinear system theory help?	3
	3.3	An ove	erview of linearization techniques	3
		3.3.1	Power backoff	3:
		3.3.2	Predistortion	3
		3.3.3	Adaptive predistortion	3
		3.3.4	Feedforward	3
		3.3.5	Dynamic biasing	3
		3.3.6	Envelope elimination and restoration	3
		3.3.7	LINC	4
		3.3.8	Cartesian feedback	4
1.	PHA	SE ALI	GNMENT IN CARTESIAN FEEDBACK SYSTEMS	4
	4.1		quences of phase misalignment in Cartesian feedback	
		system		4
		4.1.1 4.1.2	Terminology Convention	4
		/1 1 7	Impact of phase misalignment on stability	4

Contents	ix
----------	----

		4.1.3	Compensation for robustness to phase misalignment	46
	4.2	A nonl	inear regulator for maintaining phase alignment	48
		4.2.1	Nonlinear dynamical system	48
		4.2.2	Stability concerns	50
		4.2.3		51
		4.2.4	Impact of multiplier offsets	51
	4.3	A new	technique for offset-free analog multiplication	52
		4.3.1	Limits on performance	55
	4.4	Summa	ary	56
5.	A FU	JLLY IN	NTEGRATED CARTESIAN FEEDBACK SYSTEM	57
	5.1	Motiva	tion for pursuing Cartesian feedback	57
	5.2	Motiva	tion for a monolithic implementation	60
	5.3	CFB IC	C at the system level	61
	5.4	The ph	ase alignment system	62
		5.4.1	Circuit details	66
		5.4.1.1	Basic multiplier cell	66
		5.4.1.2	Phase error computation	70
		5.4.1.3	An analog integrator	71
		5.4.1.4	A constant 1-norm controller	78
		5.4.1.5	Forming the matrix rotation operator	82
		5.4.2	Phase alignment system results	84
	5.5	The lin	nearization circuitry	88
		5.5.1	Circuit details	88
		5.5.1.1	Loop driver	89
		5.5.1.2	Analog matrix rotation	92
		5.5.1.3	Upconversion mixer	93
		5.5.1.4	Power amplifier	93
		5.5.1.5	Downconverter	95
		5.5.1.6	Polyphase filters	99
		5.5.1.7	Constant-g <sub>m</sub> biasing	100
		5.5.2	Linearization system results	102
			Linearization behavior	102
		5.5.2.2	Loop stability	104
	5.6	Summa	ary	105

6.	CO	NCLUSION	113
	6.1	Summary ·	113
	6.2	Future work	114
Ap	pend	ices	117
A	The	First Prototype of the Phase Alignment Concept	117
	<b>A.</b> 1	Phase shifter	117
	A.2	Phase error and integrator	118
	A.3	Test results	118
В	The	Experimental Setup for CFB IC	123
	<b>B.1</b>	Single-ended-to-differential conversion	123
	<b>B.2</b>	Clock reference	123
	B.3	Overview of test board	124
Re	feren	ces	127
Inc	lex		133

# **List of Figures**

2.1	Block diagram of multistage amplifier.	5
2.2	Linearized static model of amplifier stage.	7
2.3	Nonlinear static model of amplifier stage.	7
2.4	Linear dynamic model of amplifier stage.	8
2.5	Static noise model of amplifier stage.	9
2.6	Maximum bandwidth versus limit on input-referred noise.	20
2.7	Optimal feedback allocation pattern, for maximum bandwidth with limit on input-referred noise. Gain = 23.5dB.	21
2.8	Maximum bandwidth versus required closed-loop gain.  Maximum input-referred noise = 4.15e-7 V rms.	22
2.9	Optimal feedback allocation pattern for maximum bandwidth versus required closed-loop gain. Maximum inputreferred noise = 4.15e-7 V rms.	23
2.10	Maximum spurious-free dynamic range versus required gain.	24
2.11	Optimal feedback allocation pattern for maximum spurious- free dynamic range versus required gain.	25
2.12	CMOS source-coupled pair and differential half-circuit.	27
2.13	Source degeneration as a form of feedback.	28
2.14	Modification for nonlinear static model.	29
2.15	Modeling dynamics using the Miller approximation.	29
2.16	MOSFET noise model.	31
2.17	MOSFET gate and drain noise.	31
3.1	A high-efficiency power amplifier.	34
3.2	Using predistortion to linearize a power amplifier.	37
3.3	An example of adaptive predistortion.	37

3.4	Feedforward linearization.	38
3.5	Envelope elimination and restoration.	39
3.6	The LINC concept.	40
3.7	Cartesian feedback.	41
4.1	Typical Cartesian feedback system.	44
4.2	Simple feedback system.	44
4.3	Cartesian feedback under 90-degree misalignment.	46
4.4	Root locus plots for dominant-pole and slow-rolloff $(\frac{k}{\sqrt{s}})$ compensation.	47
4.5	Rotation of the baseband symbol due to phase misalignment.	49
4.6	Phase alignment concept.	50
4.7	Linearized phase regulation system. 'M' is the desired	
	misalignment, which is nominally zero.	51
4.8	New technique for offset-free analog multiplication.	53
4.9	Graphically computing $c_0(t)c_{90}(t)$ .	55
5.1	The predistorting action of Cartesian feedback.	58
5.2	Cartesian feedback used to train a predistorter.	59
5.3	Conceptual diagram of CFB IC.	62
5.4	Phase alignment by phase shifting the local oscillator.	63
5.5	Phase alignment by rotating the baseband symbol.	64
5.6	Analog technique for generating $v_{\sin \phi}$ and $v_{\cos \phi}$ .	65
5.7	Analog rotation using the 1-norm.	65
5.8	Using CMOS voltage switches and a comparator to realize a folding amplifier. Switches are closed when their respective control signal is high.	66
5.9	Basic topology for multiplier cell. All transistors connected to a $y$ input are sized $M_{top}$ , and all transistors connected to a $x$ input are sized $M_{bot}$ .	67
5.10	Multiplier cell.	69
5.11	Commutating mixer for chopping. NMOS devices are sized 3/0.24, PMOS 9/0.24.	70
5.12	Phase error computation.	71
5.13	Op-amp_d1, a fully differential op-amp for the S.C. integrator.	72
5.14	Opamp_pL, a single-ended op-amp for low common-mode inputs.	74
5.15	Opamp_nL, a single-ended op-amp for high common-mode inputs.	74

List of Figures	xi	

5.16	alignment system. Switches are complementary: NMOS 2/0.24, PMOS 6/0.24.	75
5.17	Chopping clocks derived from off-chip source.	77
5.18	Integrator clock, which transitions on the trailing edge of the external 20MHz source.	78
5.19	Circuit for generating clock phases.	78
5.20	Constant 1-norm controller: circuit realization of figure 5.7.	79
5.21	Differential transconductor.	80
5.22	Folding amplifier for constant 1-norm controller.	81
5.23	Computation of the rotation operator.	83
5.24	Overview diagram of phase alignment system.	84
5.25	Phase alignment performance for a 500mV amplitude, 10 kHz square wave.	85
5.26	Effective output offset, $\delta_{O}$ , of the chopper-stabilized multipliers of figure 5.12.	87
5.27	Trace capture of a phase alignment experiment. The Cartesian feedback loop is open.	88
5.28	Illustration of phase alignment stabilizing the closed-loop CFB system.	89
5.29	Loop driver amplifier.	90
5.30	Baseband_g <sub>m</sub> , a circuit to carry out the matrix rotation.	92
5.31	Upconversion mixer. All transistors are sized $2 \times 50.4/0.24$ , all resistors are $10k\Omega$ .	94
5.32	Power amplifier.	94
5.33	Potentiometric downconversion mixer, together with biasing and capacitive RF attenuator.	96
5.34	Op-amp_d2, a fully differential op-amp for the down-	
	conversion mixer.	98
5.35	A two-stage polyphase filter.	99
5.36	A three-stage polyphase filter.	100
5.37	Constant_gm cell, which establishes the voltage 'pbias'	
	for the entire chip.	101
5.38	Die photo.	107
5.39	Comparison between predistortion inputs and down-converter outputs for no misalignment.	108
5.40	Comparison between predistortion inputs and down-converter outputs for 45-degree misalignment.	108

	0.41	Frequency-domain example of linearization behavior.	109
5	5.42	Compensation networks used in stability experiments.	109
5	5.43	Step response of aligned, dominant-pole compensated system	.110
5	5.44	Step response of aligned, uncompensated system.	110
5	5.45	Step response of aligned, slow-rolloff compensated system.	111
5	5.46	Step response comparison between dominant-pole and	
		slow-rolloff compensated systems for 90-degree misalignment	.111
F	<b>A</b> .1	Phase shifter.	117
F	<b>A.2</b>	Phase shifter implementation.	118
P	A.3	Phase error computation and integration.	119
P	<b>A.4</b>	Test setup.	119
P	A.5	Measured phase alignment vs. system drift	120
P	A.6	Phase alignment vs. baseband frequency	121
F	3.1	Converting from single-ended to differential signals.	124
E	3.2	The on-board clock reference.	124
E	3.3	The test board.	125

# **List of Tables**

2.1	Candidata atazaa	20
	Candidate stages.	26
5.1	Multiplier elements.	69
5.2	Phase error computation elements. Quiescent current	
	includes current draw of multiplier cells.	70
5.3	Elements for integrator op-amp. Quiescent current in-	
	cludes current draw of Opamp_nL and Opamp_pL.	72
5.4	Opamp_pL elements.	73
5.5	Opamp_nL elements.	75
5.6	Integrator capacitor values.	75
5.7	Elements for chopping clocks.	77
5.8	Constant 1-norm elements. Quiescent current includes	
	current draw of folding amplifier and G <sub>m</sub> cells.	79
5.9	Differential transconductor elements.	80
5.10	Folding amplifier elements.	82
5.11	Rotation operator elements.	84
5.12	Elements for loop driver amplifier. Quiescent current	
	includes current draw of Opamp_nL and Opamp_pL.	91
5.13	Matrix rotation operator elements.	93
5.14	Power amplifier elements.	95
5.15	Downconversion mixer elements. Quiescent current in-	
	cludes current draw of Op-amp_d2.	96
5.16	Elements for downconversion op-amp.	98
5.17	Polyphase filter elements.	100
5.18	Constant-g <sub>m</sub> bias cell elements.	101
A.1	Comparison with examples from the literature.	120

## Chapter 1

## INTRODUCTION

Research activity in the area of radio-frequency (RF) circuit design has surged in the last decade in direct response to the enormous market demand for inexpensive, portable, high data rate wireless transceivers. Our expectations for such transceivers, such as cellular phones, rise as they become seemingly ubiquitous. Once, the simple fact of a fairly reliable wireless voice connection was sufficient and even exciting. Now, crystal-clear voice with no lapses in coverage is actively sought, together with the capability to act as a web portal and even a digital assistant. All of this must be accomplished by a device that is cheap enough to be virtually given away, small enough to justify the claim of portability, and frugal enough with power demands to last a long time on a single battery charge.

Cellular phones are just one example of a market that has spurred recent research activity. Wireless local-area networks (WLAN's) are another relatively new application of RF circuit techniques, as is the popular Global Positioning System (GPS). Meeting this demand for a kind of general connectivity involves a host of fascinating technical challenges. Among these, many are associated with the power amplifier, the system block that drives the antenna in any radio transmitter.

### 1.1 Motivation

If the objective is an inexpensive, portable, high-performance transceiver, the desirability of certain circuit characteristics is clear. A low-cost solution is likely to be one in which as many circuit blocks as possible are implemented on the same chip: the cost savings result from the simplified PC (printed circuit) board. An inexpensive IC (integrated circuit) process, such as CMOS, translates directly into a cost savings. Portability implies at least two things from a circuit standpoint: small size, which is another advantage of a highly integrated