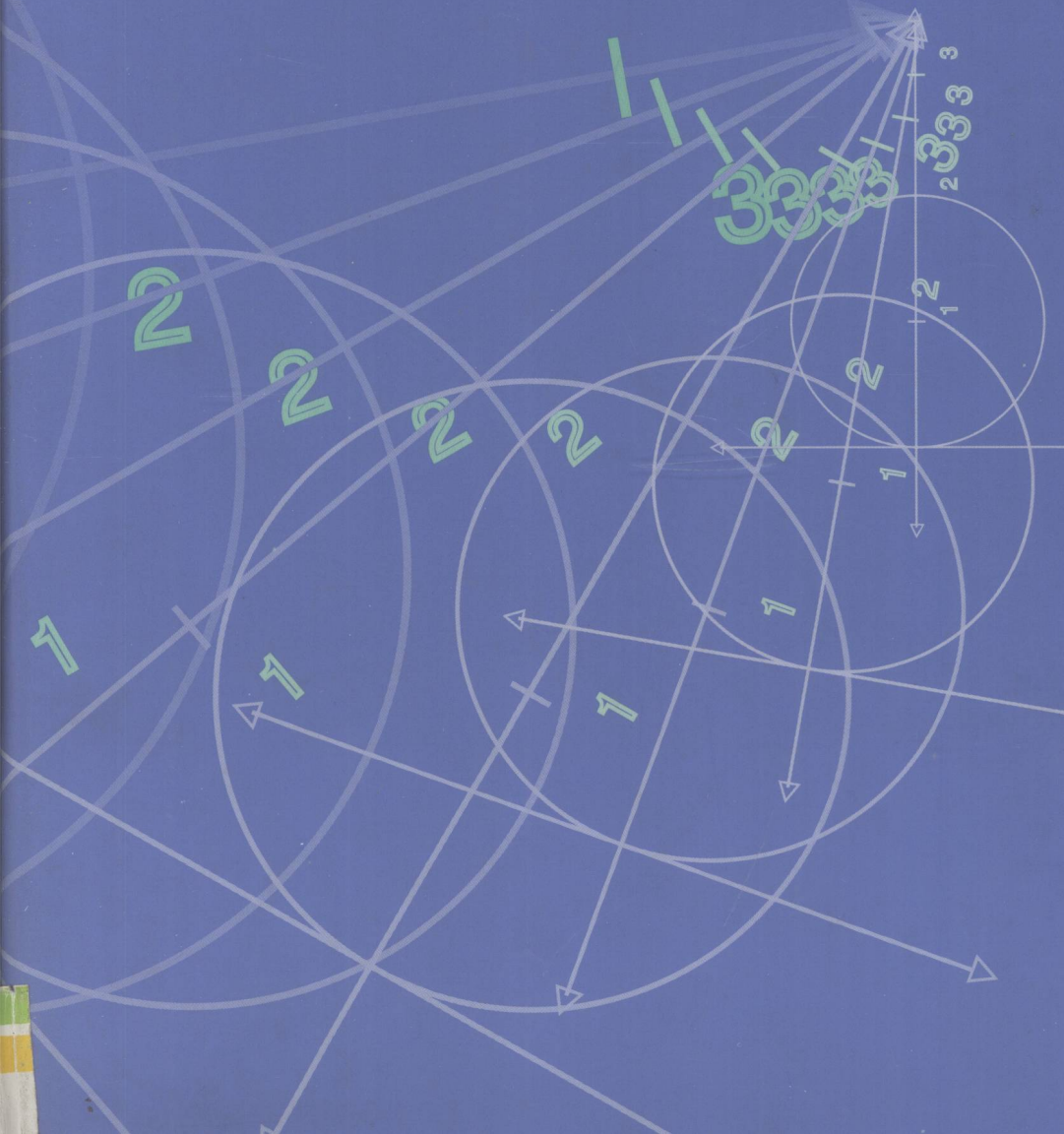
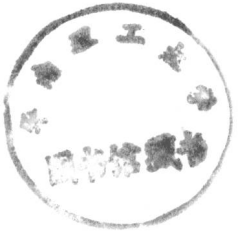
Frequency Synthesizer Design Handbook

James A. Crawford



Frequency Synthesizer Design Handbook

James A. Crawford



Artech House
Boston • London

Library of Congress Cataloging-in-Publication Data
Crawford, James A.
Frequency synthesizer design handbook/James A. Crawford.
Includes bibliographical references and index.
ISBN 0-89006-440-7
1. Frequency synthesizers. I. Title
TK7872.F73C73 1994 94-7655
621.3815'486–dc20 CIP

A catalogue record for this book is available from the British Library

685 Canton Street
Norwood, MA 02062

International Standard Book Number: 0-89006-440-7
Library of Congress Catalog Card Number: 94-7655

10 9 8 7 6 5 4 3 2 1

Frequency Synthesizer Design Handbook

For a complete listing of the *Artech House Microwave Library*,
turn to the back of this book

To Linda,
Brian,
James,
Daniel, and
Kristen

To God be all the glory
Hebrews 2:1–3

Preface

The motivation for this text evolved primarily from my prior employment at Hughes Aircraft Company, Ground Systems Group, Fullerton, California, beginning in the late 1970s. During this time, it was my privilege to work with a number of excellent engineers and scientists. I want to specifically acknowledge Mr. Gary D. Frey, Mr. Jack Chakmanian, and Dr. Knut Konglebeck. From my later tenure at the Linkabit Corporation, San Diego, California, I want to acknowledge Mr. Fritz Weinert as well. In this company, the term "RF black magic" was largely put to rest, with rigorous analytical design methods and techniques favored instead. This text has been written with this same bent toward sound engineering design practice rather than ad hoc cut and try methods.

A number of excellent texts have been available for some time addressing the frequency synthesis area, but most if not all of these books are primarily circuit oriented. This text is intended to address the synthesis subject from a systems perspective instead. Special attention has also been given to the area of sampled-data control systems as they apply to modern phase-locked loop design and as well as other areas where clear design material was felt to be unavailable.

Finally, I want to give a special acknowledgment and word of thanks to Dr. William F. Egan who reviewed major portions of this text over the three years spent in this endeavor.

Contents

Chapter 1

Introduction to Computer-Aided Frequency Synthesizer Design

The phase-lock concept was originally described in a published work by de Bellescize in 1932 [1] but did not fall into widespread use until the era of television where it was used to synchronize horizontal and vertical video scans. One of the earliest patents showing the use of a phase-locked loop with a feedback divider for frequency multiplication appeared in 1970 [2]. The phase-locked loop concept is now used almost universally in many products ranging from citizens band radio to deep-space coherent receivers.

The material presented in this book largely grew out of the author's involvement with a high-performance frequency synthesizer, which is the subject of Chapter 6. Many of the concepts, particularly those related to sampled control systems, led to a number of valuable findings, which are discussed in Chapters 4 and 5. In Chapter 4, the transition between continuous and sampled control system perspectives is dealt with in some detail leading to Chapter 5, which enlarges the sampled control system concepts further.

Many of the underlying design guidelines pertaining to frequency synthesis for wireless communications are rooted in system-level performance requirements, particularly phase noise and discrete spurious requirements. These concepts are developed in detail in Chapter 3 with additional discussion purposely provided to allow individuals to simulate these system imperfections with a computer. Phase noise performance of key synthesis elements is also discussed at some length in Chapter 3.

Chapter 7 addresses a number of the most recent synthesis techniques including direct digital synthesizers (DDSs) and hybrid phase-locked loops. Fractional-*N* synthesis techniques based on sigma-delta modulation concepts are also discussed there.

Chapter 8 addresses the issue of phase-locked loop computer simulation, drawing in part on the results found in Chapters 4 and 5. Numerical techniques that are suitable for this application are developed from first principles.

Finally, Chapter 9 takes an in-depth look at traditional fractional-N frequency synthesis. Several analyses are considered, underscoring the need on the designer's part to be intimately aware of design details at the component level as well as at the circuit design level.

The material presented in this text should be viewed as a supplement to, rather than as a replacement for, a number of excellent texts that are currently available on this subject. Prior knowledge of basic phase-locked loop principles is generally assumed throughout the text. Stochastic process theory is employed sparingly in Chapters 3, 5, and 9. Fairly heavy use of z transforms is made in Chapter 5. Appropriate outside references for this material are provided in each respective chapter.

REFERENCES

[1] de Bellescize, H., "La Reception Synchrone," *Onde Electr.*, Vol. 11, June 1932, pp. 230–240.

[2] Sepe, R.B., R.I. Johnston, "Frequency Multiplier and Frequency Waveform Generator," U.S. Patent No. 3,551,826, December 29, 1970.

Chapter 2

Building Blocks for Frequency Synthesis Using Phase-Locked Loops

The explosion in commercial and consumer level communication products in the late 1980s and early 1990s dramatically revolutionized the availability of high-quality, low-cost componentry for RF system design. The frequency synthesis area has been one of the primary areas where this market pressure has resulted in unprecedented levels of high integration. The majority of consumer level frequency synthesis is currently being done with frequency synthesizers that are based on the single phase-locked loop (PLL) architecture. Designs that would have been multiloop in nature in years past are quickly giving way to hybrid loops, which often utilize a mixture of phase-locked loop technology along with direct digital synthesis. Even more bold progress is being made using, for example, delta-sigma modulator concepts with fractional-*N* synthesis to realize single-loop architectures that can deliver almost arbitrarily small channel spacings while maintaining excellent switching speed and spurious performance.

It seems that phase-locked loops are everywhere, from frequency synthesizer applications in radios to clock deskewing applications within high-speed digital processors. Dedicated hardware frequency multipliers followed by bulky filters are a thing of the past. The integration levels and cost achievable today in the phase-locked loop area make these techniques the solution of choice. As such, the contents of this chapter (and most of this text) focus primarily on the phase-locked loop for frequency synthesis.

2.1 THE DESIGN EQUATION

In about 1983, this author was asked to formulate a high-level "design equation" for general frequency synthesizer design that would factor in all of the normal performance measures plus size, complexity, risk, schedule length, and cost. The task

was fairly meaningless because nearly every integral component, from feedback divider to voltage-controlled oscillator (VCO), had to be custom designed except in fairly benign situations where a few phase-locked loop components were available. The answer usually came back as "near infinite dollars, time, and risk" at least in the case of high-performance, military-type synthesizers. Technologies such as cellular telephone have changed this situation forever.

2.1.1 Mutually Contradictive Requirements

When designing frequency synthesis elements for standardized market areas such as analog cellular and digital cellular telephone, performance requirements have generally been arrived at that have taken into account the RF technology needed to perform the task. With the size of these markets being so large, most component vendors are ahead of the original equipment manufacturers (OEMs) in identifying clever design solutions or they are working directly with the OEMs. Because cost is such an overwhelming factor in consumer electronics, most hardware solutions for a given product are quite similar, having been optimized down to the minimally acceptable solution. Most of the system requirements, therefore, reflect prior consideration of the mutually contradictory requirements encountered in phase-locked frequency synthesizer design.

If starting from scratch, the normal trade-offs that must be made in synthesizer design include (1) phase noise performance, (2) switching speed, (3) discrete spurious performance, (4) frequency and tuning bandwidth, (5) size, (6) power consumption, and (7) cost. The last three items are by far the overwhelming factors in modern consumer electronics design.

Frequency Switching Speed

The precise definition of switching speed for a given system must be based on the modulation waveform employed (in the case of communications) and the system performance degradation incurred. These are system-level issues and are addressed in part in Chapter 3. For a quadrature phase-shift-keyed (QPSK) system, which uses phase shifts of 90-deg multiples to convey information, the settling time is normally defined as the time required for the loop to settle to within 0.1 radian of its steady-state final phase. In an analog FM system, such as an analog cellular telephone, switching speed might be defined as the time required for the loop to reach an output frequency within 100 Hz of the steady-state value. In receiving systems that estimate the incoming signal's carrier phase or frequency immediately after a frequency hop, system impairment will obviously result if the signal's parameters (i.e., phase and frequency) have not settled out because the presence of these transients will degrade the receiving system's estimates.

Increased switching speed always implies a larger phase-locked loop bandwidth, which normally results in higher discrete spurious levels. For larger loop bandwidths, frequency reference noise and phase detector noise sources lead to wider output phase noise pedestals about the carrier signal. Control loop stability margins normally degrade with increasing loop bandwidth as well, leading to increased "peaking" of noise sources present in the VCO. These issues are dealt with in greater detail in Chapters 3, 4, and 5.

A reasonably good rule of thumb for switching speed while maintaining low discrete spurs is simply 50 reference cycles. If a phase-locked loop is using a reference frequency of 30 kHz, achieving phase-lock will normally require a minimum of roughly 1.7 ms. If a switching speed requirement is at or below this guideline, more detailed assessment is mandated. This estimate is based in part on the fact that the switching transient error normally decays proportionally with respect to $\exp(-\zeta\omega_n t)$.

As discussed in Chapters 5 and 6, switching speeds on the order of a few reference periods are theoretically achievable, but not without extreme attention to detail. Normally, custom components will have to be designed if this performance level is needed, thereby driving cost issues dramatically.

Much of this text addresses phase-locked loop frequency synthesis in the context of a sampled control system. As developed in Chapter 5 at length, use of closed-loop bandwidths $\geq 0.1\ F_{\text{ref}}$ must be done with care because sampling effects can significantly affect both system phase noise and transient performance.

A trade-off study between switching speed, loop filter attenuation of the first frequency reference sideband spurs, and system stability is given in Chapter 3, which should provide some design assistance. The final feasibility answers cannot normally be obtained without knowing a minimum of information, specifically: (1) phase detector leakage or glitch energy at the reference frequency when in steady state, (2) the phase detector and loop electronics anticipated noise floor, and (3) VCO tuning sensitivity and phase noise performance. Characterization of the phase detector area is normally the most difficult because few vendors provide adequately detailed information.

2.1.2 The Fuzzy Line That Separates RF/Analog and Digital Techniques

High-speed digital VLSI has dramatically changed the frequency synthesis landscape by making what were heretofore impossible concepts physically realizable. The highly integrated complementary metal-oxide semiconductor (CMOS) PLL devices that now operate at input frequencies as high as 2.5 GHz clearly fall into this category. Digital very large scale integration (VLSI) technology, however, has done more than simply brought faster PLL devices to the marketplace.

Perhaps the most dramatic impact of high-speed digital VLSI on frequency synthesis has been in the architecture area where truly new synthesis concepts have