

APPROXIMATE REASONING

— IN —

INTELLIGENT SYSTEMS,
DECISION AND CONTROL

Edited by

E. SANCHEZ

Université Aix-Marseille II, Marseille, France
and

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University of California, Berkeley, USA

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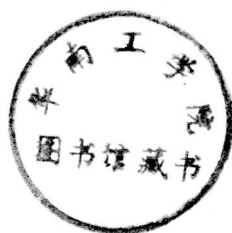
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Preface

It is a long-standing tradition in science to accord respect to what is quantitative, precise and rigorous, and view with disdain what is not. We are impressed by results which require long proof and deep reasoning even in fields in which the systems are much too complex to admit of precise analysis. As a case in point, the von Neumann-Morgenstern theories have spawned a vast and mathematically sophisticated literature aimed at constructing a rigorous foundation for decision analysis, game playing and econometric modeling. And yet, it is widely agreed at this juncture that such normative theories have failed to reflect the remarkable human ability to act in situations in which the underlying information is ill-defined, incomplete or lacking in reliability, and thus are of little predictive value in the analysis of human behavior.

In effect, what is missing in such theories are the bridges to the real world. These bridges are not there because the precision of mathematical models of human reasoning on which such theories are based is much too high considering the ways in which humans reason and make decisions in realistic settings. What this implies is that the development of theories of approximate — rather than precise — reasoning is a prerequisite for the development of theories of human behavior which can provide realistic models of rational thinking in ill-defined environments.

The papers presented in this volume are aimed at this objective. Many, but not all, of the papers make use of the conceptual framework of the theory of fuzzy sets. In this theory classes are not required to have sharply defined boundaries as they do in classical set theory. As a result, the theory of fuzzy sets provides a better model for human concepts and serves as a more expressive language for the representation of knowledge — especially commonsense knowledge.

An important advantage of fuzzy logic — which is based on the theory of fuzzy sets — is that it subsumes both multivalued logic and probability theory. By providing a single framework for both logical and probabilistic inference, fuzzy logic makes it possible to develop rules of inference in which the premises as well as the probabilities are lexically imprecise, i.e., contain predicates and probabilities exemplified by *small*, *large*, *much larger than*, *usually*, *most*, *likely*, *very unlikely*, etc. This facility plays a particularly important role in the representation of uncertainty in expert systems.

The emergence of expert systems as one of the major areas of activity in information science and technology is providing a strong impetus to the development of theories of approximate reasoning as a basis for representing — and reasoning with — expert knowledge. It would be unrealistic to expect that such theories will be easy to develop, since human reasoning is much too complex to admit of simple formalization. Nevertheless, significant progress is being made, as is demonstrated by the papers presented in this volume — papers which address a wide range of issues in approximate reasoning and represent a broad variety of viewpoints and countries of origin. What is particularly important about these papers is that they point the way to applying approximate reasoning to realistic problems which do not lend themselves to analysis by conventional techniques. Through such applications, approximate reasoning will eventually establish itself as a powerful system of reasoning for dealing with the pervasive imprecision of the real world and approaching the human ability to manipulate commonsense knowledge.

The Editors

Publisher's Note

Most of the papers appearing in this volume were presented at the International Conference on BUSINESS APPLICATIONS OF APPROXIMATE REASONING, Paris, 8-10 January 1986, sponsored by Générale de Service Informatique and organised by Georges Attard (GSI) and Elie Sanchez.

Contents

Fuzzy Hardware Systems of Tomorrow T YAMAKAWA	1
Functional Requirements for a Fuzzy Expert System Shell W SILER, J BUCKLEY & D TUCKER	21
An Uncertainty Calculus for Expert Systems J F BALDWIN	33
Automatic Generation of Verbal Comments on Results of Mathematical Modelling V NOVAK	55
Portfolio Analysis Using Possibility Distributions J J BUCKLEY	69
A Fuzzy Decision Support System for Strategic Planning N GREEN HALL	77
A Clinical Alarm System Using Techniques from Artificial Intelligence and Fuzzy Set Theory S J HENKIND, R R YAGER, A M BENIS & M C HARRISON	91
Learning from Examples in Presence of Uncertainty F BERGADANO, A GIORDANA & L SAITTA	105
Use of Fuzzy Logic in a Rule-Based System in Petroleum Geology J LEBAILLY, R MARTIN-CLOUAIRE & H PRADE	125
Rule-Based Process Control Using Fuzzy Logic J EFSTATHIOU	145
Diagnosis Based on Subjective Information in a Solar Energy Plant A ASSE, A MAIZENER, A MOREAU & D WILLAEYS	159
Diagnostics of Faulty States in Complex Physical Systems Using Fuzzy Relational Equations J KITOWSKI & M BARGIEŻ	175
Keyword Index	195

Fuzzy Hardware Systems of Tomorrow

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ABSTRACT

Nine basic fuzzy logic circuits employing p-ch and n-ch current mirrors are presented, and the fuzzy information processing hardware system design at a low cost with only one kind of master slice (semicustom fuzzy logic IC) is described. These intrinsic fuzzy logic circuits have the following distinctive features; (1) Electrical characteristics are insensitive to wafer process parameters. (2) The circuits exhibit good linearity, robustness against the thermal and supply voltage fluctuations, and very high operation speed. (MIN and MAX circuits can normally operate with supply voltage of 4V ~ 8V under the temperature range of -55°C ~ +125°C and respond enough within 20 nsec.) (3) They don't need resistors nor isolation, etc. These circuits will be building blocks of "fuzzy computer". Finally, the prospect and situation of fuzzy hardware systems are discussed.

KEYWORDS

Fuzzy computer; current mode circuit; MOS current mirror; basic logic cell; post-binary machine; fuzzy integrated circuit; ratioless circuit; decimal computer; semicustom IC.

I. INTRODUCTION

Two-state operation of digital hardware systems based on boolean algebra naturally exhibits high noise immunity and low sensitivity to the variance of transistor characteristics used in the systems. This means the

robustness and extensibility of binary digital hardware systems. It is the reason why digital computers have been popularized nowadays.

Since the binary digital hardware systems are based on crisp sets, they are suitable for the exact calculations of large numbers and processing of deterministic informations, but not for the intuitive and/or synthetic decision making and processing of ambiguous informations.

Fuzzy sets and theory proposed by Prof. L. A. Zadeh admirably compensates for this weak point of binary systems (Zadeh, 1965). Various applications of fuzzy sets to engineering, medical science, civic science, social science and other fields have been proposed and realized. The applications up to the present are confined to utilizing digital computers in any case, because there are no other tools useful for fuzzy information processing. Generation of membership functions, and calculations of MAX, MIN, Summation, Division and other functions are executed with numbers 0.0 through 10.0 or so instead of 1.0. Although the fuzzy information processing employing a digital computer is useful for many purposes according to programming, it is not so effective with respect to the speed of processing, the power dissipation, the functional density, the design and fabrication cost and so on. Fuzzy reasoning with hundreds of fuzzy implications or rules in that manner is not easy to accomplish in the real-time mode. To be able to be used and to be suitable for use are different from each other. Fuzzy information processing requires exclusive hardware systems that deal with fuzzy signals but not binary signals.

II. WHAT IS DESIRED FOR FUZZY HARDWARE SYSTEMS?

In evaluating hardware systems we usually use the measures such as operating speed (response time), reliability, power dissipation, functional density, cost and so forth. Fuzzy reasoning, pattern recognition and other information processing require fast operations. Therefore, hardware systems should be considered from the viewpoint of the operation speed.

An usual digital computer consists of the CPU, its external memories and other peripheral devices organized with buses. The operation speed in this case is limited by the rate of data transfer through buses, but not by response times of logic gates involved in the CPU. Thus the system on chip rather than off chip is desirable for high speed operation.

Response times of a synaptic junction and a nerve fiber are much longer than binary logic gates which are typical building blocks in a binary digital computer. The information processing of the whole nervous system, however, exhibits much higher speed than that simulated by a digital computer. It is caused by the differences in the architecture, algorithm, operations of gates and so forth. When the hardware was very expensive, a stored-program concept proposed by John von Neumann was evaluated to be an excellent concept, because this concept produces simple hardware systems. The integrated circuit technology allows us to get complicated hardware systems at very low price in recent years. Therefore, we should adopt the parallel architecture for higher speed even at the sacrifice of system complexity.

The hardware system of parallel architecture is in need of much more

logic gates than that of von Neumann concept. An implementation of fuzzy logic with binary devices (switches) forces hardware designers to mount a large number of active devices and a large area of inter-connection region on the silicon chip, and results in higher power dissipation, lower yield (thus higher cost), lower functional density and some other demerits. Therefore, the electronic circuits peculiar to fuzzy logic gates should be designed on the basis of linear operation or an alternative but not binary operation (intrinsic fuzzy logic gates). Needless to say, fuzzy logic devices (not fuzzy logic circuits) will be the most suitable for fuzzy hardware systems, if possible.

Accordingly, the fuzzy information processing in parallel, on chip and by using exclusive fuzzy logic gates or fuzzy logic devices are desired for fuzzy hardware systems. The following sections describe nine basic fuzzy logic function circuits, which were designed in current mode to work in linear operation and consisted of much smaller amount of devices than those implemented with binary devices.

III. BASIC FUZZY LOGIC FUNCTIONS

Basic fuzzy logic functions are defined in terms of membership functions μ_X and μ_Y ($0 \leq \mu_X, \mu_Y \leq 1$) in the following, where $\vee, \wedge, +$ and $-$ denote max, min, algebraic sum and algebraic difference, respectively.

Bounded-Difference

$$\mu_X \ominus Y \triangleq 0 \vee (\mu_X - \mu_Y) \quad (1)$$

$$= \mu_X \ominus \mu_Y \quad (1')$$

Fuzzy Complement

$$\overline{\mu_X} \triangleq 1 - \mu_X \quad (2)$$

$$= 1 \ominus \mu_X \quad (2')$$

Bounded-Product

$$\mu_X \otimes Y \triangleq 0 \vee (\mu_X + \mu_Y - 1) \quad (3)$$

$$= (\mu_X + \mu_Y) \ominus 1 \quad (3')$$

Fuzzy Logic Union (MAX)

$$\mu_X \cup Y \triangleq \mu_X \vee \mu_Y \quad (4)$$

$$= (\mu_X \ominus \mu_Y) + \mu_Y \quad (4')$$

$$= (\mu_Y \ominus \mu_X) + \mu_X \quad (4'')$$

Bounded-Sum

$$\mu_X \oplus Y \triangleq 1 \wedge (\mu_X + \mu_Y) \quad (5)$$

$$= 1 \ominus (1 \ominus (\mu_X + \mu_Y)) \quad (5')$$

Fuzzy Logic Intersection (MIN)

$$\mu_X \cap Y \triangleq \mu_X \wedge \mu_Y \quad (6)$$

$$= \mu_X \ominus (\mu_X \ominus \mu_Y) \quad (6')$$

$$= \mu_Y \ominus (\mu_Y \ominus \mu_X) \quad (6'')$$

Implication

$$\mu_X \rightarrow Y \triangleq 1 \wedge (1 - \mu_X + \mu_Y) \quad (7)$$

$$= 1 \ominus (\mu_X \ominus \mu_Y) \quad (7')$$

Absolute-Difference

$$\mu |X - Y| \triangleq \begin{cases} \mu_X - \mu_Y & (\mu_X \geq \mu_Y) \\ \mu_Y - \mu_X & (\mu_X < \mu_Y) \end{cases} \quad (8)$$

$$= (\mu_X \ominus \mu_Y) + (\mu_Y \ominus \mu_X) \quad (8')$$

Equivalence

$$\mu_X \leftrightarrow Y \triangleq \mu_X \rightarrow Y \wedge \mu_Y \rightarrow X \quad (9)$$

$$= 1 \ominus ((\mu_X \ominus \mu_Y) + (\mu_Y \ominus \mu_X)) \quad (9')$$

All of the basic fuzzy logic functions presented here can be expressed only with the Bounded-Difference and the Algebraic Sum, as described above. Thus, each basic fuzzy logic function circuit is implemented with the Bounded-Difference circuit and the Algebraic Sum circuit.

In the current mode circuits, the Algebraic Sum is implemented only by connecting two lines to be summed (Wired Sum). Therefore, the Bounded-Difference arrays can be adapted to many kinds of fuzzy information processing hardware systems, the design of which should be directed only to wiring between the Bounded-Difference circuits (ie. basic logic cells).

IV. BASIC FUZZY LOGIC FUNCTION CIRCUITS AND MULTIPLE-FANOUT CIRCUIT EMPLOYING CURRENT MIRRORS

A current mirror necessary for constructing the Bounded-Difference circuit or the basic logic cell is implemented with bipolar transistors or MOS FETs.

A bipolar current mirror produces two types of significant errors.

One is caused by the base current or the finite forward current gain of transistors. Fig. 1 (a) illustrates its aspect. Assuming that the electrical characteristics of two transistors Q_1 and Q_2 are identical to each other, the input current I_i and the output current I_o are obtained from Fig. 1 (a) at a glance as

$$I_i = I_c + \frac{2}{\beta} I_c = I_c \left(1 + \frac{2}{\beta}\right) \quad (10)$$

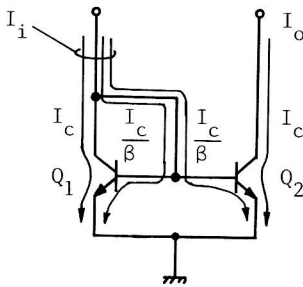
$$I_o = I_c \quad (11)$$

where β and I_c are the forward current gain and the collector current of Q_1 and Q_2 , respectively. Eqs. (10) and (11) give the current mirror factor (or current mirror ratio) G_I as follows.

$$G_I = \frac{I_o}{I_i} = \frac{I_c}{(1 + 2/\beta)I_c} = \frac{1}{(1 + 2/\beta)} \quad (12)$$

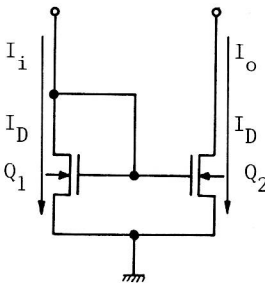
Eq. (12) shows that the current mirror factor G_I is exactly equal to unity only if $\beta = \infty$. However, in ordinary case of $\beta \approx 100$, G_I is obtained to be 0.98, and in case of the standard I^2L , the lower value of $\beta = 2 \sim 20$ (Möllmer and Müller, 1978; Flocke, 1978; Koopmans and van der Meij, 1982) inadequately gives $G_I \approx 0.5 \sim 0.9$. In contrast with the bipolar current mirror, a MOS current mirror has the input and output current paths separated, so that no error nominally appears as shown in Fig. 1 (b). The other error in bipolar current mirror is caused by the effect of saturation of one collector on the other collectors. It is shown in Fig. 2. The more collectors saturate, the more another collector current is reduced, while drain currents of a MOS current mirror are independent of each other. Since these significant errors are not permissible for fuzzy logic circuits, the multivalued I^2L family (Dao, McCluskey and Russell, 1977) is not suitable for fuzzy logic.

On the other hand, a MOS current mirror produces little error even in case of multiple output current mirror. Akiya and Nakashima (1984) presented a higher matching accuracy of a MOS current mirror with matching error of less than 0.5 % even in lower current regions and a smaller pattern area than similar bipolar current mirrors. Therefore, a MOS current mirror is adopted in this paper and represented as Fig. 1 (c) which is equivalent to Fig. 1 (b).



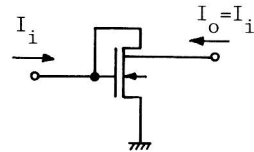
$$I_o = I_c = \frac{1}{1 + \frac{2}{\beta}} I_i$$

(a)



$$I_o = I_D = I_i$$

(b)



(c)

Fig. 1 (a) Current mirror circuit employing NPN transistors. (b) Current mirror circuit employing n-ch MOS FETs. (c) Symbol of n-MOS current mirror circuit.

The combination of this current mirror and the diode, which is easily obtained from an FET with gate connected to drain, give the basic logic cell shown in Fig. 3. It forms all of the basic fuzzy logic function circuits and thus the various complicated fuzzy hardware systems.

In Fig. 3, if the input current I_{i1} flows into the input terminal of the n-MOS current mirror, the same amount of current $I_D = I_{i1}$ flows into the output terminal of the current mirror. When $I_{i2} \geq I_{i1}$, the output current of the basic logic cell I_o is equal to $I_{i2} - I_{i1}$. When $I_{i2} < I_{i1}$, the output current I_o is equal to 0 A, because the reverse current is blocked by the diode D. Thus

$$I_o = \begin{cases} I_{i2} - I_{i1} & (I_{i2} \geq I_{i1}) \\ 0 & (I_{i2} < I_{i1}) \end{cases} \quad (13)$$

$$= 0 \vee (I_{i2} - I_{i1}) \quad (13')$$

The use of an FET of diode-connection D facilitates zero error operation under the conditions discussed later on (V.). In this circuit,

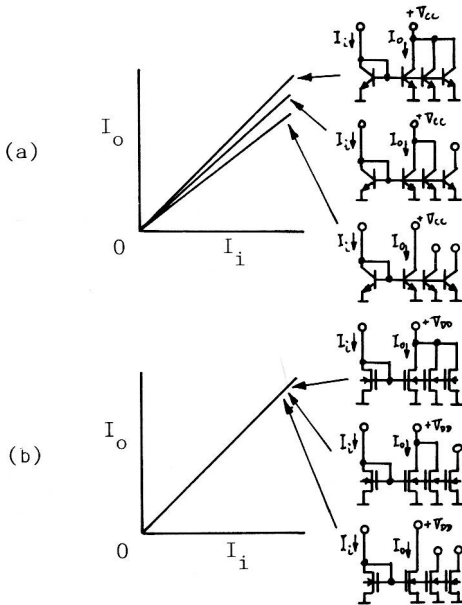


Fig. 2 Input-output characteristics of current mirrors implemented with (a) bipolar transistors and (b) MOS FETs.

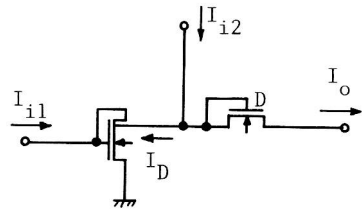


Fig. 3 Basic logic cell circuit.

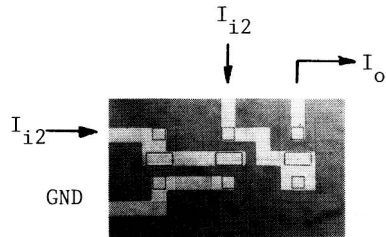


Fig. 4 Microphotograph of the basic logic cell.

TABLE 2 Functions of the Cascade-Connected Basic Logic Cells

Functions	Input			Output I_o
	I_{i1}	I_{i2}	I_{i3}	
Bounded-Sum	$\mu_X + \mu_Y$	1	1	$\mu_X \oplus Y = 1 \ominus (1 \ominus (\mu_X + \mu_Y))$
Intersection	μ_Y	μ_X	μ_X	$\mu_X \cap Y = \mu_X \ominus (\mu_X \ominus \mu_Y)$
Implication	μ_Y	μ_X	1	$\mu_X \rightarrow Y = 1 \ominus (\mu_X \ominus \mu_Y)$

Wired Sum of two basic logic cells gives us the Absolute-Difference circuit as shown in Fig. 7. The cascade connection of this Absolute-Difference circuit and the basic logic cell implements the Equivalence circuit as shown in Fig. 8. In this circuit, the diode D' can be eliminated, because the current flowing through the diode can not be negative.

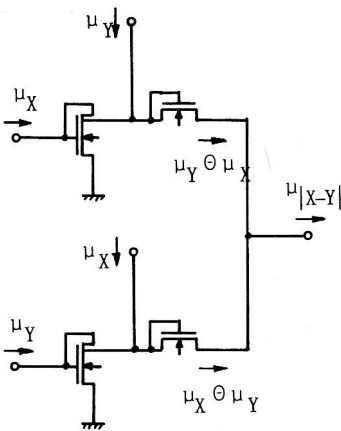
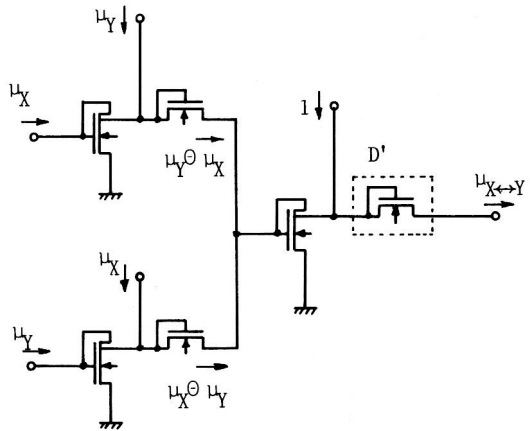


Fig. 7 Absolute-Difference circuit.

Fig. 8 Equivalence circuit. The diode D' can be eliminated.