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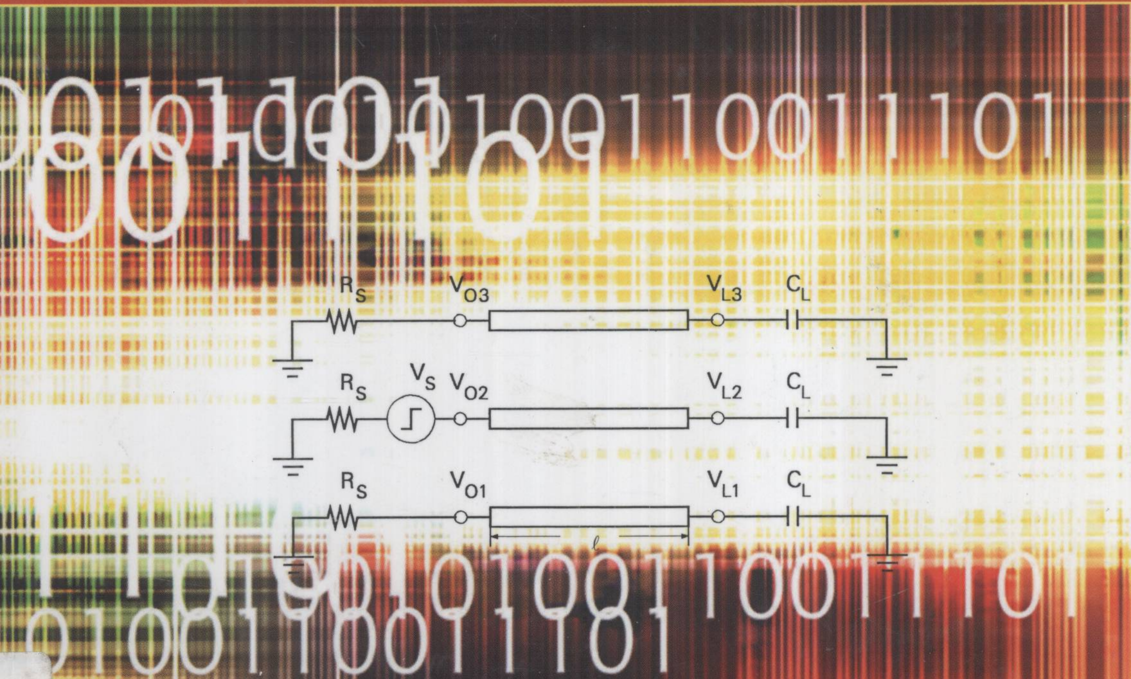
High-Speed VLSI Interconnections

Second Edition

Ashok K. Goel



Wiley Series in Microwave and Optical Engineering • Kai Chang, Series Editor

High-Speed VLSI Interconnections

Second Edition

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IEEE
IEEE PRESS

BICENTENNIAL
1807
WILEY
2007
BICENTENNIAL

WILEY-INTERSCIENCE
A JOHN WILEY & SONS, INC., PUBLICATION

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Published by John Wiley & Sons, Inc., Hoboken, New Jersey
Published simultaneously in Canada

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Wiley Bicentennial Logo: Richard J. Pacifico

Library of Congress Cataloging-in-Publication Data:

Goel, Ashok K., 1953-
High-speed VLSI interconnections / by Ashok K. Goel. – 2nd ed.
p. cm.
Includes bibliographical references.
ISBN 978-0-471-78046-5 (cloth)
1. Very high speed integrated circuits–Mathematical models. 2. Very high speed integrated circuits–Defects–Mathematical models. 3. Integrated circuits–Very large scale integration–Computer simulation. 4. Semiconductors–Junctions. I. Title.
TK7874.7.G63 2007
621.39′5–dc22

2007001710

Printed in the United States of America
10 9 8 7 6 5 4 3 2 1

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Preface

Continuous advances in very large scale integrated (VLSI) circuit technology have resulted in complex chips that have millions of interconnections that integrate the components on the integrated circuit (IC) chip. Customer demand for higher speeds and smaller chips has led to the use of interconnections in multilevel and multilayer configurations. At present, the interconnections play the most significant role in determining the size, power consumption, and clock frequency of a digital system. Parasitic capacitances, resistances, and inductances and their effects on the crosstalk and propagation delays associated with interconnections in high-density environments have become the major factors in the evolution of very high speed IC technology.

It has been over 10 years since the first edition of this book was published. During this period, several developments have taken place in the field of VLSI interconnections such as the introduction of copper interconnections for VLSI applications, realization of the importance of including inductances in the delay and crosstalk models for very high speed circuits, further research on optical interconnections, and the possibility of realizing nanotechnology ICs using nanowires, nanotubes, and wireless interconnections. An attempt has been made to include these developments in the present second edition.

This book focuses on the various issues associated with VLSI interconnections used for high-speed applications. These include parasitic capacitances and inductances, propagation delays, crosstalk, and electromigration-induced failure. It has been written as a textbook for a graduate-level course and as a reference book for practicing professionals who want to gain a better understanding of the several factors associated with high-speed interconnections. The reader is expected to have a basic understanding of electromagnetic wave propagation.

The chapters in this book are designed such that they can be read independently of one another while, at the same time, being parts of one coherent unit. To maintain independence among the chapters, some material has been intentionally repeated. Several appropriate exercises are provided at the end of each chapter which are designed to be challenging as well as help the student gain further insight into the contents of the chapter. The six chapters in this book can be described briefly as follows.

In Chapter 1, a few basic techniques and some advanced concepts regarding wave propagation in an interconnection are presented. Various types of interconnections employed in VLSI applications, including multilevel, multilayer, and multipath interconnections, are discussed. Advantages of copper interconnections and their fabrication techniques are reviewed. The method of images used to find the Green's function matrix is presented, and the method of moments, which can be used to determine the interconnection capacitances, is discussed. The even- and odd-mode capacitances for two and three coupled conductors are discussed, and the transmission line equations are derived. Miller's theorem, which can be used to uncouple the coupled interconnections, is presented. An efficient numerical inverse Laplace transformation technique is described. A resistive interconnection has been modeled as a ladder network. The various modes that can exist in a microstrip interconnection are described, and a quasi–transverse electromagnetic (TEM) analysis of slow-wave mode propagation in the interconnections is presented. The various measures of propagation delays, including delay time and rise time, are defined.

In Chapter 2, numerical techniques that can be used to determine the interconnection resistances, capacitances, and inductances on a high-density VLSI chip are discussed as well as the dependence of these parasitic elements on the various interconnection design parameters. Approximate formulas for calculating the parasitic capacitances for a few interconnection structures are presented. An algorithm to obtain the interconnection capacitances by the Green's function method, where the Green's function is calculated using the method of images, is presented. The Green's function is also calculated by using the Fourier integral approach, and a numerical technique to determine the capacitances for a multilevel interconnection structure in the Si–SiO_2 composite is presented. An improved network analog method to determine the parasitic capacitances and inductances associated with the high-density multilevel interconnections on the GaAs-based ICs is presented. Simplified formulas for the interconnection capacitances and inductances on the oxide-passivated silicon and semi-insulating gallium arsenide substrates are provided. A program called FastHenry, which can be used to determine the inductances associated with an interconnection structure, is described. A model for understanding the resistances for copper interconnections is presented. Source codes of a few computer programs to compute the parasitic capacitances and inductances are given in the appendices on the accompanying Ftp site. One of these programs has been extended to determine the electrode parasitic capacitances in a GaAs metal–semiconductor field effect transistor (MESFET).

In Chapter 3, numerical algorithms that can be used to calculate the propagation delays in the single and multilevel parallel and crossing interconnections are presented, and the dependence of the interconnection delays on the various interconnection design parameters is discussed. An analysis of interconnection delays on very high speed VLSI chips using a metal–insulator–semiconductor microstripline model is presented. A computer-efficient model based on the transmission line analysis of the high-density single-level interconnections on GaAs-based ICs is presented. The signal propagation in the single-, bi-, and trilevel high-density interconnections on GaAs-based ICs is studied, and a computer-efficient model of the propagation delays in the bilevel parallel and crossing interconnections on GaAs-based ICs is presented. A SPICE model for the lossless parallel interconnections modeled as multiple coupled microstrips is presented, and this model is extended to include lossy parallel and crossing interconnections. The high-frequency effects such as conductor loss, dielectric loss, skin effect, and frequency-dependent effective dielectric constant are studied for a microstrip interconnection. Compact expressions of propagation delays for the single and coupled interconnections modeled as *RC* and *RLC* circuits are provided. The active interconnections driven by several mechanisms are analyzed and a simplified model of the interconnection delays in multilayer ICs is presented. The source codes of a few computer programs used to determine the propagation delays in the normal and active interconnections are included in the appendices.

In Chapter 4, the mathematical algorithms which can be used to study the crosstalk effects in the single and multilevel parallel and crossing interconnections are discussed and the dependence of the crosstalk effects on the various interconnection design parameters is studied. Crosstalk among neighboring interconnections is calculated by using a lumped-capacitance approximation. Crosstalk in very high speed VLSI circuits is analyzed by using a coupled multiconductor metal–insulator–semiconductor microstripline model for the interconnections. Single-level interconnections are investigated by the frequency-domain modal analysis, and a transmission line model of the crosstalk effects in the single-, bi-, and trilevel high-density interconnections on the GaAs-based ICs is presented. This is followed by an analysis of the crossing bilevel interconnections on the GaAs-based ICs. Compact expressions for studying the crosstalk effects in the interconnections modeled as *RC* and *RLC* circuits are provided. The crosstalk effects in the multiconductor buses in the high-speed GaAs logic circuits are analyzed. The source codes of a few computer programs used to analyze the crosstalk effects are included in the appendices.

In Chapter 5, the degradation of the reliability of an interconnection due to electromigration is discussed. First, several factors related to electromigration in the VLSI interconnections are reviewed. The basic problems that cause electromigration are outlined, the mechanisms and dependence of electromigration on several factors are discussed, testing and monitoring techniques and guidelines are presented, and the methods of reducing electromigration in the VLSI interconnections are briefly discussed. Electromigration in copper interconnections is studied. The various models of IC reliability including the series model of failure mechanism in the VLSI interconnections are presented. A model of electromigration due to repetitive pulsed currents is developed. The series model has been used to analyze the electromigration-induced failure in the several VLSI interconnection components. The several computer programs available for studying electromigration in VLSI interconnections are discussed briefly. The source code of a computer program used to study electromigration-induced failure effects in the various interconnection components is included as an appendix.

In Chapter 6, a few interconnection technologies that seem promising for future ICs are discussed. The advantages, issues, and challenges associated with the optical interconnections are discussed and a lossy waveguide interconnection is modeled as a transmission line. The propagation characteristics and the comparison of superconducting interconnections with the normal metal interconnections are presented. Various technologies that seem promising for nanotechnology circuits, including nanowires, nanotubes, and quantum-cell-based wireless interconnections, are briefly discussed.

The appendices for this book containing source codes can be found at: **`ftp://ftp.wiley.com/public/sci_tech_med/high_speed_VLSI`.**

It should be noted that the various computer models presented in this book may not have been validated by experimental measurements and therefore should be used in computer-aided design programs with caution. In addition, the computer programs provided in the appendices are written for different computer systems and may need modifications to become suitable for the user's system. Finally, in the Internet-based information age, it is necessary to give references to certain websites. Though these websites were active at the time of preparation of this manuscript, it is possible that they may become inactive in the future.

ACKNOWLEDGMENTS

I would like to thank several individuals for their help and encouragement during the preparation of this book. I am grateful to Professor Kai Chang of Texas A&M University and editor of *Microwave and Optical Technology Letters* for inviting me to write this book. I am also thankful to Professor Martha Sloan of Michigan Technological University for her support. I also would like to thank my graduate students Yiren R. Huang, P. Joy Prabhakaran, Manish K. Mathur, Wei Xu, Matthew M. Leipnitz, and Jaikumar K. Parambil for their assistance with developing the computer programs and for obtaining the simulation results presented at several instances in this book. I am thankful to the Institute of Electrical and Electronics Engineers (United States) and the Institution of Electrical Engineers (United Kingdom) for their permission to use copyrighted material from over 30 papers published in *IEEE Transactions*, *IEE Proceedings*, and their other publications and I would like to take this opportunity to thank the authors of these papers whose work has been showcased in this book. I also owe special thanks to my wife, Sangita, for her constant love and encouragement. Finally, I express my deep appreciation to my son, Sumeet, and daughter, Rachna, for their patience and understanding during the preparation of this book.

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