Reliability and Degradation

Semiconductor Devices and Circuits

Edited by

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The Wiley Series in Solid State Devices and Circuits

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Microwave Devices

Variable Impedance Devices

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Reliability and Degradation

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Series Preface

The Oxford Dictionary defines the word revolution as 'a fundamental reconstruction'; these words fittingly describe the state of affairs in the electronic industry following the advent of solid state devices. This 'revolution', which has taken place during the past 25 years, was initiated by the discovery of the bipolar junction transistor in 1948. Since this first discovery there has been a worldwide effort in the search for new solid state devices and, although there have been many notable successes in this search, none have had the commercial impact which the transistor has had. Possibly no other device will have such an impact; but the commercial side of the electronics industry stands poised, awaiting the discovery of new devices as signicant perhaps as the transistor.

Research and development in the field of solid state devices has concerned itself with two important problems. On the one hand we have device physics, where the aim is to understand in terms of basic *physical concepts* the mode of operation of the various devices. In this way one seeks to optimize the technology in order to achieve the best performance from each device. The second aspect of this work is to consider the important contribution of the circuit to the operation of a device. This problem has been called *device circuit interaction*. It is a great pity that in the past these two major aspects of the one problem have been tackled by separate groups of scientists with little exchange of ideas. In recent years, however, this situation has been somewhat remedied, the improvement being due directly to the very rigorous system specifications demanded by industry. Such demands constantly require greater performance from devices, which can only be brought about by co-ordinated team work.

The objective of this new series of books is to bring together the two aspects of this problem: device physics and device circuit interactions. We hope to achieve, by coordinated co-authorship of leading experts in the respective fields, a varied and balanced review of past and current work. The books in this series will cover many aspects of device research and will deal

with both the commercially successful and the more speculative devices. Each volume will be an in-depth account of one or more devices centred on some common theme. The level of the text is designed to be suitable for the graduate student or research worker wishing to enter the field of research concerned. Basic physical concepts in semiconductors and elementary ideas in passive and active circuit theory will be assumed as a starting point.

University of Leeds
December 1980

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Preface

Since their conception solid-state semiconductor devices have always been regarded as having the potential of high reliability. This expectation was not diminished by the fact that early devices were characterized by lower lifetimes since it was quickly recognized that the sources of device failure were the result of the relatively primitive technology. Problems identified were poor crystal quality and undesirable chemical reactions between the metal–semiconductor and metal–metal interfaces which constitute major features of device structures. The exacting performance specifications impose great demands on the architecture of modern devices. Device structures are more complex, much smaller, may transport high current densities and in some cases may be expected to withstand high interfacial electric fields. Furthermore the device may have to operate at elevated temperatures.

Much of the early work on device reliability consisted of life testing and visual inspection of the degraded structures which provided semi-quantitative indirect evidence of possible degradation mechanisms. However, in recent years the development of a number of sophisticated near surface analytical techniques has shed new light on the physical processes involved. These techniques are discussed in detail in Chapter 1. Chapters 2 and 3 cover the basic interactions between metal films and silicon surfaces and between metal films and the two important III–V semiconductors GaAs and InP. Chapers 4 and 5 extend these studies to the degradation of Si, GaAs and InP device structures. The special cases of optoelectronic devices such as lasers and light emitting diodes are dealt with in Chapter 6 whilst the final chapter considers the increasingly important microwave integrated circuit.

The editors wish to thank most warmly the authors who have contributed to this volume and are particularly indebted to Dr. J. E. Davey (Naval Laboratory, Washington), Professor J. W. Mayer (Cornell University), Dr. J. Poate (Bell Laboratories), and J. Wood (ITT) for the valuable advice and constructive criticism.

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CHAPTER 1

Interactions of metal films on semiconductors

S. D. MUKHERJEE

1.1 INTRODUCTION

All semiconductor devices need electrical accessibility and therefore some form of metal contact is required. The contact may be rectifying or Ohmic, but the metals used are often unsuitable for making connections to the outside world. Invariably, therefore, layered metallizations are used for making the top metallic layer suitable for wire or tape ultrasonic–thermocompression bonding usually involving aluminium or gold, or soldering using lead–tin alloys.

When a device is fabricated, it goes through a number of processes[1,2] at the end of which it is metallized, passivated, encapsulated, or packaged or any combination of these. The device engineer knows the structure of the device which will include a number of semiconductor–metal, insulator–metal, and metal–metal interfaces. In order to ascertain the operational reliability of the device accelerated life-tests and pre-delivery burn-in or screening (or both) based on such life tests are often carried out. The stressing involves operating the device either at a higher temperature or current density in normal atmospheric, corrosive or highly irradiated environments, or in environments consisting of combinations of these.

The different interfaces in the device may change their characteristics through materials transfer by various means[3,4] at the different stages mentioned above. The interfacial changes and any resultant alterations in the bulk of the constituting materials invariably alter the electrical or mechanical performances (or both) of the device and the device is said to have degraded. More importantly, operation of the device at high power-levels or at high ambient temperatures for long periods of time reduces its useful life of operation as specified by the required electrical tolerances, while unnecessarily high stressing causes thermal runaway and device failure. It is therefore very important that the device engineer be aware of the various possible ways in

which the different interfaces alter themselves and the bulk materials that they separate, both during processing and the actual operations of the device in adverse conditions, and bears in mind the likely degradation or failure mechanisms caused by such interactions.

In this chapter we shall look into the fundamentals of these interactions. We shall also explore a number of macro- and microscopic analytical techniques used for studying them. In effect, we shall attempt to create a ground work necessary for the proper understanding of the in-depth reviews that appear later in this volume.

1.2 PROPERTIES OF THIN METALLIC LAYERS

1.2.1 Deposition techniques

Thin layers of metals can be deposited onto a semiconductor in a number of different ways,[5,6] the most important of which are:

(i) Thermal evaporation from a source heated resistively or by an electron beam.[5–7]
(ii) Molecular beam epitaxy—(MBE)[1,8] from Knudsen effusion sources, the process being similar in many respects to thermal evaporation.[9]
(iii) Sputtering from a large, planar metallic source[6,10] using non-reactive, high atomic weight gas-ions such as Ar^+, by DC–RF diode and triode cathodic sputtering,[5,6,11] magnetron sputtering, both planar[12–14] and cylindrical,[15] and large diameter ion-beam sputtering with[16] and without[17,18] ion neutralization facility.
(iv) Plating from aqueous solution,[5,6] electron assisted[19,20] and electroless.[21,22]
(v) Chemical vapour deposition (CVD) from an organometallic carrier gas,[6,23–27] deposited either pyrolitically or by chemical reactions.

Table 1.1 shows some relevant parameters of deposition techniques performed in vacuum.

Thermal evaporation from filaments or boats may involve vaporization from the liquid state, e.g., for Al, Au, Pd, Ni etc., while some metals, such as Ti, sublime from the solid state. Metals evaporated from the liquid state by resistive means are susceptible to bubbling and spitting which may degrade the uniformity of the deposited layer. Controlled heating by magnetically or electrostatically deflected electron beams reduce such problems.

For filament, boat or crucible evaporation, the melting point T_m limits the highest temperature achievable: Al_2O_3(2020 °C), BeO(2520 °C), Mo(2620 °C), Ta(2980 °C), W(3410 °C) and graphite (3700 °C). Appropriate metal–source combination is necessary. Al reacts with all refractory metals (W, Ta, Mo); Ti reacts with W but not with Ta, although Ta burns out before sufficient Ti vapour-pressure is generated; Au wets and reacts with Ta,

Table 1.1 Physical parameters associated with the different methods of metal depositions performed in vacuum

	Filament and boat evaporation	Molecular beam epitaxy	Electron beam evaporation	DC–RF sputtering	Planar magnetron sputtering
Chamber pressure (torr)	10^{-7}–10^{-5}	10^{-11}–10^{-8}	10^{-6}–10^{-5}	10^{-3}–10^{-1}	10^{-5}–10^{-2}
Deposition rate (nm min^{-1})	10–500	10–100	50–5000	20–200	20–5000
Ratio of gas to deposited atom collision rate on substrate	10^{-4}–10^{-2}	10^{-8}–10^{-5}	10^{-5}–10^{-2}	10–100	10^{-2}–1
Energy of deposited atoms on substrate (eV)	0.1–0.5	0.05–0.5	0.1–0.3	0.1–20	0.1–5
Irradiation of substrate by	IR and visible photons	IR and visible photons	X-rays, IR and visible photons, some ions as well	Electrons, UV and gas ions	UV photons and very few ions
Thermal loading of the substrate (W cm^{-2})	0.1–10	0.01	0.1–1.0	5–10	1
Substrate heating or cooling and temperature (°C)	Heated or cooled, 50°–300 °C	Temperature controlled 100°–700 °C	Heated, 200°–300 °C can be cooled in research units	Cooled, 50°–250 °C	Cooled or heated 50°–250 °C

but only partially wets W and Mo; Ni alloys with Mo, Ta, and W to form eutectics, but if Al_2O_3 coated W boats are used there is always the possibility of evaporating Al_2O_3 as well. BeO crucibles are better; but it is hard to evaporate Pt from filaments or boats.

In electron-beam evaporation, the charge (large lumps of high purity metals) is melted *in situ* inside a water-cooled copper crucible in high vacuum. Only the molten metal at the highest temperature, where the electron-beam strikes the melt, actually acts as an efficient evaporation source. The temperature diminishes radially and since the copper crucible is cooled, no mass transfer takes place there. In this way any metal can be evaporated easily and in a controlled fashion, with no contamination from the container.

In DC and RF sputtering a negative potential is developed on the metal target plate by directly coupled DC or capacitatively coupled RF sources, and a plasma is generated in the low pressure argon atmosphere. Ar^+ ions bombard the plate, dislodge metal atoms by kinetic energy transfer, which are deposited onto the facing substrate kept at ground or slightly positive potential. Electrons and some Ar^- ions bombard the substrate and so do energetic metallic ions, increasing the substrate temperature[28] and damaging electrically active layers up to a depth of 10 nm. As a result Schottky barrier height and other characteristics on GaAs are adversely affected.[29,30]

In magnetron sputtering a crossed magnetic field compels the electrons to move in cycloidal paths, increasing gas ionization probability and nearly eliminating electron bombardment of the substrate. This not only reduces the operating pressure providing a 'clean' environment, but also allows the sputtering to be used in Si–MOS technology reducing charge trapping on SiO_2. Sputtering at not very low pressures often causes gas occlusion in deposited metals that may result in porosity.[31]. Ion beam sputtering can be achieved in a differentially pumped deposition chamber operating at a much lower pressure, ensuring even cleaner environment. In all these physical deposition processes, where atoms are stripped off their neighbours in a solid state, part of the substrate heating is caused by the latent heat of condensation of these atoms[28] (cohesive energy), which on principle, cannot be eliminated.

Although it is generally believed that plating from solutions invariably incorporates impurities in the metal film, this is not so in every case. In well controlled aqueous environment less than 100 or 10 ppm or impurities can be achieved.[19] These figures are, at times, better than similar figures for physical vapour deposited layers. In plating, as well as in CVD, non-metallic atoms that are part of the electrolyte or the carrier gas may be deposited as well. For example electroless deposited Ni[22] and CVD Pt[23] may contain phosphorus while CVD Cr[24] and Ti[27] often have carbon as impurities. In some cases such impurities may be useful, e.g. for making a stuffed diffusion barrier (Section 2.5.3). Electroplating has been used for Schottky barrier diodes (SBDs)[32] and is currently used extensively for Au and Ag heat sinking of high power devices, such as IMPATTs,[33,34] TRAPATTs and TEDs (Gunn diodes).

1.2.2 Grain size and epitaxiality: grain boundary structure

Three types of solid surfaces exist: crystalline (e.g. (100) and (111) Si and (110) GaAs), polycrystalline (e.g polycrystalline silicon and metallic layers, SiO_2 and Si_3N_4) and amorphous (e.g. fused quartz, borosilicate, and phosphosilicate glasses and amorphized metal or semiconductor) and we need to deposit metals on all these surfaces for different applications. Solid state interactions are strongly dependent upon the structures of both the interface and the dissimiliar solids on the two sides of this interface. We therefore set out to find what the structure of the deposited metal is going to be like.

When a metal is deposited on a low Miller index plane on a crystalline material, oriented growth (heteroepitaxy) may occur if the misfit $\leqslant 7\%$. The misfit is defined as $100(b - a)/a$ per cent where a is the lattice parameter of the semiconductor and b, the network spacing of the metal which is some multiple of its lattice parameter that allows parallel matching of two major crystal planes of the metal and the semiconductor.[35] Such epitaxy occurs due to the lowering of interfacial potential energy when atoms on either side fall into the periodic potential wells caused by the crystallinity of the other, with that of the substrate playing the decisive role since it is thicker.[36] Any misfit in a and b can be accommodated in two ways. Firstly by the generation of strain. When the deposited layer is very thin, such as a few monolayers, the substrate forces the area of the basal plane to decrease (or increase) with a corresponding elongation (or compression) of the lattice in a vertical direction to maintain unit cell volume. This is called 'pseudomorphism' and the phenomenon is responsible for heteroepitaxy, even when misfit >10 or 20 per cent, for a larger number of cases.[37] Secondly, for thicker layers pseudomorphism cannot be maintained and the strain caused by mis-registration is reduced through the formation of narrow stripes of poor-fit, called interfacial 'misfit dislocations'[35] because of their close analogy with crystal dislocations. For a start these misfit dislocations form closed loops starting from and ending on the interface. Often they climb up to meet the free surface and threading dislocations are produced. Heteroepitaxial layers usually have high dislocation densities, 10^9 to 10^{10} cm^{-2}, i.e. at least one dislocation for every 0.1 to 1 μm of traverse on the surface.

Growth often follows a layer by layer or islands on a layer sequence when the surface energy (or the surface tension) of the deposit is very much lower than that of the substrate and when the substrate temperature during deposition is high.[38–40] If the converse is true or if misfit $\leqslant$ 7–10 per cent, individually nucleated islands are formed first. These move and enlarge in size and may coalesce to form a single crystal layer when misfit $\leqslant 7$ per cent at a high enough temperature, with threading misfit dislocations forming at or near the coalescing side faces. Or, at intermediate temperatures, for misfit <7 per cent, nucleated single crystal islands coalesce to form a texturized film having grains with a common low Miller index axis normal to the surface by being

joined to one another side by side by low or medium angle grain boundaries. Alternatively, they form a polycrystalline layer when misfit >7 to 10 per cent and at lower temperatures with high or low angle grain boundaries separating the coalesced islands. Subsequent deposition may increase the sizes of these crystallites in a vertical direction following homoepitaxy giving rise to columnar growth, or new crystallites are formed and a layer is produced with grain sizes smaller than its thickness.

In most practical cases metals are deposited onto crystalline semiconductors at temperatures much lower than that necessary for creating epilayers for fear of interfacial reactions or device or equipment constraints or both. As a result the film has a polycrystalline structure and the higher the melting point of the metal the smaller the grain size in the film.[41] Dislocation densities in these polycrystals are high, 10^9–10^{12} cm^{-2}, i.e. even 100–500 nm^2 diameter grains have at least one threading dislocation in them.

Metal epitaxy on useful semiconductors has been observed in a number of cases,[42–44] a few of the earlier cases being: Ag and Ni on (111) Si by MBE; Co, Ni, and Ag on (111) Si by evaporation; Ge on (111) and (001) Si by MBE, CVD and evaporation; Ag and Pt on (111) Si by sputtering; Ag on (001) Si by MBE; Al on (001), (110) and (111) GaAs by MBE; Zn on (001) and (111) GaAs by MBE (but Zn is a dopant); Ge on (001), (110), and (111) GaAs by MBE, CVD, LPE and evaporation; Ag on (001) and (110) GaAs by MBE and Fe on (100) GaAs by evaporation.[44] This partial list has been increased considerably in recent years.

The rise in surface temperature during sputtering in a plasma hinders rather than facilitates epitaxial growth. This is because most of the energy is deposited as kinetic energy of the incoming energetic metal atoms and ions and a few gas ions, and it disrupts the small crystallites. Therefore, not only are sputtered epitaxial layers rare but also grain size becomes much smaller than in an evaporated film, and especially so if adsorbed gases are occluded in its structure.[31a] Controlled ion-beam sputtering under UHV conditions, however, makes epitaxy possible.[31b]

Plating on the other hand, invariably creates large, faceted grains of crystallite and it is necessary for structural uniformity to reduce grain size by agitation, lower current density and higher solution temperature. Plating is often initiated from a vacuum deposited thin layer of the same metal. Homoepitaxial grain growth is the starting point and the grains become larger with increasing thickness.

In some cases epitaxial growth is also possible on amorphous[45] or liquid surfaces.[46] If the interaction of the deposit with the substrate is weak, the crystal orientation is decided by nucleation facilitated by cohesive energy, e.g. (111) Si on SiO_2. In this case thermal activation is essential. If, on the other hand, surface-atom interaction is strong, initial orientation follows the short range order of the amorphous body and growth occurs accordingly, e.g. vari-