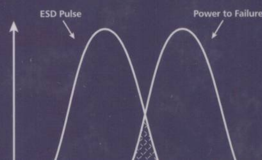
ESD

FAILURE MECHANISMS AND MODELS

STEVEN H. VOLDMAN



TN304.07
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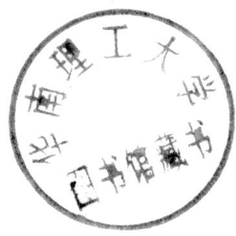

A John Wiley and Sons, Ltd, Publication

This edition first published 2009
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John Wiley & Sons Ltd, The Atrium, Southern Gate, Chichester, West Sussex, PO19 8SQ, United Kingdom

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Library of Congress Cataloging-in-Publication Data

Voldman, Steven H.
ESD : failure mechanisms and models / Steven H. Voldman.
p. cm.
Includes bibliographical references and index.
ISBN 978-0-470-51137-4 (cloth)
1. Semiconductors–Failures. 2. Integrated circuits–Protection.
3. Integrated circuits–Testing. 4. Integrated circuits–Reliability.
5. Electric discharges. 6. Electrostatics. I. Title. II. Title: Electrostatic discharge.
TK7871.852.V65 2009
621.381–dc22

2009015206

A catalogue record for this book is available from the British Library.

ISBN: 978-0-470-51137-4 (H/B)

Typeset in 10/12pt Times by Thomson Digital, Noida, India.
Printed in Great Britain by CPI Antony Rowe, Chippenham, Wiltshire.

ESD

To My Son
Aaron Samuel Voldman
On His Year of Graduation
from Brandeis University 2009

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About the Author

Steven H. Voldman is a recipient of the IEEE Fellow for "Contributions in ESD Protection in CMOS, Silicon On Insulator and Silicon Germanium Technology" in 2003, and the ESD Association Outstanding Achievement Award, in 2007. He has a B.S. in engineering science from the University of Buffalo (1979); a first M.S. EE (1981) from Massachusetts Institute of Technology (MIT); a second EE degree (Engineer Degree) from MIT; an M.S. in engineering physics (1986) and a Ph.D. EE (1991) from the University of Vermont under IBM's Resident Study Fellow program.

Dr. Voldman was Chairman of the SEMATECH ESD Working Group from 1995 to 2000, to establish a national strategy for ESD in the United States. He was also the first ESD Association Technology Roadmap Chairman. He has served as an ESD Association Board of Director (2000–2006, 2008–2011) and an Appointed ESDA Board of Director (2006–2007). He has been an ESD Symposium Technical Program Chairman, Vice Chairman, and General Chairman from 2000 to 2002, presently serving as the ESD Symposium Vice Chairman (2008), and General Chairman (2009). In the ESD Association Device Standards Development, he has served on the HBM, MM, CDM, TLP, VF-TLP, CDE, and HMM Work Groups. He has been the ESDA Chairman of the TLP Standard Committee which developed both the TLP and VF-TLP standard practice documents, released in 2004 and 2008, respectively. He presently serves on the ESDA Standard Committee body and the ESDA Education Committee, and is an ESD Threshold Magazine Associate Editor and member of the ESD Technology Roadmap team.

Dr. Voldman has provided tutorials on ESD failure mechanisms to the International Reliability Physics Symposium (IRPS), the EOS/ESD Symposium, the Taiwan ESD (T-ESD) Conference, and the International Physical and Failure Analysis (IPFA) Symposium. Additionally, he has provided tutorials to industrial tutorial programs, as well as foundries such as Chartered Semiconductor, Tower Semiconductor, and Taiwan Semiconductor Manufacturing Corporation (TSMC).

Dr. Voldman established the "ESD on Campus" program to bring ESD lectures and interaction to university faculty and students in the United States, Europe, Taiwan, Singapore, Malaysia, Philippines, China, and Thailand, including the MIT Lecture Series, Stanford University, University of Vermont, University of Illinois Urbana–Champaign, University of Wisconsin Milwaukee, University of Central Florida, University of Buffalo, Nanyang Technical University, National University of Singapore, Chulalongkorn University, Kasetsart

University, Thammasat University, Mahanakorn University, National Taiwan University, National Taiwan University of Science and Technology, National Chiao-Tung University, National Tsing Hua University, Zheijang University, Shanghai Jiao-Tong University, Fudan University, Beijing University, Mapua Institute of Technology, and Universiti Sains Malaysia.

Dr. Voldman provided ESD and latchup support for IBM between 1982 and 2007 working with CMOS, SOI, RF CMOS, and silicon germanium technology. In 2007, he joined Qimonda, working on ESD protection in 90, 65, and 45 nm technology products. In 2008, he formed a limited liability corporation (LLC), providing ESD foundry support to Taiwan Semiconductor Manufacturing Corporation (TSMC). In 2009, he is a Senior Principal Engineer at the Intersil Corporation working on ESD and latchup in digital, analog and power applications.

Dr. Voldman has written over 150 technical papers from 1982 to 2008. He is a recipient of over 185 issued US patents in the area of ESD and CMOS latchup. He was recognized as an IBM Corporate Top Inventor from 2000 to 2002, and received the IBM Master Inventor Award in 2006. He also has presented tutorials internationally on innovation, inventing, and patenting. He has served as an expert witness and provided litigation support work in the area of ESD protection and latchup.

Dr. Voldman is an author of the John Wiley & Sons ESD book series – the first book, *ESD: Physics and Devices*; the second book, *ESD: Circuits and Devices*; the third book *ESD: RF Technology and Circuits*; and a fourth book, a companion text, *Latchup*. He is also a contributor to the book *Silicon Germanium: Technology, Modeling and Design*.

Preface

ESD: Failure Mechanisms and Models is targeted at an audience of the failure analysis technician and engineer, the semiconductor process and device design engineer, the circuit designer, the test engineer, and the ESD engineer. In this text, a balance is established between the "failures" and the "fixes."

A first goal of this book is to teach the ESD failure mechanisms and physical models that occur in semiconductors and nanostructure technologies from a generalist perspective. This will be followed by specific failure mechanisms observed in the different technologies and circuits.

A second goal is to teach the methodology and basic failure analysis as an ESD design practice. From the failure mechanisms, the understanding of the root cause can be obtained. In addition, ESD failure analysis allows for the understanding of the fundamental practices of ESD design and the ESD design discipline.

A third goal is to present ESD failure mechanisms relevant to many of today's technologies. The text will discuss ESD failure mechanisms in "old" technology as well as updating the modifications to the present-day state-of-the-art technologies. The text will cover a wide spectrum of technologies from CMOS, RF CMOS, silicon-on-insulator (SOI), smart power, gallium arsenide (GaAs), magneto-resistive (MR) heads, tunneling magneto-resistive (TMR) heads, micro-electromechanical (MEM) systems, to photo-masks and reticles.

A fourth goal is to not only identify the failure mechanism, but use it as an opportunity to learn about the component under test. Using the failure mechanism, it is possible to determine current paths, internal device current distribution, temperature distribution, power distribution, device operation, and other features. Hence, a key objective of the text is to start with the discovery of the failure, and then use this as a starting point of the analysis, using the failure point as the first step in the analysis to determine many other features of the semiconductor chip.

A fifth goal is to teach how to build more ESD and EOS robust components and systems. As stated above, the discovery is the first step of the failure analysis, not the last step. If pursued in that fashion, we can learn how to build better components. This involves understanding the interrelationship between the failure mechanism, the layout design, the physics of failure, the characterization, the test, and the failure criteria. From this understanding of the failure mechanisms, and materials, it is possible to design better ESD structures, better I/O circuitry, and more robust systems.

A sixth goal is to demonstrate new failure analysis techniques, and tools, and how to use them for ESD and latchup evaluation. In the last 20 years, a significant number of failure analysis techniques and tools were developed which have been utilized to understand and quantify CMOS ESD and latchup; these tools include EMMI, AFM, KPFM, CCD, SQUID, EBIC, OBIC, OBIRCH, TIVA, CIVA, PICA, and TLP-PICA. With these advancements in the field of failure analysis, new issues in ESD and latchup can be visualized spatially and temporally.

A seventh goal is to expose the reader's knowledge of ESD failures and mechanisms. There is significant focus on CMOS, and not enough on RF CMOS, SOI, GaAs, GaN, InGaAs, smart power, and MEMs. In many of the technical publications, ESD engineers do not talk about the product case studies and only discuss the measurements of the ESD device; this misleads faculty members and students.

ESD: Failure Mechanisms and Models contains the following:

- Chapter 1 introduces the reader to the fundamentals and concepts of ESD failure analysis (FA). In this chapter, we open the discussion of the uniqueness of the ESD FA methodology. Then we discuss concepts of definition of failure: why do micro-electronic devices fail; and what is a failure? The chapter focus also includes how to use FA to build better semiconductor chips. The chapter talks about the ability to use FA to determine the current distribution, the current paths, the temperature in a semiconductor device, and device operation.

- Chapter 2 reviews the basics of FA tools, electro-thermal models, and ESD models. The chapter provides a brief discussion of FA tools used for ESD analysis. The discussion reviews established models and new models such as the transmission line pulse (TLP), very fast TLP (VF-TLP), cable discharge event (CDE), and human metal model (HMM), the charged cassette model, the charged board model, and ultra-fast transmission line pulse (UF-TLP). The chapter discusses the electro-thermal failure models and failure from the statistical approach used, using distribution functions and probability theory.

- Chapter 3 begins by discussing failure mechanisms for CMOS technology. This chapter discusses failures in resistors, diodes, and MOSFETs. In this discussion, the technology scaling from 2.0 μm to 32 nm CMOS technology is presented. In this fashion, the evolution of CMOS technology can be observed and how it influenced the failure mechanisms of the technology generation.

- Chapter 4 discusses failure mechanisms associated with CMOS peripheral circuits. In this chapter, we explore both receivers and off-chip driver (OCD) networks. Mostly, we focus on receiver networks. In the discussion, the current paths and failure mechanisms are described. By learning all the different receiver failure mechanisms, the understanding can be transferred to other circuits and peripheral devices.

- Chapter 5 discusses failure mechanisms associated with chip architecture and design synthesis. In this chapter, unique failure mechanisms typically not discussed in publications are presented. These include power grid issues, generators and regulators, digital–analog integration issues, decoupling capacitors, fuse networks, anti-fuse networks, eFUSE networks, no connect pins, and floating pads. The chapter also discusses multi-chip environments; this topic addresses concerns of "bare-die," system-on-chip, silicon carriers, and stacked chip ESD issues.

- Chapter 6 focuses on silicon-on-insulator (SOI) technology. The chapter discusses the device issues and design integration concerns in partially depleted to fully depleted SOI. This chapter focuses on how the SOI failure mechanisms differ from the bulk CMOS failure mechanisms. In the discussion, SOI technology scaling from the 2.0 μm to 32 nm CMOS technology is described.
- Chapter 7 discusses the failure mechanisms of radio frequency (RF) CMOS. In this chapter, we focus on the failure mechanisms associated with the passive elements, and how the failures manifest themselves in the different circuit topologies.
- Chapter 8 addresses micro-electromechanical (MEM) structures. With the growth of interest in MEM technology, the understanding of the failure mechanisms is key to the future of MEMs in space, military, and mainstream applications. This chapter highlights the new failure mechanisms being discovered from ratcheted motors to RF MEM switches.
- Chapter 9 discusses III–V compound devices with a focus on gallium-based devices. The chapter covers gallium arsenide, gallium nitride (GaN) LEDs, and indium gallium nitride devices. ESD solutions for these technologies will be reviewed from on-chip to off-chip solutions.
- Chapter 10 discusses smart power and LDMOS technology failure mechanisms. LDMOS technology has unique ESD and latchup issues. This chapter provides a brief introduction to some of the issues associated with high voltage CMOS, LDMOS structures, and bipolar–CMOS–DMOS (BCD) technology.
- Chapter 11 discusses magnetic recording failure mechanisms. This chapter discusses failures in magneto-resistor (MR) recording heads, and inductive heads. Additionally, giant magneto-resistor (GMR) and tunneling magneto-resistor (TMR) devices are also discussed. Additionally, the ESD design and manufacturing solutions that are applied to the magnetic recording industry are presented.
- Chapter 12 discusses failures in photo-masks, and reticles. Manufacturing solutions to avoid ESD issues in photo-masks are reviewed. ESD failure images are shown of photo-masks in the manufacturing environment.

Hopefully this text will teach engineers the mechanisms associated with the technologies. In addition, the underlying ESD FA discipline will be illuminated for the readers and will help them explore new devices and technologies in the nano-electronic era.

Enjoy the book, and enjoy the subject of ESD.

Steven H. Voldman
IEEE Fellow

Acknowledgments

I would like to thank the individuals who have helped me on the Right Path in my academic and professional career. I would like to thank the institutions that allowed me to teach and lecture at conferences, symposiums, industrial events, and universities. I would like to thank for their years of support and the opportunity to provide lectures, invited talks, and tutorials on ESD: the International Physical and Failure Analysis (IPFA) Symposium in Singapore, the Electrical Overstress/Electrostatic Discharge (EOS/ESD) Symposium, the International Reliability Physics Symposium (IRPS), the Taiwan Electrostatic Discharge Conference (T-ESDC), the International Conference Symposium on Integrated Circuits and Technology (ICSICT), as well as the ESD Association Education Committee. I would also like to thank the members of the International Physical and Failure Analysis (IPFA) Symposium for inviting me to provide tutorials on ESD failure mechanisms. I would like to thank the ESD Association for the development of ESD tutorials on failure mechanisms and models. As part of the ESD on Campus lecture series, I would like to thank the following universities and faculty for allowing me to lecture on ESD: Massachusetts Institute of Technology (MIT), University of Illinois Urbana–Champaign (UIUC), University of Wisconsin Milwaukee (UWM), University of Arizona (U of A), University of Buffalo (UB), University of Vermont (UVM), University of Central Florida (UCF), Chulalongkorn University (Thailand), Mahanakorn University (Thailand), Kasetsart University (Thailand), Thammasat University (Thailand), Mapua Institute of Technology (MIT) (Manila, Philippines), National Chiao-Tung University (NCTU) (Hsinchu, Taiwan), National Taiwan University (NTU) (Taipei, Taiwan), National Taiwan University of Science and Technology (NTUST) (Taipei, Taiwan), National Tsing Hua University (NTHU) (Hsinchu, Taiwan), Nanyang Technical University (NTU, Singapore), Fudan University (Shanghai, China), Shanghai Jiao-Tung University (Shanghai, China), Zheijang University (Hangzhou, China), and Beijing University.

I would like to thank authors who provided contributions to the text: namely, Professors Augusto Tazzoli and Gaudenzio Meneghesso from University of Padova, Italy for MEMs and GaAs ESD failure mechanisms; Sandeep Sangameswaran of IMEC for RF micro-mirror failure mechanisms; Julian A. Montoya of Intel Corporation and Larry Levit for photo-mask failure mechanisms; Albert Wallash of Hitachi Corporation for ESD failure mechanisms in magnetic recording devices; Tze Wee Chen and Professor Robert Dutton of Stanford University for UF-TLP related failure mechanisms; Shu Qing Cao of Stanford University for SOI failure data; Teruo Suzuki of Fujitsu Corporation and Koen Verhaege of Sarnoff

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Europe for fill shape failure mechanisms; Chiharu Nozaki of Toshiba Corporation for PHEMT failure mechanism; Swami Muthukrishnan and Nathan Peachey for PHEMT failure mechanisms; Peter Zampardi of Skyworks for ESD failure in MIM capacitors; Jeremy Walraven of Sandia Laboratories for ratcheted micro-motors; Don Ming Fang of Beijing University for RF spiral inductors; Franco Stellari and Al Weger of IBM for latchup analysis; and lastly, Pee Ya Tan and Sherry Khoo of Chartered Semiconductor Inc. for the TEM diffraction pattern analysis.

In the evaluation of ESD failures, I would like to thank the failure analysis teams of Taiwan Semiconductor Manufacturing Corporation, Qimonda, Chartered Semiconductor, and IBM Corporation. I would also like to thank the failure analysis teams that I have worked with over the years: James Never, Orison J. Cain, Peter Czahor, Ted Regula, Phil Kaszuba, Leon Moskowitz, Marsha Abramo, Tammy Vogel, Theodore Levin, Gregg Nuttal, Woody Bowe, David Vallett, and Richard Ross. For the atomic force microscope (AFM) work, I would like to thank James R. Slinkman, Phil Kaszuba, and James Never. For the picosecond current analysis (PICA) tool, I would like to thank the IBM Thomas J. Watson Yorktown Heights research team for co-development of the TLP-PICA technique: Pia N. Sanda, Alan Weger, Franco Stellari, and Myra McManus. For co-development of the electro-thermal device simulation tool FIELDAY III and its utilization for ESD failure analysis, I would like to thank Stephen Furkay, and David Sheridan.

I would like to thank the ESD Association office for support in the area of publications, standards developments, and conference activities, with special thanks to Lisa Pimpinella. I would also like to thank the support from Roy and Becky Walker and the entire committee of the International Reliability Physics Symposium (IRPS), the Taiwan ESD Conference, and the International Physical and Failure Analysis (IPFA) Symposium team.

I would also like to thank the publisher and staff of John Wiley & Sons, for including *ESD: Failure Mechanisms and Models* as part of the ESD book series.

And most important. . . To my children, Rachel Pesha Voldman and Aaron Samuel Voldman, and my wife Annie Brown Voldman, for support, for keeping our lives going forward, and for keeping our lives on the Right Path. And of course, my loving parents Carl and Blossom Voldman.

For this text, I would like to congratulate my son, Aaron, for his effort in Youth for America, Democracy for America (DFA), Brandeis for Democracy, the Student Peace Alliance (SPA), the Peace Alliance, and the US Department of Peace. Good luck in Washington, DC, in 2009 at the US Department of Peace office.

Baruch Hashem (B"H)
Steven H. Voldman
IEEE Fellow

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