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EDITORS:

William L. Warren

Roderick A.B. Devine

Masakiyo Matsumura

Sorin Cristoloveanu

Yoshio Homma

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Amorphous and Crystalline Insulating Thin Films—1996

PREFACE

Symposium K, "Amorphous and Crystalline Insulating Thin Films—1996", from the 1996 MRS Fall Meeting, is the fourth in a series devoted to the continuing research and development of thin dielectric films for optical and microelectronic applications. The first was held during the 1992 MRS Fall Meeting in Boston, MA, and the second during the 1994 EMRS Spring Meeting in Strasbourg, France. The third was conducted under the auspices of the Solid State Devices and Materials Conference in Osaka, Japan, during the summer of 1995.

Of the 85 papers presented at this symposium, 51 were oral (of which eight were invited) and 34 were posters. Over 10 countries were represented (48 from the United States, 10 from Western Europe, 22 from Japan, China and Korea, and five from Eastern Europe). Thirty-eight papers originated from universities, 28 from industrial laboratories and 19 from national research laboratories. Judging from previous symposia, the materials research being performed on dielectric thin films from the industrial sector is rising.

The technical program was divided into the following sessions: thin SiO_2-based dielectrics, silicon oxynitride, low-dielectric constant and organic dielectrics, high-dielectric constant materials, SiO_2 growth and properties, and silicon-on-insulator (SOI) materials.

The session on ultra-thin oxides dealt with topics ranging from the effects of the enhanced performance of deuterated oxides, the fabrication of hydrogen-free oxides and the effects of differing gate electrodes, to the effects of post-metallization annealing of these dielectrics. It appears that much of what was learned on thicker SiO_2 films may not necessarily be transferable to the ultra-thin regime (< 5 nm).

Although thermal SiO_2 has been the dominant dielectric for thin films in microelectronic applications, there is an immense need for low-dielectric constant materials for interlevel dielectrics (less capacitive cross-talk and reduced delay) and high-dielectric constant materials to minimize the space and maximize the capacitance of storage devices such as DRAMs. The sessions devoted to these topics showed that materials such as Ta_2O_5, $BaTiO_3$, $(Sr,Ba)TiO_3$, $Pb(Zr,Ti)O_3$ and $SrBi_2Ta_2O_9$ dielectrics are maturing at a fantastic rate. Some of the biggest breakthroughs have been in processing integration of these complex oxides into standard Si CMOS processing lines, as well as the improved reliability of these materials largely due to electrode technology and materials growth. The development in this field has been primarily industry-driven.

Two sessions dealt with the structure, characterization, and devices built from SOI materials formed by either the Smart Cut Unibond® process or by the O^+ implantation into Si substrates (SIMOX process). These techniques have come to fruition as viable methods for producing commercial devices that require radiation hardness and high-temperature or high-speed operation.

Oxygen vacancies still appear to be a thorn in the flesh in terms of buried oxide reliability. Nonetheless, it turns out that thanks to these defects, SOI materials may have some unique properties and applications.

For the first time we introduced a tutorial on SOI materials analysis, device operation and characterization techniques. The course was extremely well attended and was a great success.

The success of this symposium was a result of the support and contributions from various participants, as well as from that of our sponsors, Nippon Electric Company, SOITEC USA, and Hitachi Ltd.

William L. Warren
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February 1997

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Part I

Thin Oxides

Gate Electrode Effects on Dielectric Breakdown of SiO_2

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ABSTRACT

We discuss the gate electrode effects on SiO_2 degradation in MOS structures. The gate electrode material was poly-silicon, but the impurity doping procedure was varied in terms of species and concentrations. First, the origin of the substrate hole current observed in n-MOSFETs, by injecting electrons from the silicon substrate, is discussed in terms of oxide thickness and gate electrode doping species, because the dielectric breakdown is closely related to the total hole fluence in the oxide. The effects of the gate electrode on the oxide network structure and on the Si/SiO_2 interface are also experimentally investigated. Finally, the experimental results obtained for Qbd of different gate electrode MOSFETs are shown, including the polarity dependence of Qbd. Furthermore, the percolation analysis to explain the polarity dependence is introduced, since the dielectric breakdown process is really stochastic.

INTRODUCTION

The SiO_2 reliability is a main concern from the viewpoints of MOSFET miniaturization and future ULSI performance, as long as MOS devices continue to be employed in electronic devices. Nowadays, the SiO_2 thickness in advanced MOSFETs is approaching the direct tunneling limit. In fact, 1.5 nm gate oxide MOSFET has already been reported [1]. In such thin oxide MOS devices, it should be taken into consideration how the gate electrode and silicon substrate as well as the oxide itself affect the dielectric breakdown, charge trapping, and interface states generation of SiO_2. It is reported that the substrate defects or oxygen precipitates degrade breakdown characteristics due to random failure. On the other hand, the gate electrode effects have not been intensively investigated from the viewpoint of oxide reliability [2]. This is surprising since a gate electrode material such as poly-Si has a random grain size and shape, or grain boundaries with impurity segregation. In this paper, the species and concentrations of the dopants are mainly focused on from the viewpoint of dielectric breakdown of SiO_2. Though the intrinsic origin of the dielectric breakdown has not yet been clarified, we concentrate on the hole trapping model at the defect sites created by energetic hot electrons [3]. This paper focuses on two experimental points. One is the behavior of the substrate hole current under electron injection from the Si substrate observed in n-MOSFETs. The other point is the polarity dependence of the charge-to-breakdown (Qbd). We studied them as a function of gate electrode and oxide thickness. Finally, it is stressed that Qbd is a statistical quantity and that the stochastic analysis is strongly required by using the percolation approach.

EXPERIMENT

Various types of MOSFETs were fabricated by a conventional submicron CMOS process to study the systematic change of SiO_2 quality by changing the gate electrode and oxide thickness.

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