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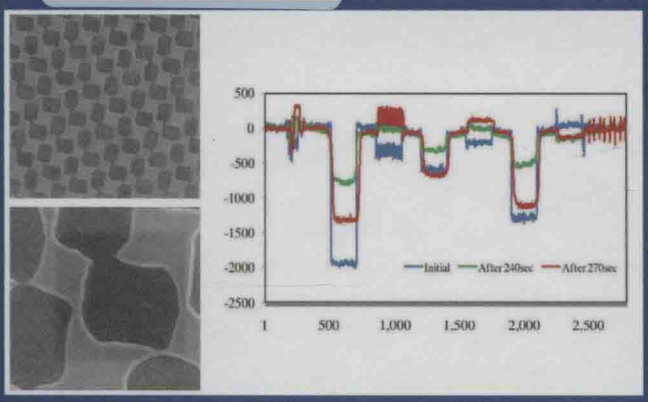

Advances in Chemical Mechanical Planarization (CMP)

Edited by Suryadevara Babu

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Introduction

The high volume fabrication of the billion or more active devices in each microprocessor chip in a silicon substrate is achieved through several evolving and continuing material and technology advances. From a manufacturing perspective, these can be best described by dividing the fabrication sequence into two segments that are commonly labeled front-end-of-the-line (FEOL) and the back-end-of-the-line (BEOL) process steps. Typically, FEOL processes include all the process steps necessary to build the device architecture in the substrate, including, in the case of CMOS devices, the structures for the electrical isolation of the devices, the source and drain of the transistors, and the gate that controls the performance characteristics of the channel between them. Of course, all these multitude of devices once fabricated need to be interconnected to form the necessary logic and memory circuits; they also need to be connected to a power source and then finally packaged. These later operations can be conveniently lumped and labeled as the BEOL process steps. Chemical mechanical planarization (CMP) has been an enabling technology in the realization of both FEOL and BEOL process steps with excellent reproducibility and acceptable product yields.

This book covers a range of topics in the rapidly advancing science and technology of CMP as it is practiced in' both FEOL and BEOL processes. The P in CMP is sometimes used to denote polishing, which may imply only material removal as in the case of a featureless blanket film. In contrast, "planarization" explicitly refers to the ultimate role of CMP in achieving the wafer- and die-level surface planarity across widely varying pattern sizes and densities. The other two words in CMP, "chemical" and "mechanical," are the essence of the process, since a synergistic interplay between what at first glance may appear to be discrete processes that are essentially chemical and mechanical in nature, is crucial to the overall success of the CMP process. The nanoscale surface topographic uniformity that is essential to overcome the depth-of-focus limitations of the lithography techniques used to pattern the device structures can only be achieved by the CMP process.

Nevertheless, since it relies on the abrasive properties of metal oxide particles suspended in a colloidal dispersion, the activity of the chemical reagents, a relatively softer polymeric pad, and a wafer carrier to hold the wafer face down to achieve the nanolevel wafer and die scale planarity, it is truly counterintuitive in its scope. The side containing the active elements of each and every wafer, always processed in an ultraclean and extremely low particle environment, is exposed to billions of abrasive particles multiple times, and after each pass *all* the particles and the chemical agents in the dispersion need to be completely removed from the wafer surface during post-CMP processing to prevent surface contamination and degradation. In spite of this, CMP has proven to be

the only viable technique that can achieve nanolevel uniformity over many generations of rapidly diminishing feature sizes.

Innovative engineering coupled with a solid scientific underpinning and creativity have led to immeasurable progress in the functionality of these integrated logic and memory devices while simultaneously lowering their ultimate cost by orders of magnitude over the last 25–30 years. Now silicon-based microelectronic devices contain over a billion active devices, a number that continues to increase, and continue to be sold at ever dropping prices. This unparalleled combination has made these devices ubiquitous in our daily life, e.g., in automobiles, smartphones and communications, video streaming, and medical diagnostics, just to name a few. In the process, they are creating an extraordinary impact on society and in some cases in unforeseen ways. Indeed, it is commonplace now to see 3- or 4-year-old children who have become proficient in manipulating screen images created by these devices to entertain themselves as well as learning from them.

Such an extraordinary functionality coupled with the necessary speedy response are achieved by continuously shrinking the feature sizes over time, planned and driven by the International Technology Roadmap for Semiconductors (ITRS), a roadmap that is updated every 2 years or so (the latest is available at http://www.itrs.net/) and keeping up with the dictates of the so-called Moore's law. Now devices containing functioning elements with a nominal size of 14 nm are in high volume production with even smaller sizes on the horizon.

The recent and successful emergence of three-dimensional finFET gate structures has led to a dramatic improvement in the performance of the logic devices but also necessitated more stringent removal rate and planarization challenges for the CMP FEOL operations. Various dielectric materials are essential components in these devices, providing electrical insulation, masking, etch and polish stops, etc., as well as playing an active role in the formation of the gate. Planarization of these dielectric films on each wafer is carried out multiple times in the process sequence and is discussed in the chapter authored by Yongsik Moon. Polishing of a-SiC, another potential stop layer in the film stack, is discussed in the chapter by Uma Lagudu.

In situ accessing of the surface of the oxide films being polished can provide very useful information. In spite of the strongly optically absorbing nature of the polishing slurries, Henrik Schumacher and Ulrich Künzelmann describe in their chapter how Fourier transform infrared spectroscopy and attenuated total reflection spectroscopy can be used to investigate the surface states as well as the chemical, mechanical, and colloidal interactions at the oxide surfaces during polishing. Additionally, planarizing SiGe and several III–V candidate materials for faster electron and hole transport across the channel in any transistor is gaining considerable attention, especially for the next generation nodes. Along with the CMP challenges, serious environmental concerns for safe handling of these materials and post-CMP disposal have emerged. These concerns are being exacerbated by the potential for various health hazards of the smaller sized abrasive particles alone or in combination with the chemical reagents present in the colloidal dispersions. These newer classes of materials and the environmental challenges posed by them are discussed in this book in the chapters authored by Patrick Ong and Lieve Teugels and by David Speed, respectively.

The immensity of the number of devices to be interconnected in the BEOL requires a complex nonplanar multilevel wiring scheme that physically towers over the silicon substrate, quite analogous to a multistory apartment complex, except that the feature sizes are at the nanolevel. Indeed, the minimum interconnect pitch, which is the sum of the wiring thickness and space between a pair of wires, is only ~52 nm and dropping, while the number of wiring levels, analogous to the number of floors in the complex, is over 14 in some current devices.

A rough metric for the signal speed in the wiring of the interconnect structures is the inverse of product of the resistance of the conductive wires and the capacitance of the dielectric insulators separating them—the lower the product, the higher the speed. Hence, in simple terms, the metals with a high conductivity and the dielectrics with a low capacitance are preferred during design and fabrication. However, the conductivity of metallic nanowires starts decreasing with decreasing line width while lower capacitance materials are prone to mechanical and electrical reliability concerns due to their fragile nature and inherent porosity, complicating this simple criterion. In any case, Cu is the current metal of choice for the electrical wiring while a variety of so-called low-k dielectrics are available as alternatives to silicon dioxide to insulate them electrically from each other. However, Cu can diffuse through various oxide dielectrics even at relatively low temperatures and hence requires a diffusion barrier layer that also enhances adhesion between it and the dielectric layer. Until recently a thin layer of Ta/TaN has been preferred for such a barrier layer. However, due its relatively low electrical conductivity and the diminishing width of the Cu lines, thinner and more conductive metallic films like Co, Ru, Mn, etc. and their alloys are being tested. In principle, these are all very good candidates but still face several challenges that need to be overcome. In this book, these concerns regarding the use of Cu for 22 nm and future smaller nodes and ultra-low-k dielectric materials are addressed in the chapters authored by Mahadevaiyer Krishnan and Michael Lofaro and by Jakub Nalaskowski and Satyavolu Papa Rao, respectively.

The differential chemical reactivity of the Cu and barrier films when exposed to the slurry chemicals in the polishing environment can lead to the desired selective material removal but can also generate a variety of defects—corrosion pits, fangs due to galvanic corrosion, etc., and the underlying processes can be best investigated using a variety of electrochemical techniques, as described in the chapter authored by Dipankar Roy.

An importance reason for the widespread use of CMP in device fabrication, whether FEOL or BEOL, is the ability to maintain the all-important process yields by minimizing various types of defects both in dielectric and metal films through a combination of an increased understanding of the formation and characterization of various types of defects and by time-consuming and rather expensive process optimization through trial and error. CMP may even eliminate some of the preformed defects in the incoming wafers, even though it is commonly felt that CMP is the root cause of most of the defects. Since abrasives by design have to dig, scratch, and remove material from the film surface that is being planarized, they also leave defects and particle/pad residue behind. These topics are discussed in the chapter authored by Wei-Tsu Tseng. Potentially, most of these defects can be eliminated if abrasive-free solutions or

dispersions with ultra-low abrasive loading can be utilized without any detrimental effects on removal rate and selectivity. Some available formulations are discussed in the chapter authored by Naresh Penta.

Another type of related, and just as important, challenge is the minimization of the within-wafer and within-die removal rate nonuniformity. The inherent complexity and dynamics of the three body interactions occurring in the wafer/abrasive/pad contact region modulated by the chemical reagents and the inability to probe this region experimentally compound and complicate the necessary process optimization. Many factors including various components in the polishing tool like the wafer carrier, pressure distribution across the wafer, retaining ring and the backing film, and the polishing pad along with the slurry flow rate and its distribution along the pad–wafer interface impact the optimization process. In spite of these difficulties, process improvements that lead to defect minimization and high product yields are being made. Slurry characteristics themselves, for example, large particles, play a crucial role in many of the polishing performance metrics. All these are discussed in the chapters authored by Manabu Tsujimura, Kevin Pate and Paul Safier, and Jihoon Seo and Ungyu Paik. Pad conditioning to maintain its surface activity is crucial and is discussed in the chapter authored by Z. Li, E. Baisie, X. Zhang, and Q. Zhang, while a novel slurry injection system that can help achieve better slurry distribution and utilization is discussed in the chapter by Len Borucki.

Since direct experimental probing of this three body contact region has not been practical, significant resources are allocated to model the interactions occurring in this region. Remarkably, the length scales involved range from hundreds of millimeters at the pad and wafer level down to nanometers at the device level, meaning a 10^7-fold variation. The advances being made in this multilength scale arena are described in the chapter authored by Wei Fan and Duane Boning.

Novel Ge-Sb-Te-based chalcogenide phase change materials have displayed immense potential for flash memory storage but require various planarization steps for resolving some of the manufacturing challenges as discussed in the chapter authored by Zhitang Song and Liangyong Wang.

Silicon-based semiconductor processing technologies are also widely used to manufacture a variety of analog/RF devices, passive components, high voltage and power transistors, sensors and actuators commonly known as MEMS (microelectromechanical systems) and MOEMS (microoptoelectromechanical systems), and biochips. Even though the feature sizes in these devices differ widely from each other and are much larger than those in Si-based devices, they pose their own processing peculiarities. Gerfried Zwicker has authored a chapter describing the remarkable applications of CMP for these diverse applications that he aptly labeled "More than Moore Devices." Next generation optoelectronic devices, a rapidly growing technology segment, require mirror-smooth GaN substrates. In spite of GaN's very high hardness and chemical inertness, CMP offers uniquely a way of achieving the desired surface finish as described in the chapter authored by Hideo Aida.

The collection of chapters that constitute this book is wide ranging but obviously does not cover the entire gamut. In particular, while immense progress has been made in understanding the fundamental science and technology of the planarization