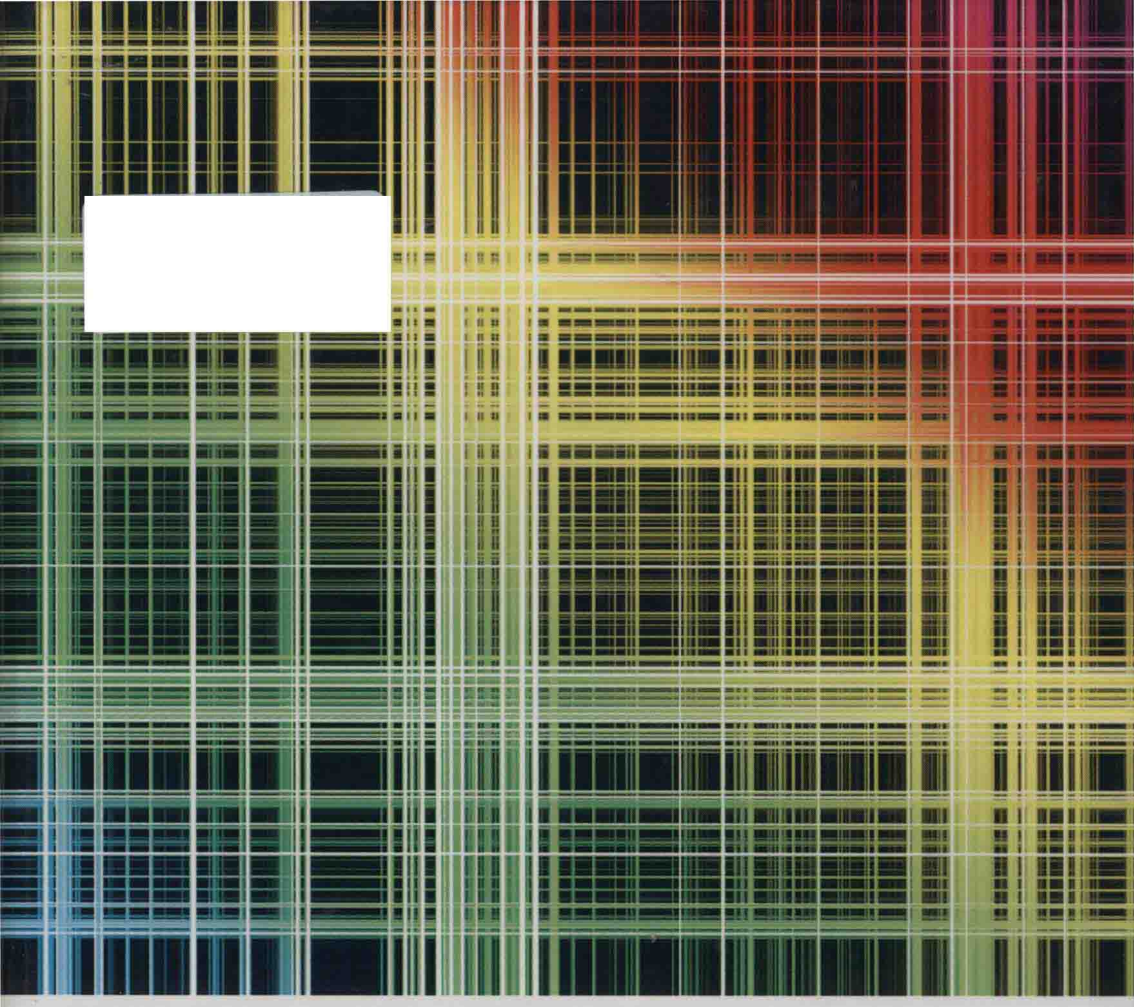

Integrated Lasers on Silicon

Charles Cornet, Yoan Léger and Cédric Robert

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Pierre-Noël Favennec, Frédérique de Fornel, Pascal Besnard

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Preface

At first sight, an entire book on integrated lasers on silicon may appear to be a very specialized reading only for experts. But given the tremendous growth of silicon photonics in research and application fields during the last 10 years, we think that a comprehensive presentation of the issues, strategies and realizations of laser sources on silicon with respect to integration constraints will provide useful information for a broad range of readers.

This book may thus be of interest to people both in the industry and academia, from the microelectronics or optoelectronics sector, especially researchers or engineers. It covers a wide range of specialization, from materials research, to laser devices and microprocessor architecture. We try to explain the prerequisites for understanding the issues and goals of laser integration on silicon as simply as possible, so that students may use this book to strengthen their general knowledge on this topic, and benefit from the numerous references provided therein.

Though the material for this book was mainly taken from the large literature in the field, some of it also come from the various interactions that we have regularly with several industrial or academic research groups working on silicon photonics worldwide.

We would like to acknowledge the contribution of colleagues from the 3D-optical-many-cores project supported by CominLabs, especially S. Le Beux, I. O'Connor, X. Letrartre and C. Monat from the Lyon Institute of Nanotechnology (INL), O. Sentieys, D. Chillet

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Charles CORNET
Yoan LÉGER
Cédric ROBERT
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Introduction

With the emergence of the first semiconductor devices in the early 1950s [BAR 48, CHA 54], it was quickly understood that their unique optoelectronic properties would definitely change our everyday lives. Rapidly, silicon became the material of choice for the development of the whole electronic industry, based on the so-called complementary metal oxide semiconductor (CMOS) technology, while III–V semiconductors (such as GaAs or InP) were widely (but independently) used since the 1970s to develop light emitters, e.g. for optical telecommunications, lightning or other photonic devices. At the dawn of the 21st Century, some pioneering research groups realized that the electronic–photonic convergence could bring various advantages in a large field of applications, such as biosensors, light harvesting devices, defense, consumer electronics, medicine, metrology, robotics, environment, imaging and information processing. Ever since a general consensus was reached on the disruptive power of such research field, as evidenced by the hundreds of research groups and thousands of researchers worldwide, either from academic institutions or the industry, presently working on the co-integration of optical functions with the electronic functions of silicon. One of the most exciting promises lies in the integration of photonics, which is at the very heart of today's microprocessors.

Indeed, looking from the information and communication technology (ICT) point of view, the 21st Century is clearly characterized by an explosion of demand for computing, storage and communication capabilities. In this context, the dramatic "bottleneck" is the difficulty in

transmitting digital information, from worldwide links to chip-to-chip and intrachip interconnections. While photonics is already found at the heart of today's communication networks, providing enormous performance to the backbone, metro and access systems, at shorter distances, the challenges posed by signal speeds, power consumption, miniaturization and overall costs are still only partially addressed. The ultimate solution to this problem could come from optoelectronic integrated circuits (OEICs), and more specifically from on-chip optical interconnects. In this approach, a photonic layer would be part of the microprocessor for information routing and processing. With lower energy consumption, faster data transmission and processing, the on-chip photonic integration may provide ground-breaking optical computation paradigms. Such a technological revolution is thus considered seriously by IBM, Intel, ST Microelectronics and various companies in the field of semiconductors. But the development of OEICs is, however, not straightforward. Elemental building blocks (waveguides, detectors, modulators, sources) should be first developed independently. One of the most serious challenges that we presently face is the development of an integrated laser source on silicon to feed the OEICs with light. The goal of this book is to comprehensively present the advances that have been achieved toward the development of an ideal integrated laser source on silicon.

Contents

1

Laser Integration Challenges

In this chapter, we provide a comprehensive overview of the ultimate properties and performances needed to truly achieve very large-scale integration of laser sources on a silicon chip. Toward this aim, the basic principles of CMOS microprocessors and the different integration schemes of a photonic layer into such architectures are first explained. Then, very simple aspects of semiconductor lasers are presented to provide the minimum prerequisites to the discussion in the next chapters. Finally, an assessment of the required quality that an integrated laser source should ideally possess is given.

1.1. Evolution of microprocessor technologies

The Sparc M7 microprocessor, announced by Oracle in late 2015, shows a record transistor count of 10 billion [AIN 15]. The smallest elements on the chip, the so-called technological node, are 20 nm large and are organized into height clusters of four cores. Thirteen layers of metallization ensure the interconnections between the cores, clock and power drive. We have come a long way from the first integrated circuit developed by Kilby roughly 60 years earlier, which contained two transistors only [KIL 76]. Nowadays, the architecture of microprocessors (MPs) has become so complex that limitations of the complementary metal oxide semiconductor (CMOS) technology progressively reveal themselves. We will see in the following that the

major concern of MP designer is presently energy, leading researchers to work on architecture solutions going beyond CMOS. Many leads are explored, from carbon nanotube electronics and spintronics to MP hybridization. In the last case, the introduction of different hardware technologies within a MP gambles on the complementary advantages of information technologies and high yield conversion between different information technology (IT) platforms or computation paradigms. The grand challenge of integrated photonics is to demonstrate the mandatory role that it could play in future generations of microprocessors, for data routing or even specific computation tasks.

This first section is a brief survey of present CMOS MP technologies and their challenges. The interested reader is encouraged to refer to dedicated books for a deeper understanding of microprocessor technologies, such as the Weste and Harris *CMOS VLSI Design* [PEA 16].

1.1.1. *Microprocessor architecture and design*

Very briefly, the architecture of CMOS microprocessors can be described as a silicon substrate or silicon on insulator (SOI) substrate, on which the logic components of the circuitry are processed, i.e. p- and n-type transistors, inverters, etc. Ion implantation and doping diffusion are mainly used to create the good and active layers of the transistors directly into the silicon. On the contrary, the gate oxide and polysilicon parts are deposited onto the substrate. The CMOS components are then connected through multiple metallization layers embedded into silicon dioxide. Transistor processing occurs at the beginning of the production line in the fab. It is called the "front-end of line" process while the final metallization is called the "back-end" process. By extension, front-end and back-end sometimes characterize positions within the chip, as we will see later. A fab line is generally developed for a single technological node as defined by the International Technology Roadmap for Semiconductors (ITRS). For microprocessors, the technological node refers to the lateral size of the

transistor polysilicon gates. All the other dimensions of the chip components, from the transistor measurements to the size and spacing of the wires at each metallization level are tabulated following this technological node, as design rules. At the 32 nm node, nine metallization layers are necessary to ensure the interconnections between transistors as shown in Figure 1.1. At the 20 nm node, 13 metallization layers are necessary. This reveals the decisive role that interconnects play in last generations of microprocessors.

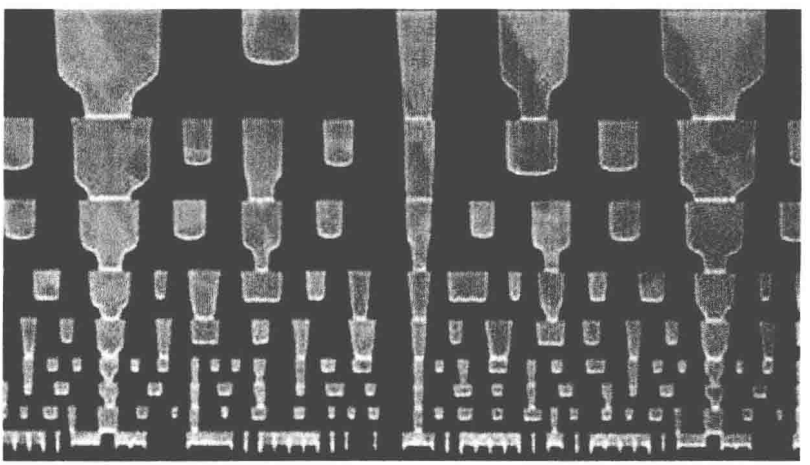

Figure 1.1. *Scanning electron microscopy cross-view of an Intel 32 nm node 9 layer Cu interconnect stack. Only the lowest levels are linked to the transistor plane which is not even spatially resolved on the picture, from Moffat and Josell [MOF 13]. Reprinted with permission from the Electrochemical Society*

On the conceptual side, the design of an MP can be analyzed at different abstraction levels (see Figure 1.2). The higher abstraction level is called the system or architecture level. It describes the prime role of the architecture, its interactions with external devices and also the hierarchy between subsystems of different roles within the chip. An algorithm view of the system with major building blocks is discussed at this level. Next comes the logic and circuit level of abstraction. Its role is to describe in terms of circuitry and logic

diagrams the functions of the different subsystems. At this stage, one of the main concerns of developers is to find the most elegant designs to achieve a particular function. The circuit and logic level hides delay and timing considerations, which are scrutinized at a lower abstraction level. By contrast, power and efficiency of the design is already partly determined at this level of abstraction. Closer to the real architecture of the chip is the layout level. It describes the real geometry of the electronic interconnections and position of the CMOS components. The main issues of this level are the co-integration of the components and the compatibility of the design with a fab line. We will indeed see in the following that the lowering of the technological node induces more and more interactions between the chip elements that are often detrimental to the reliability and yields of the chip. Clever designs have to be developed to prevent such problems with the constraint of keeping within a specific process flow. Thermal management is also a concern of this level since MP operation will necessarily induce formation of hot-spots in the architecture, which can affect the behavior of surrounding components [HAM 07]. The layout level is also highly dependent upon the upper and lower abstraction levels: the logic and circuit level and the last so-called physical level. This last level describes the geometry of the CMOS components, for example if the diffusion parts of many transistors are merged together or not. It is mainly compelled by the technological node and the fab capacities. A clever design of the CMOS components will have the crucial and final role on determining the global speed and power of the chip as well as the signal reliability. The commercial introduction of SOI substrates in the late 1990s has deeply modified the design at the physical level. Transistors are then embedded into an insulating oxide, improving the power and delay yields of the components but also inducing novel design complications such as variability of the delays due to the floating body voltage. One especially understands that the physical level will be highly impacted by the shift toward beyond-CMOS technologies where the very nature of transistors will be modified [NIK 13].