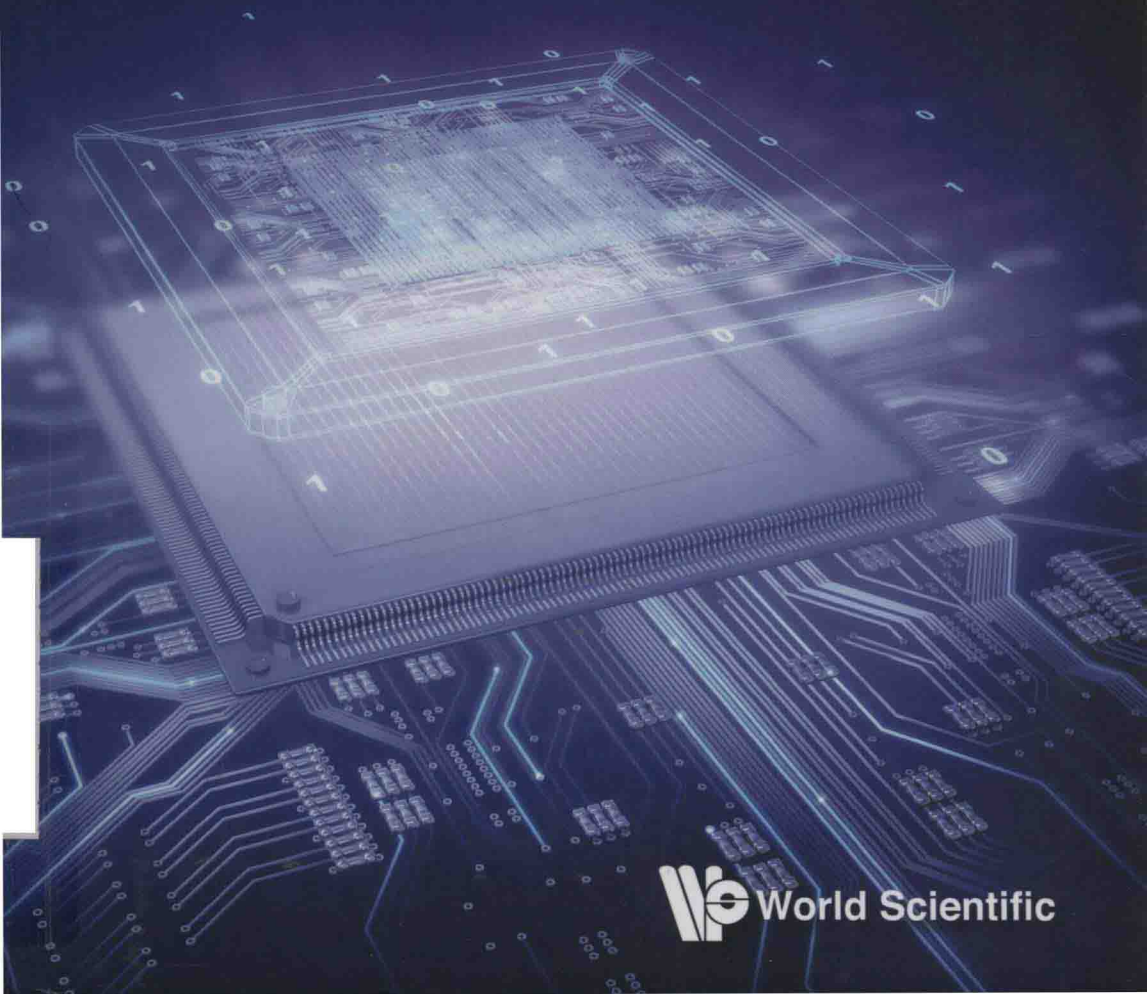
Series on Emerging Technologies in Circuits and Systems

Advances in 3D Integrated Circuits and Systems

Hao Yu • Chuan Seng Tan



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NTU, Singapore

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by Hao Yu and Chuan-Seng Tan

Preface

In the past few decades, the design of computers has been primarily driven by improving performance with faster clock frequency of single-core processor using transistor scaling. The transistor scaling towards high performance of fast clock frequency is, however, stuck recently due to the constraint of power density. By exploiting parallelism, multi-core processor based design of computers has emerged to scale up performance of throughput under power budget. As such, the scaling paradigm has changed to integrate as many processor cores as possible on one single chip. In the traditional 2D based memory-logic integration, the scalability of many-core integration is limited by the communication between the cores and memory by I/O interconnections, which have posed stringent requirements for high utilization efficiency of both bandwidth and power towards operating thousands of microprocessor cores on chip.

Stacking one layer (with core or memory blocks) above the other with short-distance RC interconnects of through-silicon vias (TSVs), 3D integration has become one promising alternative for many-core memory-logic integration with high bandwidth and low power. The other possible alternative for many-core memory-logic integration is 2.5D integration, to place core and memory blocks both on one common substrate, interconnected with the aid of middle-distance transmission lines (underneath the substrate) of through-silicon interposers (TSIs). Even though 3D and 2.5D integrations are potential candidates for many-core memory-logic integration, there are a few critical issues to be addressed as shown in this book.

From the device fabrication perspective, TSV involves a complex process due to its smaller dimension and demanded accuracy with existence of liner material around metal-fill. On the other hand, fabrication of TSI involves fabrication of TSV, microbumps and other metal layers, thus involving

additional complexity. The modeling of TSV/TSI can be quite different from the traditional RC interconnects. Existence of liner material around TSV metal-fill and also thermal-mechanical stress due to mismatch of coefficient of thermal expansion (CTE) between Si and TSV metal-fill can have critical effect on the active device parameters in the vicinity of TSV. In addition, as the fabricated TSVs may result in a poor yield, careful physical design and testing needs to be carried out. However, due to the existence of thousands of TSVs, a low complex physical design is required.

From the system management perspective, thermal management is one of the key challenges to be addressed in 3D integration. In addition to allocating dummy TSV for cooling, recent microfluidic channel based active cooling is also introduced. Microfluidic channels can be etched beneath the substrate of each layer in 3D and the microfluid flowing through the channel can help in cooling the substrate layer. However, an effective management of microfluid has to be performed such as flow-rate control to avoid unnecessary overhead. Similarly, dummy TSVs can be inserted to reduce the thermal and stress gradients across the chip. In addition to thermal management, power management needs to be performed in 3D many-core processors as well to avoid dark silicon dilemma. Many multi-core processor designs make use of off-chip power converters, which may not be scalable for the surge of the supply current demanded by many-core processors. As such, an effective power management of power I/Os needed to be carried with less number of power converters.

What is more, signal I/Os are utilized for the communication between memory and logic blocks. The available limited communication bandwidth is often the bottleneck. Bandwidth utilization of 2.5D TSI I/Os is less compared to that of 3D TSV I/Os. To improve the bandwidth utilization, memory controller needs to be explored with configurability. Previous works on memory controllers are either static or non-scalable for many-core processors. Further, with the increase in communication between memory and logic blocks, communication power also increases. Reduction in I/O voltage swing can help in reducing the communication power at the expense of bit-error-rate (BER). As some types of workloads can tolerate a certain amount of BER, I/O communication can thereby be performed with reduced voltage swing by the use of signal I/O management.

This book is intended to address all the above mentioned challenges. The need for many-core processors with according design challenges faced in the traditional 2D integration is presented in Chapter 1. The rest of the book is divided into five parts as follows.

Part 1 deals with the 3D-IC device modeling. We introduce fabrication methodology utilized for TSVs and TSIs and also evaluate their performance with different kinds of materials in Chapter 2. We further develop TSV and TSI device models in Chapter 3.

Part 2 presents the 3D-IC physical design and testing. We introduce macromodeling to reduce the physical design complexity of thousands of TSVs, which is followed by the corresponding TSV allocation methods for power grid and clock in Chapter 4 and Chapter 5 respectively. Moreover, to effectively evaluate the reliability of TSVs under test, we further propose the TSV testing with compressive sensing as discussed in Chapter 6.

Part 3 illustrates the thermal management of 3D-IC many-core processors. We introduce the system level thermal and power models in Chapter 7. We further discuss microfluid based thermal management in Chapter 8.

Part 4 deals with the power and signal I/O management of the 3D-IC many-core processor. To improve power-converter utilization, we present the power I/O management by space-time multiplexing in Chapter 9. To improve I/O channel utilization, we also present the signal I/O management by the space-time multiplexing and the adaptive voltage-swing in Chapter 10.

Part 5 presents 3D-IC design examples. We first show the 3D integration of MEMS sensor and CMOS readout circuit in Chapter 11. Next, we present the 2.5D I/O design such as pre-emphasis, adaptive driver, and clock-data recovery in Chapter 12. We further discuss an 8-core microprocessor with accelerator and memory blocks integrated by 2.5D I/Os. Lastly, we discuss the 3D integration of the non-volatile memory in Chapter 14.

Lastly, the authors would like to thank their students at Nanyang Technological University: Sai Manoj P. D., Lin Zhang, Hongyu Li, Hantao Huang, Kanwen Wang, Yuhao Wang, Dongjun Xu, Xiwei Huang, Hanhua Qian, Shunli Ma, Yang Shang, Jie Lin and Shikai Zhu, for their contribution to this book. Sai Manoj P. D. in particular has made the significant help for this book. The authors would also like to thank their colleagues: Prof. Paul Franzon, Prof. Sungkyu Lim, Prof. Dennis Sylvester, Prof. Sheldon Tan, Prof. Yuan Xie, Prof. Eby Friedman, Prof. Chiphong Chang, Prof. Zhiyi Yu and Prof. Wei Zhang, for their kind suggestion and collaboration. The relevant research is funded by MOE Tier-2, A*STAR PSF, DIRP and NRF CRP grants from Singapore.

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