TOP-DOWN DIGITAL VLSI DESIGN

From Architectures to Gate-Level Circuits and FPGAs

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MORGAN KAUFMANN

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Top-Down Digital VLSI Design

Preface

WHY THIS BOOK?

Designing integrated electronics has become a multidisciplinary enterprise that involves solving problems from fields as disparate as

- Hardware architecture
- Software engineering
- Marketing and investment
- Semiconductor physics
- Systems engineering and verification
- Circuit design
- Discrete mathematics
- Layout design
- Electronic design automation
- Hardware test equipment and measurement techniques

Covering all these subjects is clearly beyond the scope of this text and also beyond the author's proficiency. Yet, I have made an attempt to collect material from the above fields that I have found to be relevant for making major design decisions and for carrying out the actual engineering work when developing Very Large Scale Integration (VLSI) circuits.

The present volume covers front-end design, that is all steps required to turn a software model into a gate-level netlist or, alternatively, into a bit stream for configuring field-programmable logic devices. A second volume on back-end design may follow at a later date.

The text has been written with two audiences in mind. As a textbook, it wants to introduce engineering students to the beauty and the challenges of digital VLSI design while preventing them from repeating mistakes that others have made before. Practising electronics engineers should find it appealing as a reference book because of the many tables, checklists, diagrams, and case studies intended to help them not to overlook important action items and alternative options when planning to develop their own circuits.

What sets this book apart from others in the field is its top-down approach. Beginning with hardware architectures, rather than with solid-state physics, naturally follows the normal VLSI design flow and makes the material more accessible to readers with a background in systems engineering, information technology, digital signal processing, or management.

HIGHLIGHTS

- Top-down approach.
- Systematic overview on architecture optimization techniques.
- A chapter on field-programmable logic devices, their technologies and architectures.
- Key concepts behind both VHDL and SystemVerilog without too many syntactical details.
- A proven naming convention for signals and variables.
- Introduction to assertion-based verification.
- Concepts for re-usable simulation testbenches.
- Emphasis on synchronous design and HDL code portability.
- Comprehensive discussion of clocking disciplines.
- Largely self-contained (required previous knowledge summarized in two appendices).
- Emphasis on knowledge likely to remain useful in the years to come.
- Plenty of detailed illustrations.
- Checklists, hints and warnings for various situations.
- A concept proven in classroom teaching and actual design projects.

NOTES TO INSTRUCTORS

Over the past decade, the capabilities of Field-Programmable Gate Arrays (FPGA) have grown to a point where they compete with custom-fabricated ICs in many electronic designs, especially for products marketed by small and medium enterprises.

Beginning with the higher levels of abstraction enables instructors to focus on those topics that are equally relevant irrespective of whether a design eventually gets implemented as "mask-programmed" chip or from components that are configured electrically. That material is collected in chapters 1 to 6 of the book and best taught as part of a Bachelor program for maximum dissemination. No prior introduction to semiconductor physics or devices is required. For audiences with little exposure to digital logic and finite state machines, the material can always be complemented with appendices A and B.

Chapter 7 is the only one to have a clear orientation towards mask-programmed circuits as clocking and clock distribution are largely pre-defined in field-programmable logic devices. As opposed to this, the material on synchronization in chapter 8 is equally important to FPGA users and to persons specializing in full- or semi-custom design.

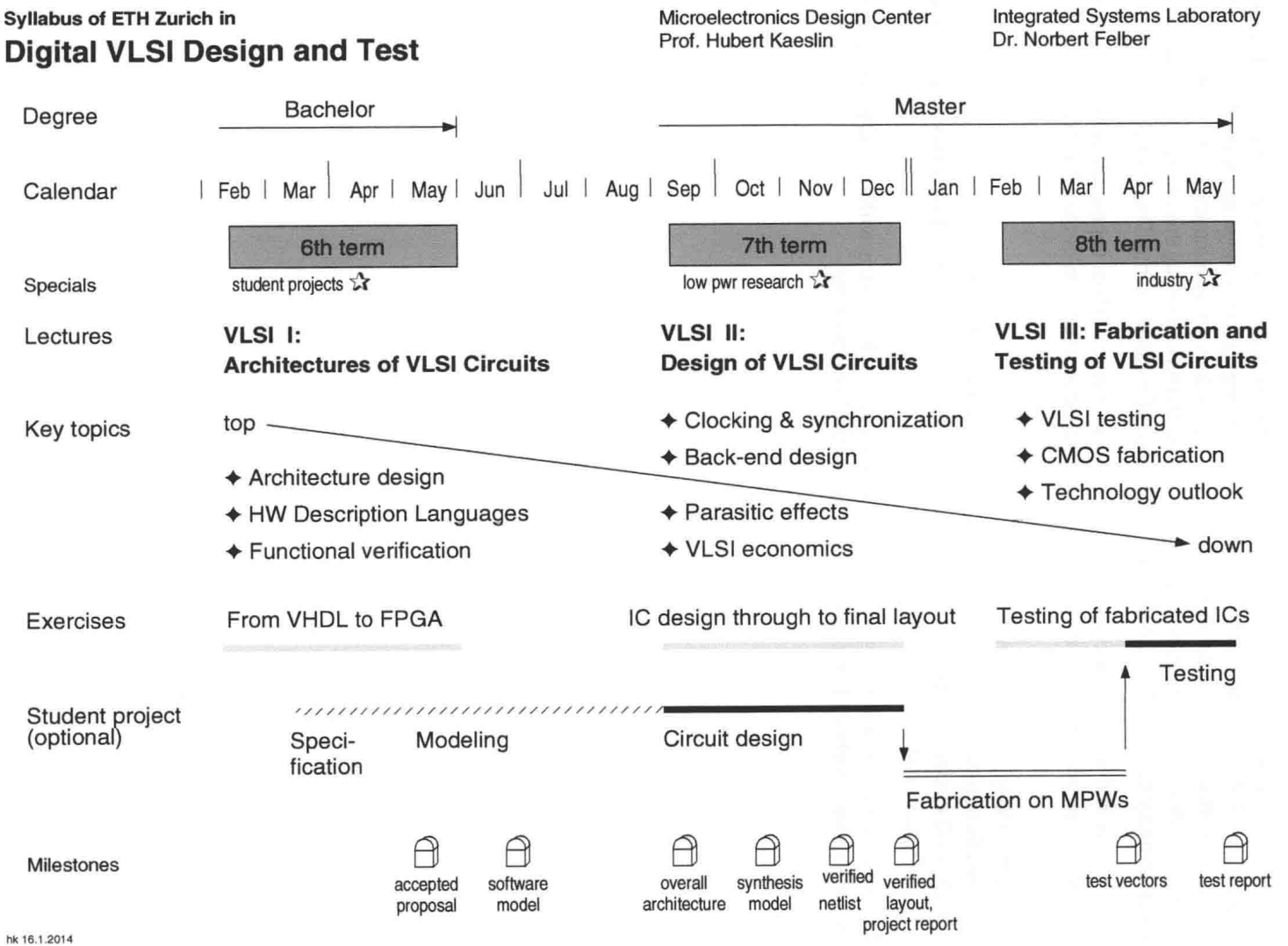
Probably the best way of preparing for an engineering career in the electronics and microelectronics industry is to complete a design project where circuits are not just being modeled and simulated on a computer but actually fabricated and tested. At ETH Zürich, students are given this opportunity as part of a three-semester course given by the author and his colleagues, see figure below. The 6th term covers front-end design. Building a circuit of modest size with an FPGA is practiced in a series of exercises. Provided they come up with a meaningful proposal, students then get accepted for a much more substantial project that runs in parallel with their regular lectures and exercises during the 7th term.

Typically working in teams of two, students are expected to devote at least half of their working time to that project. Following tapeout at the end of the term, chip fabrication via an external multi-project wafer service roughly takes three months. Circuit samples then get systematically tested by their very developers in the 8th and final term. Needless to say that students accepting this offer feel very motivated and that industry highly values the practical experience of graduates formed in this way.

Most chapters in this book come with student problems. Some of them expose ideas left aside in the main text for the sake of conciseness. Problems are graded as a function of the effort required to solve them.

- * A few thoughts lead to a brief answer.
- ** Details need to be worked out, count between 20 min and 90 min.
- *** A small engineering project, multiple solutions may exist. Access to EDA and other computer tools may help.

Solutions and presentation slides are available to instructors who register with the publisher from the book's companion **website** http://booksite.elsevier.com/9780128007303.


Syllabus of ETH Zurich in
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Prof. Hubert Kaeslin
Integrated Systems Laboratory
Dr. Norbert Felber
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Master
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verified
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project report
test vectors
test report
hk 16.1.2014

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Next, I would like to extend my sincere thanks to all students who have followed our courses on Digital VLSI Design and Test. Not only their comments and questions, but also results and data from many of their projects have found their way into this text. Sebastian Axmann deserves special credit for helping with the solutions on a voluntary basis.

Giving students the opportunity to design microchips, to have them fabricated, and to test physical samples is a rather onerous undertaking that would clearly have been impossible without the continuous funding by ETH Zürich. Let me express our gratitude for that on behalf of all our graduates.

In cooperation with Christoph Wicki and his IT support team, the staff of the local Microelectronics Design Center does a superb job in setting up and maintaining the EDA infrastructure and the services indispensable for VLSI design in spite of the frequent landslides caused by rapid technological evolution and by unforeseeable business changes. I am particularly grateful to them for occasionally filling all sorts of gaps in my technical knowledge without making me feel too badly about it.

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