



HARDWARE HANDBOOK



HARDWARE HANDBOOK

Copyright © 1982 Digital Equipment Corporation.
All Rights Reserved

Digital Equipment Corporation makes no representation that the interconnection of its products in the manner described herein will not infringe on existing or future patent rights, nor do the descriptions contained herein imply the granting of license to make, use, or sell equipment constructed in accordance with this description.

The information in this document is subject to change without notice and should not be construed as a commitment by Digital Equipment Corporation. Digital Equipment Corporation assumes no responsibility for any errors that may appear in this manual

DEC, DECnet, DECsystem-10, DECSYSTEM-20, DECTape
DECUS, DECwriter, DIBOL, Digital logo, IAS, MASSBUS, OMNIBUS
PDP, PDT, RSTS, RSX, SBI, UNIBUS, VAX, VMS, VT
are trademarks of

Digital Equipment Corporation

This handbook was designed, produced, and typeset
by DIGITAL's New Products Marketing Group
using an in-house text-processing system.

PREFACE

VAX is DIGITAL's family of 32-bit minicomputers. This handbook provides a brief introduction to VAX and detailed descriptions of the VAX family members: the new VAX-11/730, the VAX-11/750, the VAX-11/780, and the new VAX-11/782.

PART I introduces the reader to VAX with an overview of the VAX architecture and the capabilities of the newly enhanced VAX/VMS operating system. To complete the VAX family picture, a hardware overview of the VAX processors is provided.

For detailed information on the new entry-level VAX, PART II of this book describes the VAX-11/730 console subsystem, the central processing unit, the main memory subsystem, the UNIBUS subsystem, and the privileged registers.

PART III covers the VAX-11/750, including the topics listed above and a chapter on the MASSBUS subsystem.

Both the VAX-11/780 and the VAX-11/782 are discussed in PART IV. Additional chapters for the VAX-11/780 include Chapter 15 on the Synchronous Backplane Interconnect and Chapter 19 on Interconnects and the VAX-11/782.

PART V details the wide range of dependability features built into VAX computer systems. These features were designed to ensure VAX reliability, availability, and maintainability.

PART VI of this book contains 13 appendices, a glossary, and an index for your convenience.

In addition to this handbook, two other VAX handbooks are available:

- The *VAX Architecture Handbook*, describing the VAX system architecture, addressing modes, and the native mode instruction set
- The *VAX Software Handbook*, describing the VAX/VMS operating system, its operation, hardware interaction, data structures, features, and capabilities

As with all VAX handbooks, a comment card has been placed in the back of the book. All comments are greatly appreciated, as they help us make the VAX handbook set meet your needs.

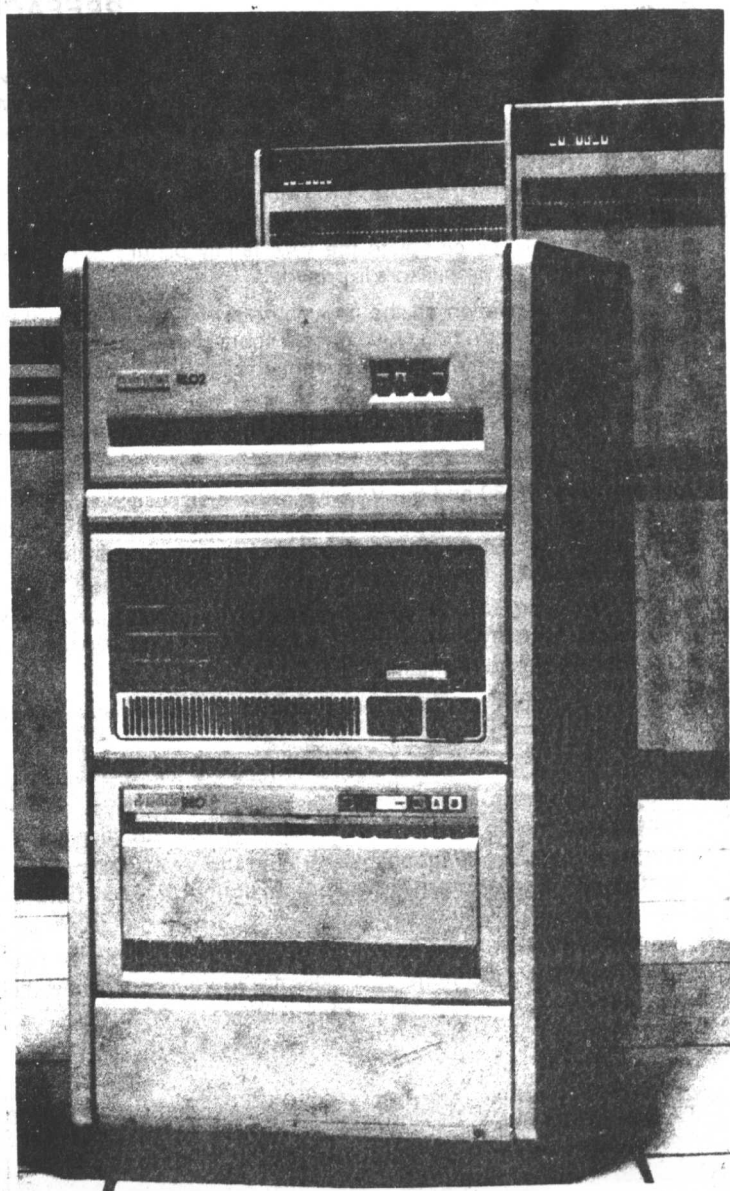


TABLE OF CONTENTS

PREFACE	IX
----------------------	-----------

PART I INTRODUCTION

CHAPTER 1 AN INTRODUCTION TO VAX	
THE VAX FAMILY	1
ARCHITECTURE OVERVIEW	4
SOFTWARE OVERVIEW	7
HARDWARE OVERVIEW	9
READING THIS HANDBOOK	15

PART II THE VAX-11/730

CHAPTER 2 VAX-11/730 CONSOLE SUBSYSTEM	
INTRODUCTION	19
CONSOLE MODES	20
CONSOLE TERMINAL	23
CONSOLE COMMAND LANGUAGE	24
INTEGRAL TU58 TAPE DRIVES	35
BOOTING THE VAX-11/730 SYSTEM	35

CHAPTER 3 VAX-11/730 CENTRAL PROCESSOR	
INTRODUCTION	39
PROGRAMMED ARRAY LOGIC TECHNOLOGY	41
HARDWARE ELEMENTS	41

CHAPTER 4 VAX-11/730 MAIN MEMORY SUBSYSTEM	
INTRODUCTION	47
BASIC MEMORY OPERATIONS	49
CONTROL AND STATUS REGISTERS	50
ERROR CHECKING AND CORRECTION	54

CHAPTER 5 VAX-11/730 UNIBUS SUBSYSTEM	
INTRODUCTION	57
VAX-11/730 UNIBUS SUMMARY	58
VAX-11/730 UNIBUS ADAPTER	62
PROCESSOR ACCESS TO UNIBUS	62
UNIBUS INITIATED DATA TRANSFERS	63

DMF32 COMMUNICATION BOARD	67
---------------------------------	----

CHAPTER 6 VAX-11/730 PRIVILEGED REGISTERS	
INTRODUCTION	69
CONSOLE TERMINAL REGISTERS	70
TU58 REGISTERS	73
TIME-OF-YEAR CLOCK AND INTERVAL TIMER REGISTERS	75
FLOATING POINT ACCELERATOR REGISTER	77

PART III THE VAX-11/750

CHAPTER 7 VAX-11/750 CONSOLE SUBSYSTEM	
INTRODUCTION	81
CONSOLE MODES	82
VAX-11/750 FRONT PANEL	84
CONSOLE TERMINAL	86
CONSOLE COMMAND LANGUAGE	86
INTEGRAL TU58 CARTRIDGE TAPE DRIVE	96
BOOTING THE VAX-11/750 SYSTEM	96

CHAPTER 8 VAX-11/750 CENTRAL PROCESSOR	
INTRODUCTION	105
GATE ARRAY TECHNOLOGY	107
HARDWARE ELEMENTS	107

CHAPTER 9 VAX-11/750 MAIN MEMORY SUBSYSTEM	
INTRODUCTION	113
BOOT ROMS	114
BASIC MEMORY OPERATIONS	115
CONTROL AND STATUS REGISTERS	116
BATTERY BACKUP	120
ERROR CHECKING AND CORRECTION	120

CHAPTER 10 VAX-11/750 UNIBUS SUBSYSTEM	
INTRODUCTION	123
VAX-11/750 UNIBUS SUMMARY	124
VAX-11/750 UNIBUS ADAPTER	128
PROCESSOR ACCESS TO UNIBUS	129
UNIBUS INITIATED DATA TRANSFERS	130

CHAPTER 11 VAX-11/750 MASSBUS SUBSYSTEM	
INTRODUCTION	139

MASSBUS ADAPTER OPERATION	141
MBA REGISTERS	142
DATA PATH	142
MBA ACCESS	143
DATA TRANSFER PROGRAM FLOW	153

CHAPTER 12 VAX-11/750 PRIVILEGED REGISTERS	
INTRODUCTION	157
CONSOLE TERMINAL REGISTERS	158
TU58 REGISTERS	160
CLOCK REGISTERS	162
MACHINE CHECK ERROR SUMMARY REGISTER (MCESR)	165
MACHINE CHECK STATUS REGISTER (MCSR)	166
TRANSLATION BUFFER GROUP DISABLE REGISTER (TBDR)	167
CACHE DISABLE REGISTER (CADR)	168
CACHE ERROR REGISTER (CAER)	168
TRANSLATION BUFFER REGISTER	169
FLOATING POINT ACCELERATOR REGISTER	169

PART IV THE VAX-11/780

CHAPTER 13 VAX-11/780 CONSOLE SUBSYSTEM	
INTRODUCTION	173
CONSOLE INTERFACE BOARD	174
CONSOLE BUS STRUCTURE	177
INTERNAL DATA BUS	177
Q BUS	178
V BUS	178
CONSOLE/VAX-11 INTERACTION	179
READ-ONLY MEMORY (ROM)	179
VAX-11/780 PROCESSOR CONTROL PANEL	179
CONSOLE COMMAND LANGUAGE	182
CONSOLE ERROR MESSAGES	189
BOOTING THE VAX-11/780	192
DEFAULT BOOTSTRAP COMMAND PROCEDURE	195

CHAPTER 14 VAX-11/780 CENTRAL PROCESSOR	
INTRODUCTION	197
HARDWARE ELEMENTS	198
PROCESSOR OPERATION	201

CHAPTER 15	SYNCHRONOUS BACKPLANE INTERCONNECT ..	
INTRODUCTION		207
SBI STRUCTURE		209
PARITY FIELD		211
SBI THROUGHPUT		228
CHAPTER 16	VAX-11/780 MAIN MEMORY SUBSYSTEM	
INTRODUCTION		231
MEMORY CONTROLLER		232
BASIC MEMORY OPERATIONS		233
INTERLOCK CYCLES		236
ERROR CHECKING AND CORRECTION (ECC)		237
MEMORY CONFIGURATION REGISTERS		238
MEMORY INTERLEAVING		243
ROM BOOTSTRAP		244
BATTERY BACKUP		244
CHAPTER 17	VAX-11/780 UNIBUS SUBSYSTEM	
INTRODUCTION		247
UNIBUS SUMMARY		248
THE UNIBUS ADAPTER		253
SBI ACCESS TO THE SBI ADDRESS SPACE		253
UNIBUS ACCESS TO THE SBI ADDRESS SPACE		258
UNIBUS ADAPTER DATA TRANSFER PATHS		262
INTERRUPTS		274
UNIBUS ADAPTER (NEXUS) REGISTER SPACE		278
SBI ADDRESSABLE UNIBUS ADAPTER REGISTERS		280
POWER FAIL AND INITIALIZATION		300
SBI UNJAM		302
EXAMPLE		303
CHAPTER 18	VAX-11/780 MASSBUS SUBSYSTEM	
INTRODUCTION		309
MASSBUS ADAPTER OPERATION		312
CONTROL PATH		315
MBA ACCESS		315
INTERNAL REGISTERS		317
EXAMPLE		328
CHAPTER 19	INTERCONNECTS AND THE VAX-11/782	
OVERVIEW		331
DR780 HIGH PERFORMANCE 32-BIT PARALLEL INTERFACE		332
DR32 DEVICE INTERCONNECT (DDI)		333

PROGRAMMING INTERFACE	337
PROGRAMMING HINTS	339
PHYSICAL CHARACTERISTICS	347
CONFIGURING THE DR780 IN VAX-11/780 SYSTEMS	347
MA780 MULTIPORT MEMORY	349
CAPACITY AND EXPANDABILITY	350
THROUGHPUT	351
DATA INTEGRITY	352
FAILSOFT CAPABILITY	353
USING SHARED MEMORY	354
VAX-11/782 ATTACHED PROCESSOR SYSTEM	359
SOFTWARE	362

CHAPTER 20 VAX-11/780 PRIVILEGED REGISTERS	
INTRODUCTION	367
CONSOLE TERMINAL REGISTERS	368
CLOCK REGISTERS	369
FLOATING POINT ACCELERATOR REGISTERS	372
VAX-11/780 MICRO CONTROL STORE	374

PART V VAX DEPENDABILITY

CHAPTER 21 VAX SYSTEM DEPENDABILITY	
INTRODUCTION	379
FEATURES COMMON TO VAX SYSTEMS	379
VAX-11/730 SPECIFIC FEATURES	388
VAX-11/750 SPECIFIC FEATURES	390
VAX-11/780 SPECIFIC FEATURES	391

PART VI APPENDICES, GLOSSARY, AND INDEX

APPENDIX A COMMONLY USED MNEMONICS	397
APPENDIX B INSTRUCTION INDEX	401
APPENDIX C ADDRESS VALIDATION RULES	411
APPENDIX D VIRTUAL TO PHYSICAL ADDRESS TRANSLATION	415

APPENDIX E	VAX-11/730 INTERNAL PROCESSOR REGISTERS	419
APPENDIX F	VAX-11/750 INTERNAL PROCESSOR REGISTERS	425
APPENDIX G	VAX-11/780 INTERNAL DATA (ID) BUS REGISTERS	435
APPENDIX H	OPERAND SPECIFIER NOTATION	449
APPENDIX I	I/O SPACE RESTRICTIONS	453
APPENDIX J	TECHNICAL SPECIFICATIONS FOR VAX-11/730 PROCESSOR	455
APPENDIX K	TECHNICAL SPECIFICATIONS FOR VAX-11/750 PROCESSOR	461
APPENDIX L	TECHNICAL SPECIFICATIONS FOR VAX-11/780 PROCESSOR	469
APPENDIX M	SYSTEM THROUGHPUT CONSIDERATIONS	477
	GLOSSARY	483
	INDEX	525

AN INTRODUCTION TO VAX

THE VAX FAMILY

VAX is DIGITAL's family of 32-bit minicomputer systems. The new family members—the VAX-11/730 and the VAX-11/782 attached processor system—together with the VAX-11/750 and VAX-11/780, make the power of VAX systems available to a wide range of users, applications and budgets.

All VAX processors implement a 32-bit architecture, an extensive instruction set with numerous data types, and a 32-bit bus structure for high throughput. All VAX system hardware is complemented by the newly enhanced VAX/VMS operating system, a powerful multiprogramming operating system that handles multiuser, realtime and multistream batch applications, plus online program development.

The newest member of the VAX family, the VAX-11/730, incorporates bit-slice and Programmed Array Logic (PAL) technology. Like the other family members, the VAX-11/730 implements the VAX architecture and runs the VAX/VMS operating system and layered software. With the VAX-11/730, however, VAX functionality is available at a much lower price, providing the ability to move VAX power down to the project or section level. The VAX-11/730 can also be used as a powerful, remote DECnet node, allowing its users access to higher performance members of the VAX family when necessary. Connection to mass storage devices and other peripherals is provided through a UNIBUS adapter.

The VAX-11/750, the mid-range member of the VAX family, incorporates many innovations designed to increase performance and to reduce the overall cost of ownership. The VAX-11/750 is the first 32-bit minicomputer to be implemented primarily in custom bipolar LSI Schottky logic (designed entirely by DIGITAL engineers). One UNIBUS adapter (integral to the processor) and up to three MASSBUS adapters or one additional UNIBUS and two MASSBUS adapters may be used for connection to mass storage devices and other peripherals.

The VAX-11/780 was designed to meet the needs of many users with large databases and extensive processing needs. Central to its I/O system is a 32-bit wide data and control path that can move up to 13.3 MB of data per second among the system's major hardware components. Up to four UNIBUS and four MASSBUS adapters may be used for connection to mass storage devices and other peripherals. The support of high-performance disks and tapes by the VAX-11/750,

VAX-11/780 and VAX-11/782, combined with their ability to network with the other VAX family members provides significant and varied configuration possibilities.

The VAX-11/782 attached processor computer system is a tightly-coupled asymmetrical multiprocessor system that can provide up to 1.8 times the performance of a single VAX-11/780 system for compute-intensive applications. Consisting of two VAX-11/780 CPUs, the VAX-11/782 attached processor computer system can support up to 8 MB of MA780 shared memory.

NOTE

Specific information on the VAX-11/782 attached processor system is contained in Chapter 19, Interconnects and the VAX-11/782. Unless otherwise specified, most of the VAX-11/780 features in this chapter apply to the VAX-11/782.

Application Performance

VAX hardware and software were designed to complement each other. Hardware implementation combined with the VAX/VMS operating system, 32-bit addressing, a 4 billion byte virtual memory, an address translation buffer, a prefetch instruction buffer, an optional floating point accelerator, and the powerful VAX instruction set, give VAX systems their impressive performance.

The impressive CPU power and throughput, plus the high performance-to-cost ratio, make VAX systems ideal for interactive applications. The high computational ability and large program size mean VAX systems can handle tough realtime applications as well. Furthermore, the VAX/VMS operating system provides extensive facilities for good batch performance—including job control, multi-stream, spooled input and output, operator control, conditional command branching, and accounting functions. A choice of options such as additional physical memory, user control store, and additional peripheral equipment interfaces, allow even greater flexibility in configuring systems to optimize performance for specific applications.

Ease of Use

VAX systems are user-oriented systems designed for easy operation. The DIGITAL Command Language (DCL) interface used by VAX/VMS is easy to learn and is suitable for both interactive and batch environments. The software compatibility of VAX systems allows software developed for one VAX system to run on another VAX system without modification. Because VAX systems use the same instruction set, it

also means that users need not learn a new series of instructions to take full advantage of another VAX system's capabilities.

VAX/VMS provides extensive system management facilities, giving system managers and operators the tools necessary to control the system configuration and the operations of system users for maximum efficiency. Users will appreciate the extensive HELP commands and complete multiuser security. The VAX family processors also implement a PDP-11 Compatibility Mode which recognizes almost all PDP-11 instructions. This allows users to execute code written for the PDP-11 with few modifications.

The VAX console subsystem also contributes to ease of use. A separate console terminal replaces the traditional toggle switches and lights, and a carefully designed console command language lets the user perform operations such as EXAMINEs and DEPOSITs, or boot the system, using simple commands. This console terminal also provides a hardcopy record for complete documentation of console transactions. Furthermore, switches on the front panel of the CPU can be set up to reboot the system automatically, with no operator intervention, in the event of a power failure or system crash.

Additionally, VAX systems are designed to facilitate rapid, low-cost applications development. With the complete set of VAX/VMS development tools, file system features, optional information management products, and other software packages, applications are easier to develop and require far less debugging time. DIGITAL's extensive educational services are also available to train and assist users in exploiting the wide and varied capabilities of VAX systems.

Easy Installation and Maintenance

A variety of system configurations is available so customers can purchase exactly what is required. VAX systems are easily tuned and adapted allowing additional peripherals and options to be interfaced at any time. Customers may choose from a wide variety of peripherals and packaging options to configure a VAX system to suit their requirements—whether the site is an office, a laboratory, or an industrial setting.

Once the system is installed, extensive reliability, availability, and maintainability features (discussed in Part V of this book) in both the hardware and the software ensure data integrity and increase system uptime. Features such as ECC (Error Correcting Code) memory, on-line error logging, and a complete range of online and stand-alone diagnostics verify system integrity and help ensure proper system

operation. The Remote Diagnosis option for the VAX-11/750 and VAX-11/780 allows a customer to be directly linked to a DIGITAL Diagnostic Center for diagnosis of hardware and software failures. For VAX-11/730 users, customer runnable diagnostics allow a system user the capability of verifying proper hardware operation and the quick isolation of system failures to the subsystem or device level. The Remote Support option, utilizing Remote Diagnosis technology, provides the DIGITAL service engineer with a further level of technical resources.

Sound Long-Term Investment

The features of the VAX series described above, together with the many other features described in the chapters that follow, make VAX systems a sound long-term investment. The new VAX-11/730 and VAX-11/782 systems are a reflection of DIGITAL's ongoing commitment to the VAX family of 32-bit minicomputers and further proof that the VAX family exemplifies the architecture of the 1980s. The wide range of systems possible with the VAX-11/730, VAX-11/750, VAX-11/780, and VAX-11/782 ensures that these systems can be tailored to individual application requirements and can be easily reconfigured if those needs should change in the future—an important consideration for customers involved in long-term projects and implementations.

The following sections in this chapter will introduce the reader to a variety of VAX family architectural and software features, as well as to many of the important hardware features of the various VAX implementations. Appendix A in the back of this book contains a table of commonly used VAX family mnemonics.

ARCHITECTURE OVERVIEW

The VAX family architecture is characterized by a powerful and complete instruction set of 304 instructions (see Appendix B), a wide range of data types, an efficient set of addressing modes, full demand paging memory management, and a very large virtual address space of over 4 billion bytes.

The VAX Native Instruction Set is an extension of the PDP-11 instruction set. Instructions can be grouped into classes based on their functions and uses:

1. Instructions to manipulate arithmetic and logical data types. These include integer, floating point, packed decimal, character string, and bit field instructions.

The data type identifies how many stored bits are to be treated as a unit and how the unit is to be interpreted. Data types that may be used are:

Data Type	Represented As
Integer	Byte (8 bits), word (16 bits), longword (32 bits), quadword (64 bits)
Floating point	4-byte F_floating, 8-byte D_floating, 8-byte G_floating, 16-byte H_floating
Packed decimal	String of bytes (up to 31 decimal digits, 2 digits per byte)
Character string	String of bytes interpreted as character codes (up to 64 KB); a numeric string is a character string of codes for decimal numbers (up to 31 digits)
Bits and bit-fields	Field length is arbitrary and is defined by the programmer (0 to 32 bits in length)

Integer, floating point, packed decimal, and character data are stored starting on an arbitrary byte boundary. Bit and bit field data start on an arbitrary bit boundary. A collection of data structures can be packed together to use less storage space.

2. Instructions to manipulate special kinds of data. These include queue manipulation instructions (i.e., those that insert and remove queue entries), address manipulation instructions, and user-programmed general register load and save instructions. These instructions are used extensively by the VAX/VMS operating system.
3. Instructions to control basic program flow. These include BRANCH, JUMP, and CASE instructions, subroutine CALL instructions, and procedure CALL instructions.
4. Instructions to perform special operating system functions quickly. These include process control instructions (such as two special context switching instructions which allow process context variables to be loaded and saved using only one instruction for each operation), and the FIND FIRST instruction which (among other uses) allows the operating system to locate the highest priority executable process. These instructions contribute to rapid and efficient rescheduling.
5. Instructions provided specifically for high-level language constructs. During the design of the VAX family architecture, special attention was given to implementing frequently-used, high-level language constructs as single VAX instructions. These instructions contribute to decreased program size and increased

execution speed. Some of the constructs which have become single VAX instructions include:

- The FORTRAN-computed GOTO statement (translates into the CASE instruction).
- The loop construct (e.g., add, compare, and branch translates into the ACB instruction).
- An extensive CALL facility (which aligns the stack on a longword boundary, saves user-specified registers, and cleans up the stack on return); the CALL facility is used compatibly among all native mode languages and operating system services.

VAX instructions and data are variable in length. They need not be aligned on longword boundaries in physical memory, but may begin at any odd or even byte address. Therefore, instructions not requiring arguments use only one byte, while other instructions may take two, three, or up to 54 bytes depending on the number of arguments and their addressing modes. The advantage of byte alignment is that instruction streams and data structures can be stored in much less physical memory.

The VAX processors offer several addressing modes. Eleven of these use the general registers to identify the operand location and operate similarly to the PDP-11 addressing modes. The names of the modes are:

- Register
- Register deferred
- Autoincrement
- Autoincrement deferred
- Autodecrement
- Byte, word and longword displacement (similar to the PDP-11 index mode)
- Byte, word, and longword displacement deferred (similar to the PDP-11 index deferred mode)

The two additional addressing modes implemented by VAX family processors are:

- Indexed
- Literal

Because the VAX instruction set is so flexible, most functions require fewer instructions and less storage than on non-VAX processors. The result is more compact and efficient programs, faster program execution, faster context switching, more precise and faster math functions,