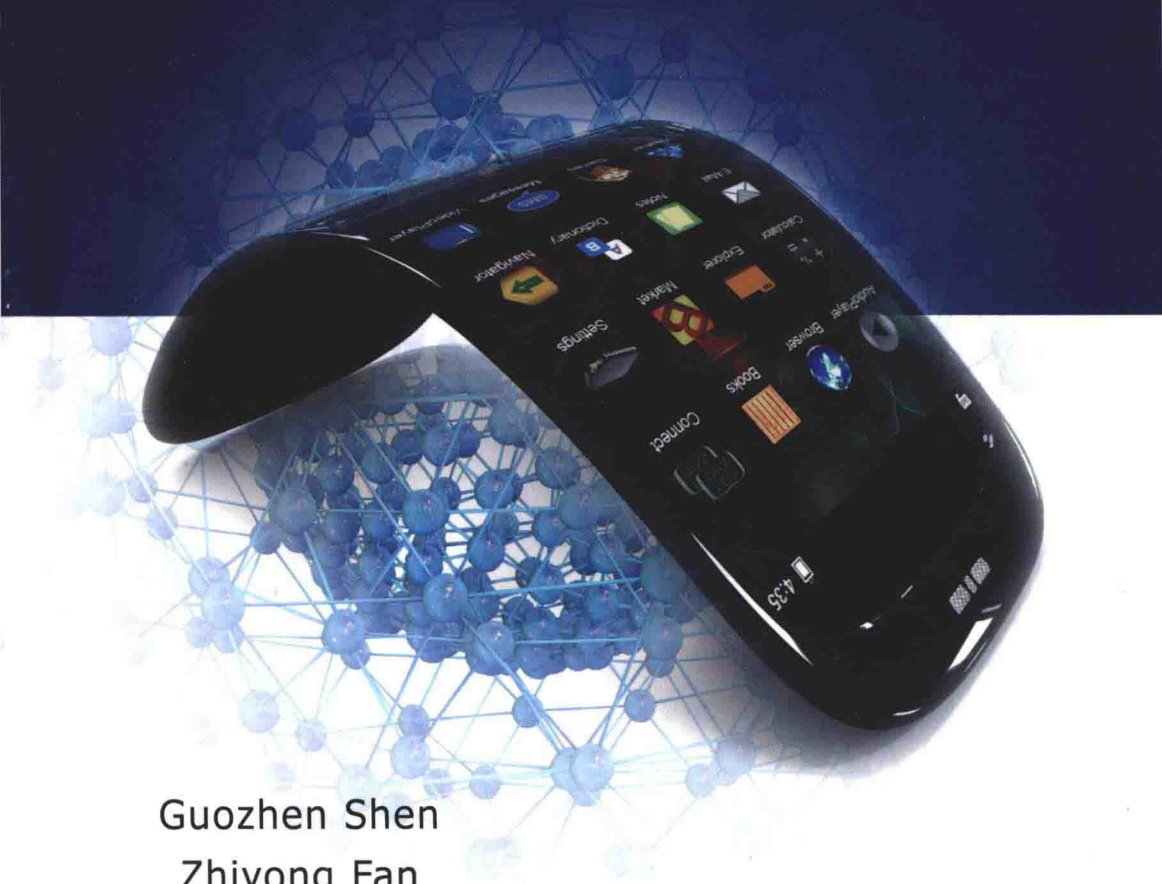
Flexible Electronics

From Materials to Devices



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CONTENTS

CHAPTER 1

CARBON NANOTUBE FLEXIBLE ELECTRONICS

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Single-wall carbon nanotubes (SWNTs) possess fascinating electrical properties and offer new entries into a wide range of novel electronic applications that are unattainable with conventional Si-based devices. The field initially focused on the use of individual or parallel arrays of nanotubes as the channel material for ultra-scaled nanoelectronic devices. However, the challenge in the deterministic assembly of SWNTs has proven to be a major technological barrier. In recent years, solution deposition of semiconductor-enriched SWNT networks has been actively explored for high performance and uniform thin-film transistors (TFTs) on both mechanically rigid and flexible substrates. This presents a unique niche for nanotube electronics by overcoming their limitations and taking full advantage of their superb electronic properties. This chapter focuses on the large-area processing and electronic properties of SWNT TFTs. A wide range of applications in flexible electronics including integrated circuits, radio-frequency (RF) transistors, displays, and electronic skins will be discussed. With emphasis on large-area systems where nm-scale accuracy in the assembly of nanotubes is not required, the demonstrations show SWNTs' immense promise as a low-cost and scalable TFT technology for flexible electronic systems with excellent device performances.

1. Introduction

Single-wall carbon nanotubes (SWNTs) can be considered as monolayer graphene sheets with a honeycomb structure that are rolled into seamless, hollow cylinders. Owing to their small size (diameter around 1–2 nm), as well as their superior electronic properties without surface dangling bonds, SWNTs hold great potential for a wide range of applications in solid-state devices and are envisioned as one of the promising candidates for beyond-silicon electronics. SWNTs can be categorized by their chiral vectors defined on the hexagonal crystal lattice using two integers (m and n). The chiral vectors correspond to the direction along which a graphene sheet is wrapped to result in a SWNT. The electronic properties of SWNTs heavily depend on their chiral vectors and the SWNTs can be either metallic ($m = n$ or $m - n$ is a multiple of 3) or semiconducting (all other cases).[1–4] Using this rule of thumb, one can infer from the possible (n,m) values that one third of SWNTs are metallic and the other two thirds are semiconducting. For practical use as the active channel component of electronic devices, semiconducting SWNTs are commonly used. The advantages of semiconducting SWNTs over other conventional semiconductors are multifold. First of all, the charge carriers in carbon nanotubes have long, mean free paths, on the order of a few hundred nanometers for acoustic phonon scattering mechanism. As a result, scattering-free ballistic transport of carriers at low electric fields can be achieved in carbon nanotubes at moderate channel lengths (e.g., sub-100 nm).[5] Second, the carrier mobility of semiconducting nanotubes is experimentally measured to be > 10,000 $cm^2V^{-1}s^{-1}$,[6,7] at room temperature which is higher than the state-of-the-art silicon transistors. Finally, their small diameters enable excellent electrostatics with efficient gate control of the channel for highly miniaturized devices. Thereby, SWNTs have stimulated enormous interest in both fundamental research and practical applications in nano- and macro-electronics.

Researchers have previously demonstrated excellent field-effect transistors (FETs)[5–12] and integrated circuits[13–17] using individual SWNTs. Figures 1(a) and 1(b) depict the transfer (I_{DS}–V_{GS}) and output (I_{DS}–V_{DS}) characteristics of the state-of-the-art individual SWNT-FET with self-aligned source/drain contacts and near ballistic transport.[11] Impressive

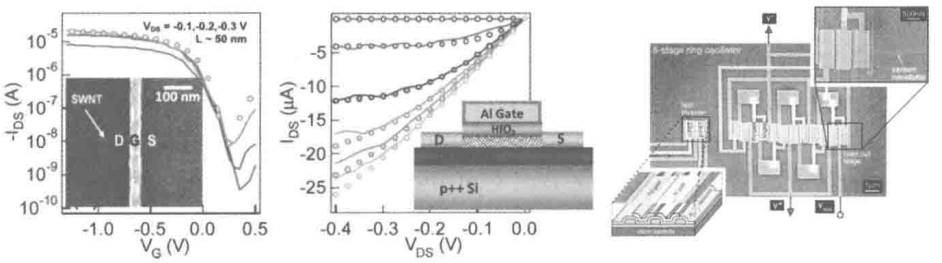


Figure 1. State-of-the-art individual SWNT transistors and circuits. (a) I_{DS}–V_{GS} characteristics of a self-aligned ballistic SWNT-FET with a channel length of 50 nm. Inset: Scanning Electron Microscope (SEM) image of the device. (b) Experimental (solid line) and simulated (open circle) I_{DS}–V_{DS} characteristics of the same device shown in panel (a). Inset: schematic of the device. Reproduced with permission from Ref. 11. (Copyright 2004 American Chemical Society.) (c) SEM image of a 5-stage ring oscillator constructed on an individual SWNT. Reproduced with permission from Ref. 16. (Copyright 2006 The American Association for the Advancement of Science (AAAS).)

performance with subthreshold slope (*SS*) of 110 mV/dec, on-state conductance of 0.5 × $4e^2/h$ and saturation current upto 25 μA/tube (diameter ~1.7 nm) has been achieved in devices with channel lengths down to 50 nm.[11] Better *SS* of ~70 mV/dec, which is close to the theoretical limit of 60 mV/dec, has also been achieved in transistors with slightly longer channel lengths (500 nm).[10] More recently, SWNT-FETs with sub –10 nm channel lengths have been demonstrated.[12] Such devices exhibit an impressive *SS* of 94 mV/dec, current on/off ratio of 10^4, and on-current density of 2.41 mA/μm, which outperform silicon FETs with comparable channel length. Using SWNT-FETs, integrated circuits with various functionalities have been demonstrated. Notable examples include a five-stage ring oscillator (Fig. 1(c)) and pass-transistor-logic-based integrated circuits (full adder, multiplexer, decoder, D-latch, etc.).[16,17]

Despite the tremendous progress made with individual nanotube transistors and circuits, major technological challenges remain, including the need for deterministic assembly of nanotubes on a handling substrate with nm-scale accuracy, minimal device-to-device performance variation, and development of a fabrication process scalable and compatible with industry standards. Hence, the use of carbon nanotubes for nanoelectronic applications is still long from being realized. On the other hand,

the use of SWNT networks, especially based on semiconductor-enriched samples, present a highly promising path for the realization of high performance thin-film transistors (TFTs) for macro- and flexible electronic applications. The most significant advantages of using SWNT random networks for TFTs lie in the fact that the SWNT thin-films are mechanically flexible, optically transparent, and can be prepared using solution-based room temperature processing, all of which cannot be provided by amorphous and poly silicon technologies.[18–20] Compared with organic semiconductors,[21–25] the other competing platform for flexible TFTs, the SWNT thin-films offer significantly better carrier mobility (~2 orders of magnitude improvement). Thereby, large-area TFT applications seem to offer an ideal niche for carbon nanotube based electronics, taking advantage of their superb physical, chemical and electrical properties without being hindered from their precise assembly limitations down to nm-scale.

Numerous research efforts have been devoted to the successful realization of large-scale chemical vapor deposition (CVD) growth of high-density horizontally aligned SWNTs on single crystal quartz or sapphire substrates.[26–34] Transfer techniques have been further developed, enabling the demonstration of high-performance transistors and integrated circuits using the aligned nanotubes on various types of rigid and flexible substrates.[35–42] However, considering the fact that roughly one third of the as-grown nanotubes are metallic, techniques such as electrical breakdown[43] is necessary to remove the leakage-causing metallic paths, which adds complexity, is not scalable, and significantly degrades the device performance due to the high applied fields during the process. Preferential growth of aligned semiconducting SWNTs has been reported recently,[32,44,45] which is an important step forward, however, the purity is not yet high enough to achieve transistors with high on/off current ratio (I_{on}/I_{off}) for digital applications. Therefore, for the purpose of obtaining devices with better I_{on}/I_{off}, it is more attractive to have networks of SWNTs with higher percentage of semiconducting tubes and/or with random orientation where individual nanotubes do not directly bridge the source/drain electrodes, thereby minimizing the metallic pathways.[46–50]

Figure 2 illustrates the most common assembly methods for random nanotube networks including direct CVD growth,[51,52] dry filtration,[53]

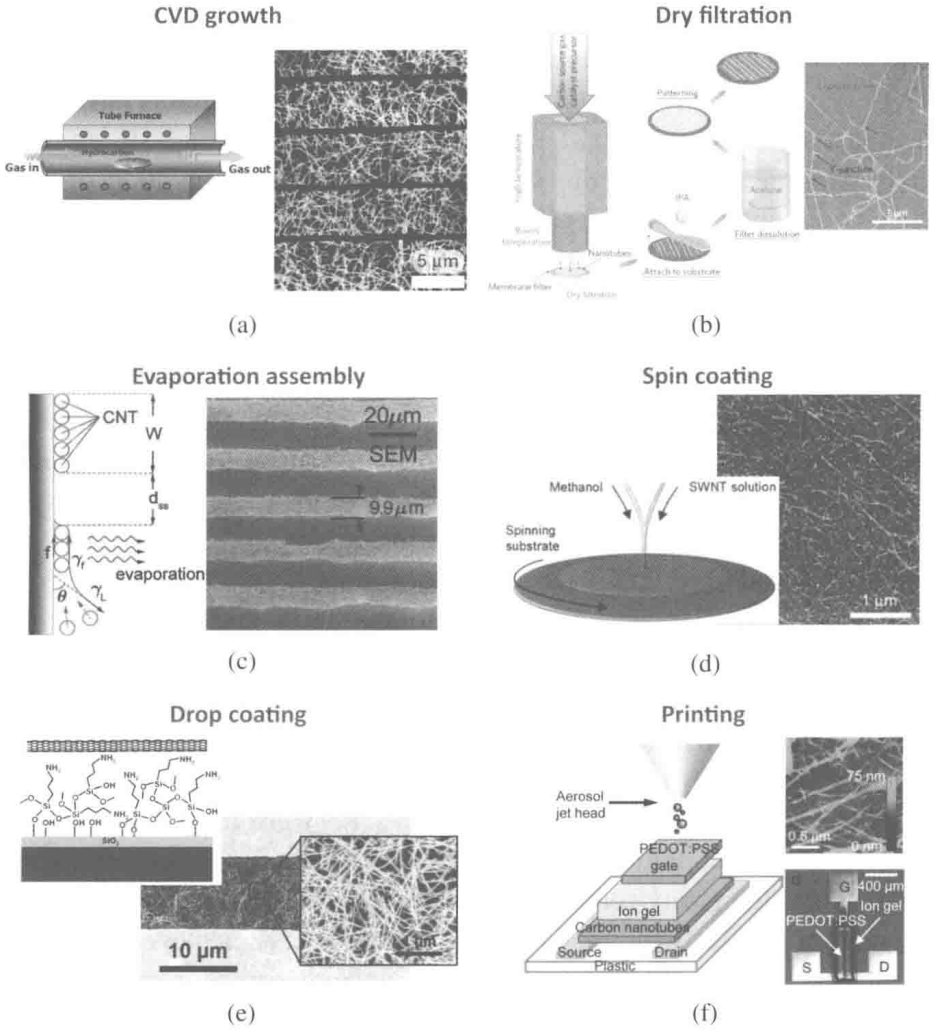


Figure 2. Different methods used for assembling SWNT networks. (a) CVD growth. Reproduced with permission from Ref. 51. (Copyright 2008 Nature Publishing Group.) (b) Dry filtration. Reproduced with permission from Ref. 53. (Copyright 2011 Nature Publishing Group.) (c) Evaporation assembly. Reproduced with permission from Ref. 54. (Copyright 2008 American Chemical Society.) (d) Spin coating. Reproduced with permission from Ref. 55. (Copyright 2004 American Chemical Society.) (e) Drop casting. Reproduced with permission from Ref. 59. (Copyright 2009 American Chemical Society.) (f) Printing. Reproduced with permission from Ref. 64. (Copyright 2010 American Chemical Society.)

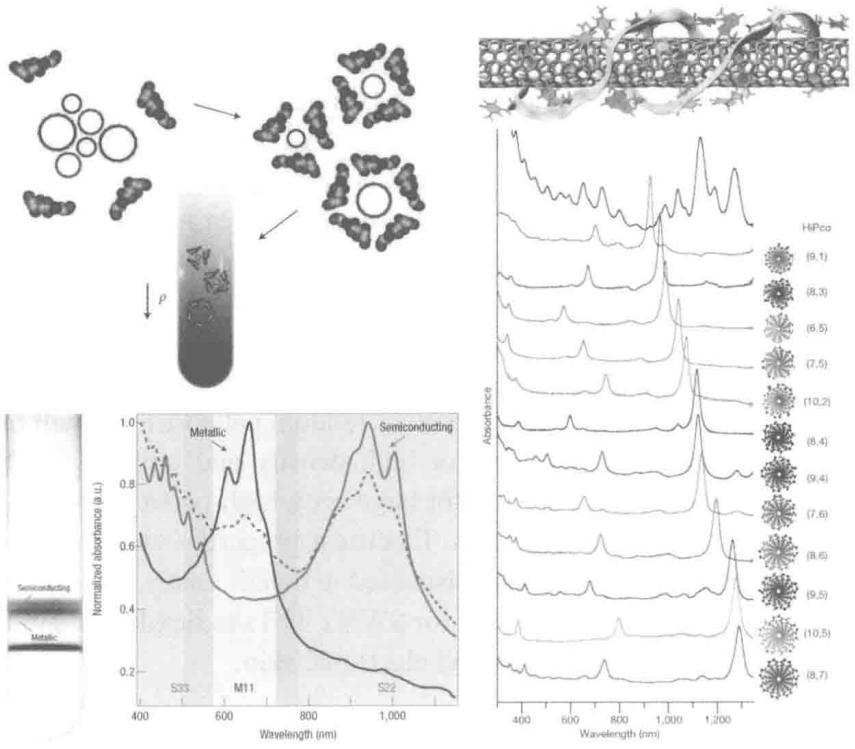
evaporation assembly,[54] spin coating[55–57] drop coating[58–63] and printing.[64–68] CVD-grown nanotube networks have been widely explored for TFTs (Fig. 2(a)) and medium scale flexible integrated circuits have been demonstrated by Rogers *et al.*[51] For this method, metal catalysts are typically deposited on the entire substrate using either evaporation or spin coating methods followed by CVD growth using hydrocarbon precursors such as methane, ethylene, ethanol, methanol etc. Despite the tremendous success in making flexible nanotube TFTs and circuits with promising electrical performance, the drawback is the existence of metallic nanotubes, which degrades the current on/off ratio of the devices. Although stripe-patterning (Fig. 2(a) right panel) has been proposed to improve the device on/off ratio by cutting the percolative transport through metallic paths in the transistors,[51] the channel length needs to be made relatively large in this case, limiting the degree of integration in the future. Dry filtration method (Fig. 2(b)) has been used by Ohno and co-workers to achieve high-performance flexible nanotube TFTs and D-flip-flop circuits.[53] In this method, SWNTs grown by plasma enhanced CVD are captured using a filter membrane and the density of the nanotubes can be easily controlled by the collection time. The collected nanotube networks can be subsequently transferred to fabrication substrates by dissolving the filter using acetone. The group at the IBM T.J Watson Research Center used a novel evaporation assembly method to obtain aligned nanotube strips with high purity semiconducting nanotubes (Fig. 2(c)).[54] Although submicron devices with good performance have been achieved, the scalability of this assembly method can be a potential problem. SWNT networks can also be obtained by dropping the nanotube solution onto a spinning substrate (Fig. 2(d)).[55] The drawback for this method is also scalability because the deposited SWNTs often align along different orientations depending on the location on the substrate, preventing wafer-scale fabrication with high uniformity. The other two solution-based SWNT assembly methods — drop coating (Fig. 2(e)) and printing (Fig. 2(f)) — are found to be more promising for large scale applications of nanotube TFTs. For the drop coating method, the substrates are first functionalized with amine-containing molecules, which are effective adhesives for SWNTs. By simply immersing the substrate into the nanotube solution, highly uniform nanotube networks can be obtained

throughout the wafer, enabling the fabrication of nanotube TFTs with high yield and small device-to-device variation.[59,60,62,63] Printing (Fig. 2(f)) represents another low-cost approach for fabricating large-scale nanotube TFTs and circuits where SWNT channel, electrodes, and gate dielectric can all be printed using ink-jet[64,65] or gravure printing[66–68] processes. This approach is useful for making cost-effective large-area nanotube circuits requiring only moderate performance as the resolution that can be achieved using printing process is generally lower than the conventional photolithography. Each of these methods discussed above presents unique opportunities and challenges. In this chapter, we will primarily focus on the use of semiconductor-enriched SWNT random networks. We will first discuss the assembly techniques for high density and uniform SWNT networks, and fabrication schemes for large-area, high-performance TFTs on mechanically flexible substrates. Electrical properties study and performance benchmarking will also discussed in detail. Lastly, we review a wide range of potential applications for SWNT TFTs in flexible integrated circuits, RF transistors, displays, and electronic skin.

2. Solution-Processed TFTs using Semiconductor-enriched SWNTs

2.1. *Nanotube Separation and TFT Fabrication*

As discussed in the previous section, one of the major challenges limiting the electronic applications of SWNTs is the coexistence of metallic and semiconducting nanotubes with roughly one third of the as-grown being metallic. The metallic SWNTs cause significant leakage current when the transistors are in the off state, and thus need to be selectively removed. As a result, high-purity semiconducting SWNTs have long been desired in order to achieve devices with high I_{on}/I_{off}. To address this problem, many groups have been actively working on nanotube separation based on electronic types. Hersam *et al.* proposed and demonstrated the use of density gradient ultracentrifugation (DGU) to achieve diameter,[69] electronic type,[70] or even chirality-based[71] separation. By mixing the pristine unsorted SWNTs with surfactants, a density gradient between metallic and semiconducting SWNTs is created and upon ultracentrifugation, the



(a) DGU (b) DNA-based chromatographic purification

Figure 3. (a) A density gradient between metallic and semiconducting SWNTs is created by mixing the pristine SWNTs with surfactants. Upon ultracentrifugation, the metallic and semiconducting nanotubes can be separated from each other as shown in the UV–Vis–NIR absorption spectra. Reproduced with permission from Ref. 70. (Copyright 2006 Nature Publishing Group.) (b) SWNTs with different chiralities can be separated by chromatographic purification by using DNA with different sequence motifs. Reproduced with permission from Ref. 72. (Copyright 2009 Nature Publishing Group.)

metallic and semiconducting nanotubes are separated from each other as shown in Fig. 3(a). In the photograph of the test tube, the brown band contains primarily semiconducting nanotubes and the green band contains mainly metallic ones. The high purity semiconducting and metallic nanotubes are further evidenced by the UV–Vis–NIR absorption spectra. Noteworthy, the semiconductor-enriched nanotubes are now commercially available, which makes it easy for research groups worldwide to explore device applications based on this purified material system. Even with high purity semiconducting nanotubes, there are still many different possible

chiralities, and thus different bandgaps. This factor can negatively affect the device performance and uniformity. In order to achieve chirality-specific purification of SWNTs, DNA modification with different sequence motifs have been used and purified SWNTs with different chiralities have been obtained using chromatographic purification (Fig. 3(b)).[72]

As described in the earlier section, solution-based deposition of the high purity semiconducting nanotubes at macroscales has been reported.[59,60,62,63] Most commonly, the substrates are first functionalized with amine-containing molecules or polymers such as aminopropyltrieth-oxysilane (APTES)[59,60] or poly-L-lysine[62,63] whose molecular structures are shown in Fig. 4(a). By dipping the substrate into APTES or poly-L-lysine, amine-terminated layers are formed on the SiO_2 surface which works as an effective adhesive layer for SWNTs (Fig. 4(b)). The amine-functionalized substrate is subsequently immersed into high-purity (up to 99%) semiconducting nanotube solution followed by deionized (DI) water and isopropanol rinse, and blow dry in nitrogen. Using the method described above, highly uniform SWNT random networks can be achieved at full wafer-scale. As shown in Fig. 4(c), the scanning electron microscopy (SEM) images taken at different locations on a 3-inch Si/SiO_2 wafer indicate that uniform nanotube deposition is achieved. The importance of substrate functionalization is clearly illustrated in Figs. 4(d) and 4(e). From the images, one can find that the samples with (Fig. 4(d)) and without (Fig. 4(e)) an adhesion layer exhibit rather drastic difference in terms of nanotube density and surface coverage.

Using the solution-deposited semiconductor-enriched nanotube thin-films, high performance TFTs can be fabricated on mechanically flexible substrates. A schematic illustration of a representative fabrication process is shown in Fig. 5(a). For the device fabrication on flexible substrates, polyimide is commonly explored, which can be spun coated and cured on a silicon handling wafer.[62,63,73] Polyimide is a high temperature plastic, allowing the dielectric layer and other passive components to be deposited at temperatures as high as 300°C. The fabrication process typically involves gate formation, dielectric deposition, nanotube deposition, source/drain formation, and unwanted nanotube etching (Steps 1–6 in Fig. 5(a).[63,73] Atomic layer deposition (ALD) is used to deposit high-κ oxide layers such as Al_2O_3, HfO_2, or ZrO_2 as the gate dielectric. For the

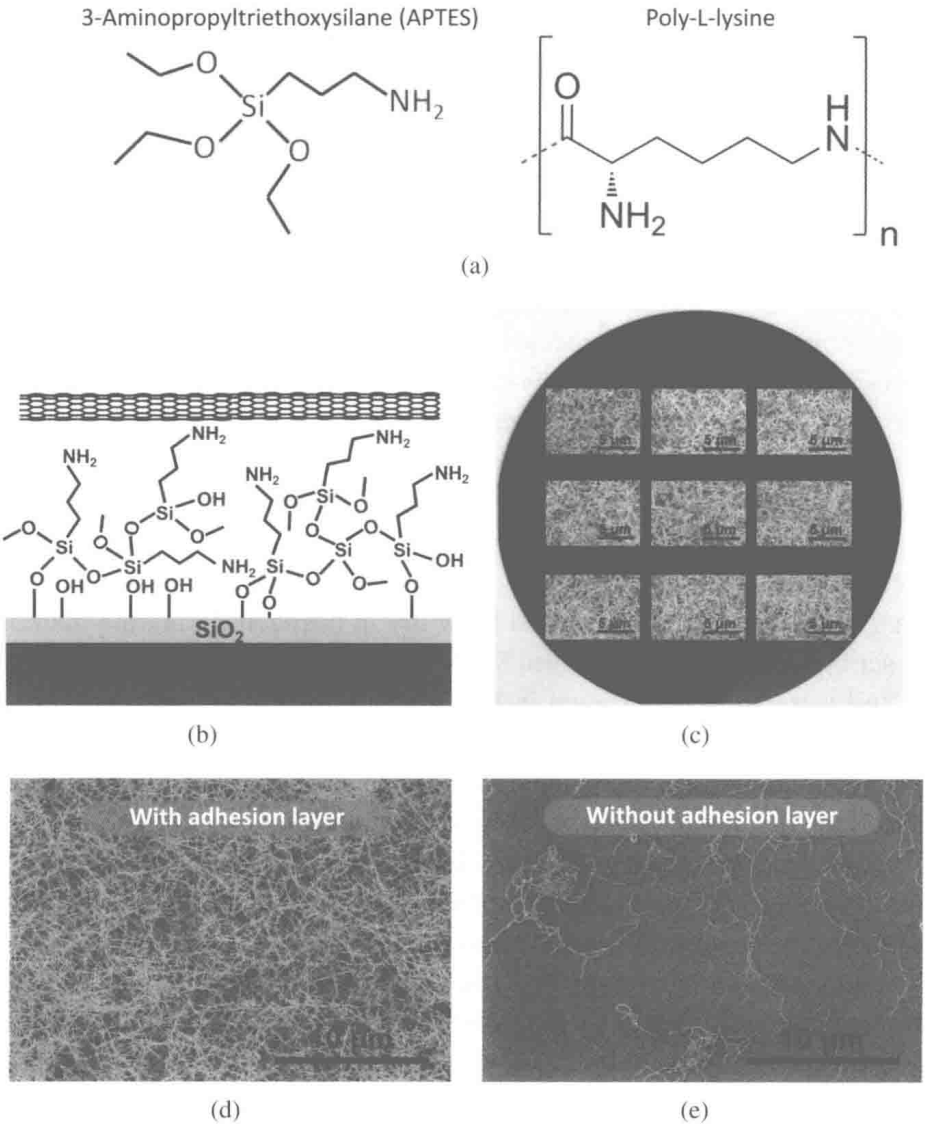


Figure 4. (a) Molecular structure of adhesive layers commonly used for large-scale semiconducting nanotube network deposition. (b) Schematic diagram of APTES-assisted nanotube deposition on Si/SiO_2 substrate. (c) SEM images showing that highly uniform nanotubes are deposited at different locations on a 3-inch Si/SiO_2 wafer. (d, e) SEM images of semiconducting nanotube networks deposited on Si/SiO_2 substrates with (d) and without (e) APTES functionalization. Reproduced with permission from Ref. 59. (Copyright 2009 American Chemical Society.)