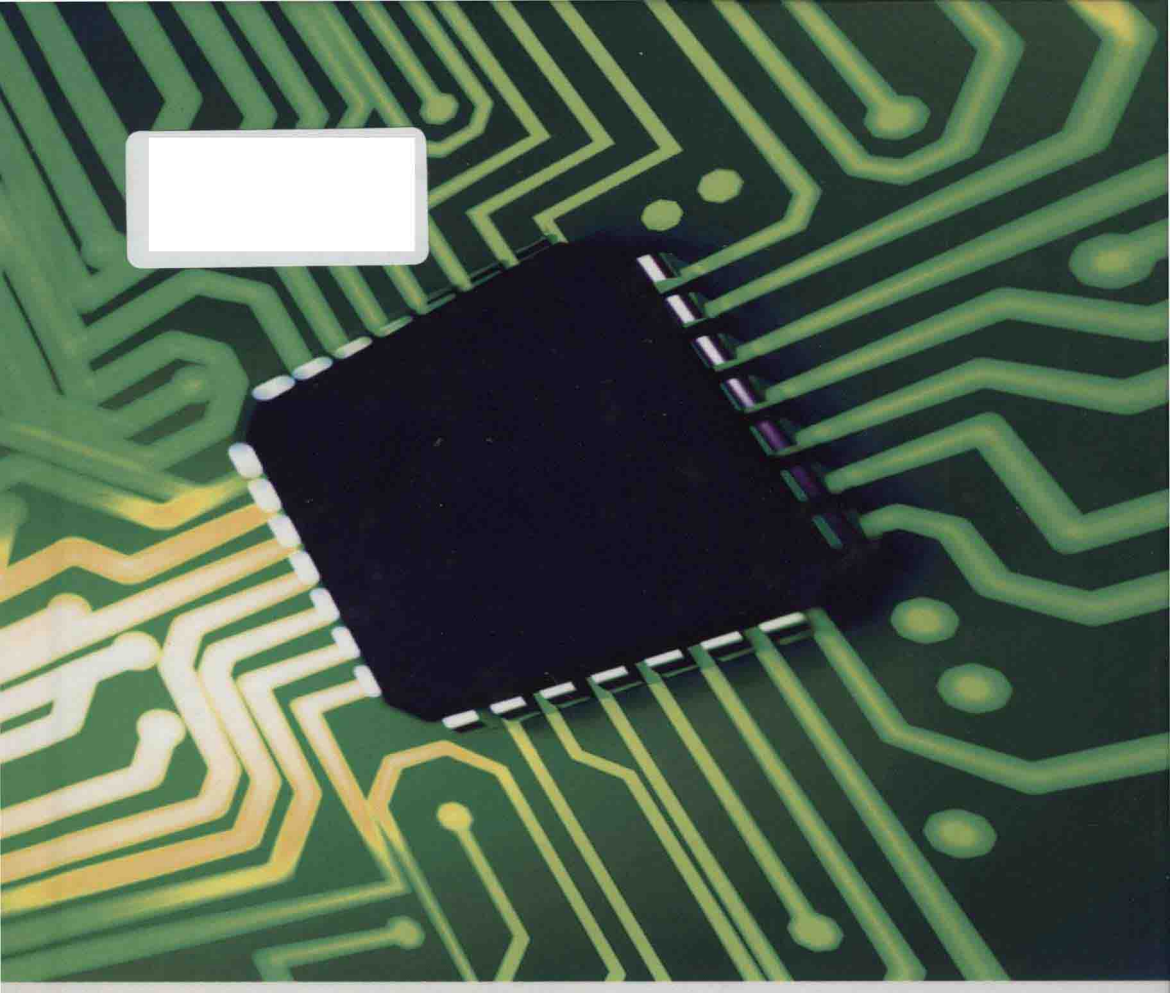

Plasma Etching Processes for Interconnect Realization in VLSI

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List of Acronyms

ARC	Anti-reflective coating
ATRP	Terpinene
BARC	Bottom anti-reflective coating
BEOL	Back-end-of-line
CCP	Capacitively coupled plasma
CD	Critical dimension
CMOS	Complementary metal oxide semiconductor
CMP	Chemical–mechanical planarization
CVD	Chemical vapor deposition
DEMS	Diethoxymethylsilane
DFCCP	Dual frequency capacitively coupled plasma
DMDCS	Dichlorodimethylsilane
DS	Downstream
EM	Electromigration
ER	Etch rate
ESL	Etch stop layer
FC	Fluorocarbon
FDSOI	Fully depleted silicon on insulator

FEOL	Front-end-of-line
FSG	Fluorine-doped silicon glass
FTIR	Fourier transform infrared spectroscopy
HDMS	Hexamethyldisilazane
HF	Hydrofluoric acid
HSQ	Hydrogen silesquioxane
IC	Integrated circuit
ICP	Inductively coupled plasma
ITRS	International Technology Roadmap for Semiconductor
MEOL	Middle-end-of-line
MER	Mass etch rate
MERIE	Magnetically enhanced reactive ion etcher
MHM	Metal hard mask
MOSFET	Metal oxide semiconductor field effect transistor
MSQ	Methyl silsesquioxane
MTBC	Mean time between clean
OTMSA	Trimethylsilylacetate
P4	Post-porosity plasma protection
PECVD	Plasma enhanced chemical vapor deposition
PL	Planarizing layer
PPLK	Photopatternable low-k
PR	Photoresist
RC	Resistive-capacitive
RF	Radio frequency
RIE	Reactive ion etching
RMS	Root mean square

SEM	Scanning electron microscopy
SOI	Silicon on insulator
TCP	Transformer coupled plasma
TDDB	Time-dependent dielectric breakdown
TEOS	Tetra ethyl ortho silicate
TFMHM	Trench first metallic hard mask
TMCS	Trimethylchlorosilane
TMDS	Tetramethyldisilazane
TMSDEA	Trimethylsilydiethylamine
ULK	Ultra low-k
UV	Ultra violet
VLSI	Very large scale integrated
VUV	Vacuum Ultraviolet
XPS	X-ray photoelectron spectroscopy

Preface

Electronics and information systems play an ever-increasing role in the worldwide economy. With a global income of $265 billion in 2008, the semiconductor industry contributed to more than $1,300 billion in the electronics industry and $5,000 billion in services, which represented nearly 10% of the gross domestic product. Electronics and information systems have penetrated and transformed all aspects of life, including transportation, communications, health and well being, government services, banking systems, entertainment and education.

Micro- and nanoelectronics are the key enabling technologies for electronics, information and communications technology, and as a result, the semiconductor market is increasing at double the rate of gross domestic product growth. The specific position of the microelectronics industry has been made possible by the constant downscaling of device dimensions, which increases the performance to fulfill the current societal needs in consumer electronics that can now be divided into two main paths: performance improvement and energy efficiency. For this, during the last 50 years, integrated circuits have evolved from a 100-transistors chip in 1966 to multibillion-transistors circuits in 2010, with the smallest device measuring less than 20 nm.

However, the problem with the constant downscaling in dimension is that the resistive–capacitive (RC) delay coming from interconnects has become the main issue for devices with high performance. That is

why copper-based interconnects have been introduced at the end of the 1990s to reduce the resistivity of wires, and low dielectric constant materials (low-k dielectrics) were introduced to deal with interconnects capacitance and signal propagation delay. But these changes have not been done without some difficulty.

Indeed, for the last 10 years, low-k dielectrics (i.e. materials with a lower dielectric constant than silicon dioxide) have evolved from fluorine-doped silicon glass (FSG; k = 3.2), to organosilicate (SiOCH; k = 3.0 and 2.7) and porous SiOCH (k = 2.55 and 2.4). Further decreasing the dielectric constant requires us to increase the porosity. Unfortunately, the presence of interconnected pores has amplified the dielectric sensitivity to plasma-based processes that are required for interconnects fabrication. It is thus impossible to define patterns in porous low-k materials without damaging their electrical properties with current etching technologies. Moreover, the mechanical strength of the dielectric, already significantly degraded by a decrease in network connectivity in SiOCH, is now reduced even further when porosity is added. For these reasons, technological roadmaps have constantly been revised and chip manufacturers are currently planning to step back to more robust dense materials with larger dielectric constant, thus degrading the global integrated circuits performance.

The goal of this book is to present the difficulties encountered for interconnect realization in very large-scale integrated (VLSI) circuits, especially focusing on plasma-dielectric surface interaction. After an introduction to interconnects presented in Chapter 1, we will see in Chapter 2 the sensitivity of low-k and ultra-low-k films to plasma etching and stripping steps which are the most critical steps in advanced interconnects realization. Then, in Chapter 3 we will present the various flows for dielectric films integration and their associated challenges. Finally, we will discuss in Chapter 4 the options to further reduce the dielectric constant for the future technological nodes.

Nicolas POSSEME
January 2015

Contents

1

Introduction

In 1947, the bipolar transistor was invented by Bardeen, Brattain and Shockley. Following this invention, in 1957, Kilby created five transistors simultaneously, forming the first integrated circuit (IC). In 1960, the first metal oxide semiconductor field effect transistor (MOSFET) on a silicon substrate with SiO_2 gate insulator was fabricated. The MOSFETs are slow compared to bipolar devices but are easier to fabricate and have a higher layout density. But both devices (bipolar and MOSFET) suffer from high power dissipation and have a restricted use in large integrated chip.

In 1963, the invention of the complementary metal oxide semiconductor (CMOS) marked a new milestone in the area of semiconductors. Indeed, the CMOS transistor has lower power dissipation and the possibility to integrate millions of CMOS transistors onto a chip. Since then, ICs have evolved from a 100-transistors chip in 1966 to multibillion transistors circuits in 2010, with the smallest device of less than 20 nm.

Semiconductor fabrication is composed of three major parts, front-end-of-line (FEOL), middle-end-of-line (MEOL) and back-end-of-line (BEOL), including different main steps such as deposition,

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Chapter written by Nicolas POSSEME and Maxime DARNON.

lithography, etching and cleaning. The whole process flow represents several hundreds of steps for the manufacturing of chips.

The FEOL processes correspond to isolation, gate patterning, spacer, extension and source/drain implantation, silicide formation and dual stress liner formation.

The MEOL is mainly gate contact formation, which becomes more and more challenging as device dimensions are reduced [MEB 14].

The BEOL allows transistor functionality by electrically interconnecting transistors. Interconnects are composed of insulating layers (dielectric) and metal levels. Interconnects (see Figure 1.1) are composed of several metal levels. Each metal level is composed of horizontal metallic lines connected to the lower and upper metal levels through short vertical lines called vias.

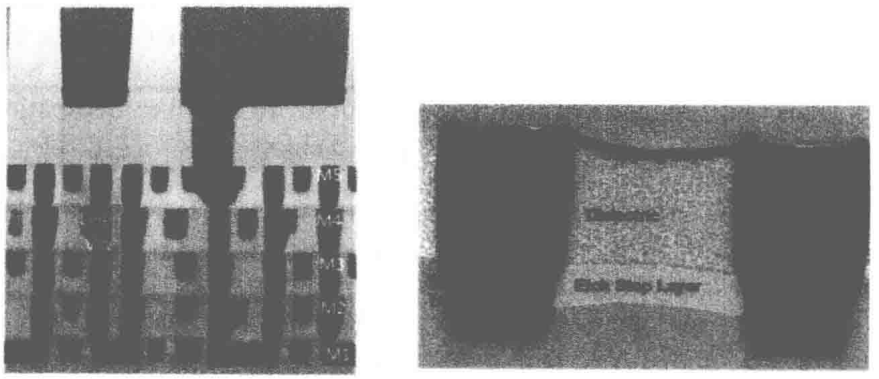

Figure 1.1. *Illustration of interconnects from metal 1 (M1) to metal 5 (M5) (left-hand side) and transverse cross section of two metal lines of a similar metal level (right-hand side)*

The combination of aluminum (Al) metal lines and silicon dioxide (SiO_2) as dielectric material has been used so far for interconnects in ICs. The problem lies with the constant downscaling in device