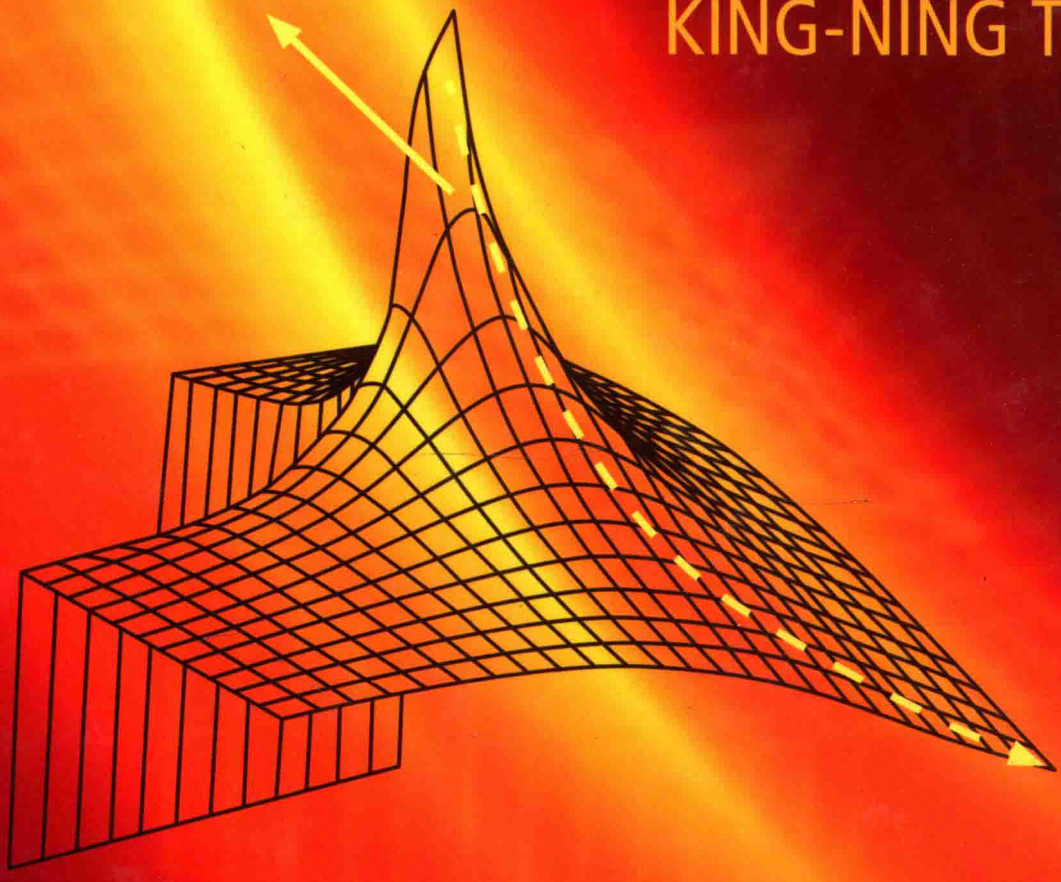
Electronic Thin-Film Reliability

KING-NING TU



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Electronic Thin-Film Reliability

Thin films are widely used in the electronic device industry. As the trend for miniaturization of electronic devices moves into the nanoscale domain, the reliability of thin films becomes an increasing concern. Building on the author's previous book, *Electronic Thin Film Science* by Tu, Mayer, and Feldman, and based on a graduate course at UCLA given by the author, this new book focuses on reliability science and the processing of thin films. Early chapters address fundamental topics in thin-film processes and reliability, including deposition, surface energy, and atomic diffusion, before moving on to systematically explain irreversible processes in interconnect and packaging technologies. Describing electromigration, thermomigration, and stress-migration, with a closing chapter dedicated to failure analysis, the reader will come away with a complete theoretical and practical understanding of electronic thin-film reliability. Kept mathematically simple, with real-world examples, this book is ideal for graduate students, researchers, and practitioners.

King-Ning Tu is a Professor in the Department of Materials Science and Engineering at the University of California at Los Angeles. Since receiving his Ph.D. in Applied Physics from Harvard University in 1968, he has gained 25 years' experience at IBM T.J. Watson Research Center as a Research Staff Member in the Physical Science Department. He is a Fellow of the American Physical Society, the Metallurgical Society, the Material Research Society, and an Overseas Fellow of Churchill College, Cambridge. He is also an academician of Academia Sinica of the Republic of China. Professor Tu has published over 450 journal papers, authored a book (*Solder Joint Technology*, 2007) and co-authored a textbook (*Electronic Thin Film Science*, 1992).

Dedicated to my wife, Ching Chiao Tu

Preface

The book is intended as a textbook for first and second year graduate students in the Department of Materials Science and Engineering. It can also be used as a reference book for self-study by engineers in the microelectronic industry. The early chapters in this book evolve from *Electronic Thin Film Science*, by K. N. Tu, J. W. Mayer, and L. C. Feldman, and published by MacMillan in 1993. The contents of this book have been taught in a graduate class on "Thin film materials science" at UCLA for over 15 years.

The emphasis in thin-film research is twofold: (1) to invent or to process new thin-film materials having useful functions in applications, and (2) to improve the reliability of functional thin films in large-scale applications, for example, in consumer electronic products. To achieve these goals, on the basis of the discipline of thin-film materials science, requires the study of correlation among structure—properties—processing—performance—reliability of thin films. There are textbooks on the processing of thin films, such as deposition methods by sputtering, electroplating, and MBE growth. There are also textbooks on characterization techniques such as SEM, TEM, RBS, XPS, UPS, Auger, and STM, etc. However, there is no textbook on thin-film reliability science.

When a technology is mature and in mass production, and has widespread application, reliability issues become crucial. As the trend of miniaturization of electronic devices moves into the nanoscale region, the reliability concern of nanotechnology will become serious in the near future. Reliability of nanotechnology may depend on the experience and understanding of reliability in microelectronic technology.

To have a reliable device, it is important to include the concept of reliability into the design and processing of materials in making the device. Thus, there is a strong link between the processing and reliability. It is the goal of this book to combine the science therein, but the emphasis will be on reliability.

What is reliability science? Typically, we tend to assume that the microstructure in a device is stable in its lifetime of usage. Unfortunately, this is not true. In most electronic applications, we must apply an electric field or an electric current. Under a high current density, electromigration occurs in the microstructure and induces circuit failure due to opening by void formation or shorting by extrusion. The high current density causes joule heating and the temperature rise will lead to thermal stress in the device between different materials having different thermal expansion coefficients. The stress gradient and temperature gradient, in addition to electromigration, may induce atomic diffusion and lead to microstructure change and phase transformations. Under a stress gradient or temperature gradient, it means that pressure or temperature is not constant. What is

unique in these changes is that they occur in the domain of non-equilibrium thermodynamics or irreversible processes. The basic science that is needed in order to develop an understanding of these reliability problems and to find a way to prevent them from occurring is reliability science.

At the start of the book, the fundamental subjects needed in thin-film processes and reliability such as deposition, surface energy, atomic diffusion, and elastic stress–strain in thin films will be reviewed. The essence of irreversible processes and entropy production will be covered in Chapter 10. This is followed by chapters on electromigration, thermomigration, and stress-migration, with a few examples of reliability failure. The final chapter will discuss failure analysis on the basis of both physical and statistical analyses. Appendixes A–G cover some of the very basic and useful topics and data related to this book.

It is worth mentioning that electromigration itself does not necessarily lead to microstructure failure. Only when there is atomic flux divergence in the microstructure may failure occur. Furthermore, even flux divergence is not enough to cause failure. We require a non-constant volume process in which lattice shift does not occur. In the absence of lattice shift, the non-constant volume change can lead to the generation of extra lattice sites which account for void and hillock or whisker formation.

In preparing the book, I have been helped greatly by students in my classes and in my research group. In particular, I would like to thank Miss Hsin-Ping Chen, Miss Tian Tian, and Mr. Daechul Choi at UCLA for typing part of the text, and revising figures and references. Mr. Choi proofread the book. I would also like to thank Professor Andriy M. Gusak at Cherkasy National University, Ukraine, for a review of Chapter 10 and Chapter 15. Appendix C on the derivation of electron windforce was taken from the lecture notes of Prof. Gusak. Research funding support on reliability study from NSF, SRC, National Semiconductor Corporation, Hitachi (Japan), Seoul Technopark (South Korea), and Advanced Semiconductor Engineering (Taiwan, ROC) is acknowledged.

King-Ning Tu, October 2009.

Contents

1 Thin-film applications to microelectronic technology

1.1 Introduction

Layered thin-film structures are used in microelectronic, opto-electronic, flat panel display, and electronic packaging technologies. A few examples are given below. Very large-scale integration (VLSI) of circuits on computer chips are made of multilayers of interconnects of thin metal films patterned into submicron-wide lines and vias. Semiconductor transistor devices rely on the growth of epitaxial thin layers on semiconductor substrates, such as the growth of a thin layer of p-type Si on a substrate of $n+$-type Si [1–3]. The gate of the transistor device is formed by the growth of a thin layer of oxide on the semiconductor. Solid-state lasers are made by sandwiching thin layers of light-emitting semiconductors between layers of a different semiconductor. In electronic and optical systems, the active device elements lie within the top few microns of the surface; this is the province of thin-film technology. Thin films bridge the gap between monolayer (or nanoscale structures) and bulk structures. They span thicknesses ranging from a few nanometers to a few microns. This book deals with the science of processing and reliability of thin films as they apply to electronic technology and devices [4]. To begin, this chapter describes the application of thin films to modern advanced technologies with examples.

1.2 Metal-oxide-semiconductor field-effect-transistor (MOSFET) devices

Advances in layered thin-film technology have been pivotal to the evolution of integrated circuits and opto-electronics. Today, we can fabricate hundreds of millions of transistors on a piece of Si chip the size of a fingernail. These transistors must be interconnected by thin-film lines to form circuits in order to function together. The basic circuit in a memory device is very simple. It consists of a transistor and a capacitor. A schematic cross-section of such a field-effect transistor is shown in Fig. 1.1, consisting of a transistor junction of $n+/p/n+$ type and a gate with a thin gate oxide over the p-type channel. The conductor on the gate is a bilayer structure consisting of a silicide and a heavily doped poly-Si, where the silicide is a metallic compound of metal and silicon. The $n+$ regions in the transistor junction are the source and drain regions and are connected by silicide contacts to the "word" line. Hence, silicide is used as a gate contact as well as source and drain contacts. There is a "bit" line connecting the source contact to the capacitor. The

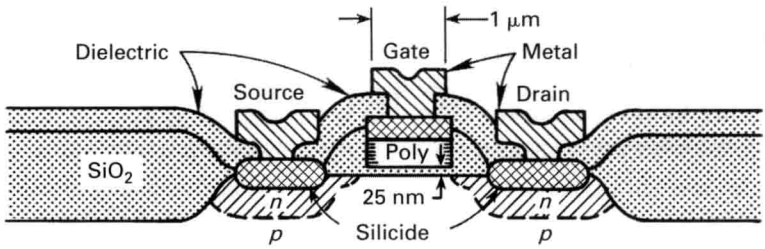

Fig. 1.1 Cross-section of a FET consisting of a transistor junction of $n+/p/n+$-type and a gate with a thin gate oxide over the p-type channel.

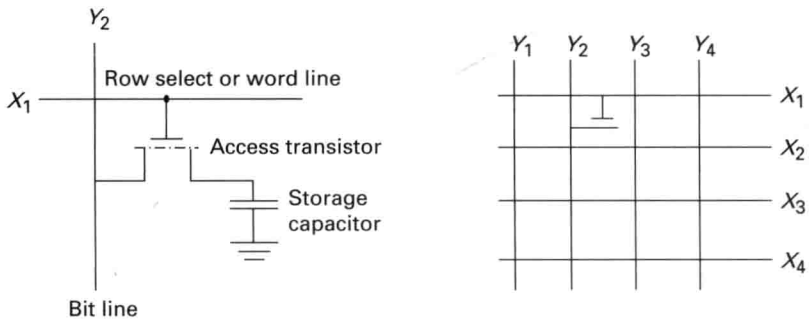

Fig. 1.2 Schematic diagram of an array of two-dimensional integrated circuits of MOSFET. Used with permission from *VLSI Technology*, S. M. Sze (1988), p. 494.

capacitor serves as a memory unit of either "1" (when the capacitor is full of charges) or "0" (when the capacitor is empty or stores no charge). The metal-oxide-semiconductor (MOS) field-effect transistor (FET) serves as a control (or gate) to allow the capacitor to discharge or not to discharge so that we can read or detect the two states of the capacitor, either full or empty [1–3].

Fig. 1.2 depicts an array of two-dimensional integrated circuits of MOSFET. In the x-coordinate, we have x_1, x_2, x_3, x_4, and so on, and in the y-coordinate, we have y_1, y_2, y_3, y_4, and so on. At each coordination point of (x, y), for example, take (x_1, y_2), we build a memory unit consisting of an FET and a capacitor. To operate the memory unit, a turn-on voltage is applied from the "word" line to open the gate. It attracts electrons to the p-type region and forms an inversion layer below the gate oxide. The inversion layer with electrons now electrically connects the two $n+$ regions. If the capacitor is full of stored charges, it will discharge so that a signal pulse can be detected at the end of the "bit" line. When this happens, we have identified a memory bit of "1" at the point (x_2, y_3). On the other hand, if the capacitor has no stored charges, there will be no discharge and no signal will be detected when we open the gate; then we have a memory bit of "0" at the point (x_2, y_3). The two-dimensional circuit integration as shown in Fig. 1.2 enables us to operate and detect every coordinate point on the two-dimensional integration of circuits, so it is called random access memory (RAM). Often, we use dynamic random

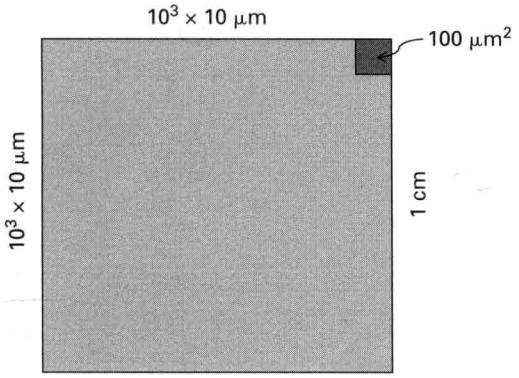

Fig. 1.3 Schematic diagram of a Si chip of size of 1 cm × 1 cm, divided into $10^3 \times 10^3 = 10^6$ small squares, so that each squares has an area 10 μm × 10 μm.

access memory (DRAM) to describe the device because the capacitors leak, since they are interconnected with lines, so we have to recharge them frequently and the recharge is a dynamic process. In certain devices, when the gate is isolated, we can use it as a floating gate.

In Fig. 1.3, we depict a Si chip of size 1 cm × 1 cm, and we divide it into $10^3 \times 10^3 = 10^6$ small squares, so that each of the squares has an area 10 μm × 10 μm. In each square, or cell area, if we can fabricate a FET and a capacitor, we have made a chip which has one million memory units. Needless to say, we should be able to interconnect them with their bit lines and word lines. In addition, we should also be able electrically to connect the chip to the outside circuit when we want to use it. The latter is a function of electronic packaging technology.

Next, we divide the 10 μm × 10 μm area into four smaller areas, i.e. cells about 5 μm × 5 μm. If we can shrink and build a FET and a capacitor in the smaller area, we will have a chip which has four million units of memory. This is the principle behind the miniaturization of the Si microelectronics industry in the last quarter century, or the essence of progress as suggested by Moore's law. The advance of one generation means the increase of a factor of four in circuit density on a chip. It goes from 1, 4, 16, 64, 256, to 1024 and so on. The industry started with about a one-thousand memory unit in the late 1960s and has advanced to about one billion memory units per chip today. Table 1.1 lists the dimensional changes of cells in several generations of devices. As the cell size becomes smaller, the feature size of the transistor, capacitor, and interconnects elements in the cell should also become smaller. There is a scaling law behind the shrinkage, which affects the electrical behavior of the transistor as well as the interconnect.

The VLSI of circuits is achieved by interconnecting all the transistors together using multilayers of Al or Cu thin-film interconnects. The process and reliability of multilayered thin-film interconnect structures are crucial to device applications. Today, there are eight or more layers of interconnects built on the transistors. Fig. 1.4 shows a scanning electron microscopic (SEM) image of a two-level Al interconnect on a Si surface after