



THE

MOS System

Olof Engström



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The cover image is an example of multi-parameter admittance spectroscopy (MPAS, Chapter 6) from an Al/HfO₂/Si structure as measured by Dr. Bahaman Raeissi.

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The MOS System

This detailed and up-to-date guide to modern MOS structures describes important tools, cutting-edge models, novel phenomena, and current challenges in measuring and improving the control of future MOS systems for transistor channels.

Building up from basic electrostatics, it introduces the ideal MOS system, physical and electrical properties of high- k oxides, their dielectric constants, and energy offsets to semiconductors and metals, before moving on to electrical and physical characterization methods for high- k dielectric materials. Finally, real MOS systems are introduced: high- k dielectrics and interlayers, the influence of phonon dynamics, interface states and bulk traps, effective metal work functions, gate leakage phenomena, and high mobility channel materials.

Abstract concepts are supported by practical examples and critical comparison, encouraging an intuitive understanding of the principles at work, and presented alongside recent theoretical and experimental results, making this the ideal companion for researchers, graduate students, and industrial development engineers working in nanoelectronics.

Olof Engström is Professor Emeritus of Microtechnology and Nanoscience, Chalmers University of Technology, Göteborg, Sweden, having formerly held positions in industrial high power devices, MOS technology and sensors. His research focuses on semiconductor quantum structures and interfaces. He is a member of the Royal Swedish Academy of Engineering Sciences and Societas Scientarum Fennica.

Preface

The motivation for writing this book has grown out of a feeling that a novel, compiled description of more recent results within the MOS area is needed after the often-cited work from 1982, *MOS (Metal Oxide Semiconductor) Physics and Technology*, by E. H. Nicollian and J. R. Brews (New York: John Wiley & Sons). Their work has been of extensive use within the MOS community. However, it only describes silicon dioxide structures and their approach follows a practical engineering path.

In the present text, I have included the most important consequences of using MOS insulators with higher dielectric constants, the so-called high- k oxides. Furthermore, since these insulators have given rise to new challenges from the point of view of materials physics, I have tried to start from a more physical basis. Still, my objective has been to write for a circle of readers including engineers, graduate students and researchers.

The book would not have come about without injections of inspiration from friends and colleagues, who have provided valuable discussion, help and up-to-date research during the preparation and writing of the text. Steve Hall and colleagues at the University of Liverpool, Ivona Mitrovic and Naser Sadeghi together with Henryk Przewlocki at the Institute of Electron Technology in Warsaw, and my former student, Bahman Raeissi, have filled in fuel and criticism for keeping up my typing. Specific and educational discussions on e-mail with Valery Afanas'ev, Douglas Buchanan, Jim Chelikowsky, Paul Hurley, Pat Lenahan, Winfried Mönch, Luca Selmi and Andre Stesmans are highly appreciated. Also, financial backing from the Department of Microtechnology and Nanoscience (MC2) at Chalmers is acknowledged together with the greatly valued assistance from colleagues of MC2 in keeping up my research during the writing period: Dag Winkler, Jan Stake, Peter Modh, Göran Petersson and Fredrik Henriksen.

Special thanks are directed to Julie Lanchashire, Mia Balashova and Elizabeth Horne at Cambridge University Press, for their patience with my continually postponed deadlines, and to David Hensley for linguistic assistance.

I dedicate this book to my wife, Anita, for her support and her persistence in living with a person, who for a long time has had an affair with his laptop.

Olof Engström

Contents

<i>Preface</i>	<i>page xi</i>
----------------	----------------

1	Introduction	1
1.1	The early days of MOS technology	1
1.2	Nature's freak of fate	2
1.3	Silicon dioxide becomes inadequate	2
1.4	High- k dielectrics	3
1.5	Characterizing the MOS system	4
1.6	Next episode	5
1.7	Overview of the subject	6

Part I Basic properties

2	Basic properties of the MOS system	11
2.1	Energy band diagram	11
2.2	Charges and potentials of the insulator	14
2.3	Charges and potentials of the semiconductor for an ideal MOS system	16
2.4	The capacitance of an ideal MOS system	21
2.4.1	The low-frequency capacitance	21
2.4.2	The high-frequency capacitance	24
2.5	Influence of insulator charge, insulator thickness and doping	25
2.6	The MOS capacitance at flatband	28
2.7	Influence of higher k -values	30
	References	31
3	Basic properties of the gate stack	32
3.1	High- k oxides with properties interesting for gate stacks	32
3.2	Properties required for gate oxides	34
3.3	The dielectric constant	38
3.3.1	A schematic case	38
3.3.2	An isotropic three-dimensional case	40
3.4	Energy barriers at interfaces including bandgap materials	43

3.5	The Schottky barrier	46
3.5.1	The Cowley–Sze model	46
3.5.2	Schottky barriers: chemical trends based on electronegativities	48
3.5.3	Origin of dipoles at the interface between metal and bandgap material	51
3.5.4	Chemical trends and Fermi-level pinning based on chemical reactivities	53
3.6	Energy band alignments of the MOS system	55
3.6.1	Metal/oxide barriers: induced gap states and the Cowley–Sze model	55
3.6.2	Semiconductor/oxide barriers: induced gap states and the Cowley–Sze model	59
3.6.3	Mönch’s model based on electronegativities	61
3.6.4	Ab initio calculations	62
3.6.5	Summary of energy barrier models	66
	References	68
4	Electron states at MOS interfaces	71
4.1	The influence of interface states	71
4.2	The canonical ensemble for describing an atomic system	71
4.3	The grand canonical ensemble for describing an electron system	74
4.4	An extended ensemble for describing the trap system	77
4.5	The influence of entropy	80
4.6	Charge carrier capture and emission at traps	85
4.7	Charge carrier generation at interface states	87
4.8	Creation of minority carriers at the oxide/semiconductor interface	90
4.9	Random telegraph signals from single traps	92
4.9.1	Single traps and the Ergodic Hypothesis	92
4.9.2	Statistics for single traps in MOSFET channels	94
4.10	Validity of thermal emission measurements performed on depletion regions	95
4.11	Recombination at oxide/semiconductor interfaces	98
	References	101
5	Carrier capture at bulk oxide traps	104
5.1	Background	104
5.2	Occupation statistics for bulk oxide traps	104
5.3	Thermal and optical processes of vibrational traps	108
5.4	Injection processes followed by capture	109
5.5	Capture mechanisms	112
5.6	Injection probability at electrical potential distributions for high- k structures with an interlayer	113
5.7	Capture at multi-electron traps	116
5.8	Analysis of electron injection	119
5.9	Computed results	121
	References	126

Part II Characterization techniques

6	Electrical characterization by Fermi-probe technique	131
6.1	Capacitance contribution from interface states	131
6.2	Charge carrier dynamics leading to interface state admittance	134
6.3	Admittance contribution from interface states	136
6.4	Influence from circuit elements: measured quantities	138
6.5	Influence from D_{it} and σ_n distributions	139
6.6	High-frequency $C-V$ technique	141
6.6.1	The influence of interface states	141
6.6.2	High-frequency $C-V$ curves for three cases of D_{it}	141
6.6.3	Capture cross sections obtained from the high-frequency $C-V$ technique	145
6.6.4	D_{it} obtained from high-frequency $C-V$ data	149
6.7	Low-frequency $C-V$ technique by the quasi-static method	151
6.8	The conductance method	153
6.9	Multiparameter admittance spectroscopy	157
6.9.1	The methodology	157
6.9.2	Influence of interface states on MPAS appearance	157
6.10	Charge pumping	159
6.10.1	The methodology	159
6.10.2	Statistics for the charge pumping cycle	162
	References	167
7	Electrical characterization by thermal activation	168
7.1	Thermally stimulated current method	168
7.1.1	Basic principle	168
7.1.2	TSC for investigating border traps	168
7.2	Deep level transient spectroscopy	173
7.2.1	Basic principle	173
7.2.2	Constant capacitance DLTS for investigation of MOS interface states	179
7.2.3	Capacitance-controlled DLTS by lock-in filtering	186
7.2.4	Limitations in DLTS for investigation of MOS interfaces	187
7.3	Conductance method for measuring thermal activation energies	189
	References	194
8	Characterization of oxide/silicon energy band alignment: internal photoemission and X-ray photoelectron spectroscopy	196
8.1	Internal photoemission	196
8.1.1	Basic principles	196
8.1.2	The photocurrent	197
8.1.3	The influence of absorption length and escape length	199
8.1.4	The emission probability $P(E)$	200

8.1.5	Image force barrier lowering	201
8.1.6	IPE yield for silicon MOS structures	203
8.1.7	Influence of interlayers and tunneling	210
8.2	X-ray photoelectron spectroscopy	212
8.2.1	Basic principles	212
8.2.2	XPS for determination of energy offset values in MOS structures	213
8.2.3	Charging effects	215
8.2.4	Influence of interlayers	216
	References	219
9	Electron spin-based methods	221
9.1	Electron spin resonance	221
9.1.1	Basic principles	221
9.1.2	The coupling between magnetic field and spin	222
9.2	Hyperfine interaction	225
9.3	Spin-dependent recombination at interface states	225
	References	227
 Part III Real MOS systems		
10	MOS systems with silicon dioxide dielectrics	231
10.1	Engineering efforts at the dawn of MOS technology	231
10.2	The Deal–Grove oxidation model	231
10.3	Atomic structure and properties of the silicon/silicon dioxide interface	234
10.4	Influence of the atomic structure on electrical properties of SiO _x /Si systems	240
10.5	Interface states	241
10.5.1	The influence of interface states on transistor performance	241
10.5.2	The P _b center	242
10.5.3	Relation between the P _b center and density of interface states	243
10.5.4	Trapping properties of interface states	246
10.5.5	Passivation and de-passivation of interface states	248
10.5.6	Dissociation kinetics of the P _b center	252
10.6	Bulk oxide traps: the E' center	255
	References	256
11	MOS systems with high-<i>k</i> dielectrics	261
11.1	The motivation for high- <i>k</i> dielectrics	261
11.2	The dielectric constant for high- <i>k</i> oxides	264
11.2.1	Transition, rare-earth and ternary oxides	264
11.2.2	Relationship between the <i>k</i> -value and phonon dynamics	266
11.2.3	<i>k</i> -value of crystalline structures	270
11.3	The interlayer	272
11.4	Remote carrier scattering in transistor channels	275

11.5	Energy offset values between silicon and high- k oxides	276
11.6	Interface states	277
11.7	Bulk oxide traps	287
11.7.1	Theoretical treatment of oxygen vacancies in cubic HfO_2	287
11.7.2	Polarons and self-trapping	289
11.8	Chemical stability	291
	References	293
12	Gate metals	297
12.1	Metal properties influencing the transistor threshold voltage	297
12.2	The Schottky barrier and effective work function of metal/high- k oxide structures	299
12.3	Tuning the metal/oxide energy barrier	303
12.3.1	Relationship between annealing and metal work function: an example	303
12.3.2	Influence of oxygen vacancies on effective work function	305
	References	306
13	Transmission probabilities and current leakage in gate oxides	308
13.1	The concept of tunneling	308
13.2	The WKB approximation	310
13.2.1	Derivation of the transmission probability	310
13.2.2	The influence of image force	313
13.3	Direct and Fowler–Nordheim tunneling in the WKB approximation	314
13.4	Tunneling involving traps	315
13.4.1	Tunneling through a trap potential	315
13.4.2	Tunneling probabilities for trap assisted tunneling	317
13.4.3	Poole–Frenkel effect	320
13.5	Gate leakage by tunneling	325
13.5.1	Direct tunneling current for a single-layer oxide	325
13.6	Tunneling through high- k oxides with interlayers	327
	References	330
14	MOS systems on high-mobility channel materials	333
14.1	Motivation for high-mobility channel materials in MOSFETs	333
14.2	MOS systems on III–V materials	334
14.2.1	N-channels built in InGaAs	334
14.2.2	Interface states at III–V semiconductor/oxide interfaces	336
14.2.3	Energy band alignment at oxide/ $\text{In}_{1-x}\text{Ga}_x\text{As}$ interfaces	339
14.3	MOS systems on silicon- and germanium-based materials	341
14.3.1	Channels built on Ge and SiGe	341
14.3.2	Energy band alignment at oxide/Ge interfaces	343
	References	348
	<i>Index</i>	352

1 Introduction

1.1 The early days of MOS technology

In the past couple of decades, the increasing influence of electronics on human life has promoted MOS technology to a role of similar significance for cultural change as, for example, electric power transmission and combustion engine transport. The basic device for this development, the metal–oxide–semiconductor field-effect transistor (MOSFET), was patented in 1928 by Lilienfeld. The invention had to wait for realization until 1961 when Khang at Bell Telephone Labs first demonstrated a working device. Until then, one of the main hurdles for implementing Lilienfeld's idea was finding a material combination such that a surface channel for charge carriers could be brought about by an external electric field. A charge-free surface or interface was needed, which required a structure free of charge carrier traps. Here, silicon technology opened new possibilities. By thermally oxidizing the surface of silicon crystals into SiO_2 , an insulator was obtained with eminent properties and with a low concentration of traps at the SiO_2/Si interface and in its volume. At the beginning of the 1960s, a considerable amount of work was performed to optimize the properties of SiO_2 prepared this way and to understand the metal–oxide–semiconductor system. Important contributions to the understanding of the MOS system came from a group of William Shockley's former disciples at Fairchild Semiconductor in Palo Alto. In the same period, activities were also initiated at the IBM Thomas Watson Research Center, at the Bell labs and at some universities in the USA.

In parallel with this research on silicon dioxide, the MOSFET was developed. When a voltage is applied to the gate electrode of a MOS structure, a bending of the semiconductor energy bands occurs such that charge carriers can be injected from a source contact and collected by a drain contact on the opposite side of the gate. A channel is then opened at the Si/SiO_2 interface, and the current between source and drain can be regulated by the voltage on the gate, producing transistor action. After mastering the materials problems, this ingenious and simple geometrical design conquered other technologies for logic circuitry. The tremendous development potential of the device can be realized by considering that the channel lengths of the original MOSFETs were tens of microns while in today's transistor development, the corresponding distance is a couple of tens of nanometers. This was the ramp that launched the expansion of communications and computation present everywhere in global society today. At the time of writing this book, no serious competing device structure has been

proposed to replace the MOSFET for future applications. Observers of the field forecast that MOS technology will continue to dominate electronics applications for the foreseeable future.

1.2 Nature's freak of fate

As the MOS system operates by creating a channel between the insulator and the semiconductor for charge carrier transport, this sets high demands on the degree of perfection at this interface. Oxides used as the insulator material are generally amorphous, while the semiconductor material is crystalline. Therefore, the atomic structure at the interface between these two material types contains geometrical misfits, and thus imperfections due to open electron orbitals, which give rise to electron traps. Such “dangling bonds” are important sources of charge at insulator/semiconductor interfaces and influence the transport and stability properties of MOSFETs. At its beginning and for a long period of time, the whole MOS concept was leaning on the possibility to prepare the gate oxide by thermal oxidation of the silicon crystal surface. By a freak of nature, the SiO_2/Si interface built up that way. Not only existed a semiconductor material based on an element with a high abundance on earth, with a crystal structure of high mechanical strength and an energy bandgap well suited for electronic applications, but its natural oxide was almost perfect for use as an insulator! These materials properties together with the simple and flexible design of the MOSFET are the linchpins that have carried MOS technology to its present position.

1.3 Silicon dioxide becomes inadequate

In the downscaling of device dimensions, which in the past four or five decades has roughly followed Moore's law and resulted in a rapidly increasing number of transistors per chip, one of the main issues has been to design the properties of the transistor channel. Decreasing the distance between source and drain, thus making the depletion regions of these two p-n junctions approach each other, gives rise to increased current leakage and decreased threshold voltage. This problem, known as the “short channel effect” and occurring for each new technology generation, was solved by introducing sophisticated doping geometries for the source and drain contacts and by increasing the channel doping. However, the latter measure, which serves to decrease transistor leakage, has a detrimental influence on the capacitive coupling between the gate and the channel. This in turn influences the ability of the transistor to switch between its on- and off-states.

The switching capacity is one of the most important properties of the MOSFET. It depends on the characteristics of the MOS system constituting the gate/channel combination. For a given change in gate voltage, a high share needs to be supplied to the semiconductor in order to flip its energy bands efficiently and create or eliminate the channel. This voltage partition depends on the relation between the capacitances

of the gate oxide and of the channel region, respectively. A high ratio between these two quantities is desirable. However, increasing the channel doping in order to solve the problem of the short channel effect will increase the channel capacitance for a given voltage drop and thus impair the semiconductor's switching capability. The remedy is to increase the oxide capacitance. If SiO_2 is kept as the insulator material, this means that its thickness needs to be decreased. Such steps were part of transistor development until the SiO_2 layer thickness approached the lower limit of about 1.5 nm, where the leakage current between gate and channel could no longer be accepted. At this point, the way to proceed included the use of oxynitrides, thus increasing the dielectric constants a couple of units from the value of 3.9 for SiO_2 . For a couple of technology generations, this allowed the use of a thicker insulator with high enough capacitance and low enough leakage. Finally, in order to be able to continue into channel lengths shorter than about 40 nm, SiO_2 -based gate insulators could no longer be used. A drastic step had to be taken by changing to materials based on elements from other parts of the periodic table, the so-called "high- k " dielectrics, where k stands for the dielectric constant. The first development in this area was made for the 45 nm CMOS node, where a "hafnium-based" oxide was used. For the continued race of downscaling, therefore, the problem of finding new gate insulator materials will be one of the most important issues.

This necessary turn into novel materials for MOS development has been reflected in other parts of the transistor architecture. In the early period of this technology escalation, the atomic species used were mainly silicon, oxygen, aluminum, boron, arsenic and phosphorus. Prerequisites of more recent progress have been the use of, for example, copper and low- k materials for interconnects, and silicides based on various metals and different metal combinations for gate contacts; the search for novel metal oxides has included a large part of the transition and rare-earth metal range of the periodic system.

1.4 High- k dielectrics

The search for suitable materials to satisfy the gate functions of future MOS transistors has led the scientific semiconductor community on a quest through the periodic system to find the "Dielectric Grail." The goal is a material with acceptable energy offset values between the energy bands of the dielectric and the silicon crystal while, at the same time, having a high enough dielectric constant. The former quantity influences leakage for a given thickness, the latter secures channel coupling for a given leakage. So far for CMOS applications, most of the efforts have been limited to metal oxides. The change from the extremely well-mastered thermal SiO_2 material to an oxide based on metals among the transition or rare-earth series has revealed obstacles that were unnoticeable using traditional technology. As well as problems of chemical stability between these new "high- k " oxides and the silicon substrate, issues of crystallization, sensitivity to humid environment, higher concentrations of oxide traps and interface states have been encountered. Driven by technology, this has made it important to understand their microscopic properties from the chemical, physical and electrical points of view.

A common attribute of high- k oxide films deposited on silicon is the occurrence of an SiO_x interlayer between the high- k material and the silicon crystal. This evokes interface electron state properties similar to those at thermal SiO_2/Si interfaces. Even if the interlayer lowers the effective k -value of the film, it often gives better conditions for a transistor channel than those offered by a direct interface due to lower charge carrier scattering by the former. However, it must be paid for by an extra interface between the SiO_x and the high- k material. As the total physical thickness of the film is in the range of a couple of nanometers, on this length scale the transition from SiO_x to the high- k material can hardly be considered abrupt. It is found to include a transition region with undefined stoichiometry and thus with possible structural instabilities.

In order to use a convenient measure when comparing the thicknesses of insulators with different dielectric constants, the concept of “equivalent oxide thickness” (EOT) has been introduced. This is the thickness that a layer of SiO_2 would have for the same capacitance as a certain high- k layer. In order to fulfill the demands on transistors for the 22 nm node and beyond, the EOT values must be below 1 nm. The SiO_x interlayer has a k -value of roughly that same magnitude as SiO_2 and decreases the effective dielectric constant for the entire high- k stack. As it often appears with a thickness of about 1 nm, it must be eliminated in future applications. One possible solution to this problem has been the replacement of SiO_x by silicate.

1.5 Characterizing the MOS system

As the MOS system constitutes a capacitive device, a natural way to investigate its properties from an electrical point of view is by studying its admittance. From such measurements, capacitance and conductance as functions of voltage and frequency can be extracted and used as diagnostic data. Information about the properties of interface states and oxide charge can also be deduced from such results. Consequently, two traditional methods in wide use for MOS characterization are the capacitance versus voltage (C - V) and the “conductance method.” In the pioneering work of the 1960s on understanding the physical properties of MOS structures, the C - V method was used to establish the main qualities of oxide/silicon interfaces. Based on this tool, the importance of interface state densities and oxide charge were revealed. Later, this technique was joined by the conductance method, where the real part of the MOS admittance was shown to complete data from the C - V method. From these initiatives, a number of variations and a huge amount of applications have blossomed for a continued detailed understanding of the technologically useful MOS structure.

The conductance method has lived through a discursive development after the first preliminary study, published in 1965 by Nicollian and Goetzberger. In that original work, the interpretation of measured data was oversimplified and a more realistic treatment followed by the same authors in a later published paper. The conductance method is based on resonance phenomena between the frequency of a probing voltage from the measurement set-up and the rate by which charge carriers are emitted from and captured to interface states. From such data, interface state densities and capture cross