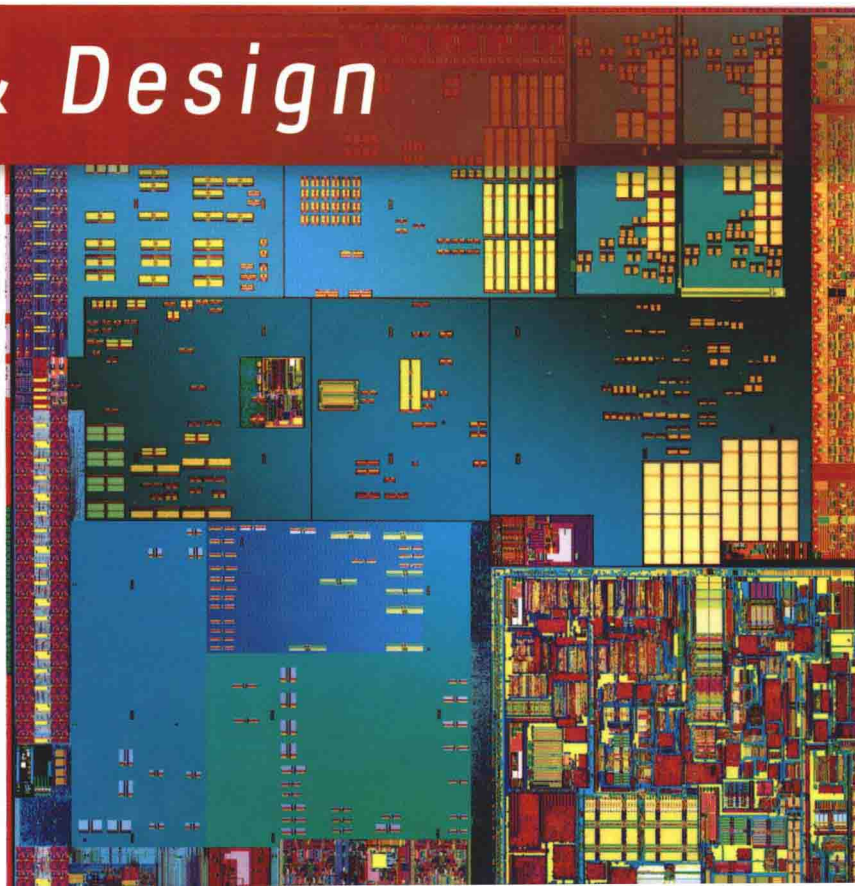
# CMOS Digital Integrated Circuits

4th Edition

## Analysis & Design



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# CMOS Digital Integrated Circuits

## *Analysis and Design*

**Fourth Edition**

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# CMOS Digital Integrated Circuits

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**Chulwoo Kim** received BS and MS degrees in electronics engineering from Korea University, and a PhD in electrical and computer engineering from the University of Illinois at Urbana-Champaign. In 1999, he worked as a summer intern at

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Dr. Kim received the Samsung HumanTech Thesis Contest Bronze Award, the ISLPED Low-Power Design Contest Award, the DAC Student Design Contest Award, the SRC Inventor Recognition Award, the Young Scientist Award from the Ministry of Science and Technology of Korea, the Seoktop Award for excellence in teaching, and the ASP-DAC Best Design Award. He is currently on the editorial board of *IEEE Transactions on VLSI Systems* and on the Technical Program Committee of the IEEE International Solid-State Circuits Conference.

# PREFACE

Complementary metal oxide semiconductor (CMOS) digital integrated circuits are the enabling technology for the modern information age. Because of their intrinsic features in low-power consumption, large noise margins, and ease of design, CMOS integrated circuits have been widely used to develop random access memory (RAM) chips, microprocessor chips, digital signal processor (DSP) chips, and application-specific integrated circuit (ASIC) chips. The popular use of CMOS circuits continues to grow with the increasing demands for low-power, low-noise integrated electronic systems in the development of mobile computing platforms, wearable communication devices, smart phones, and multimedia systems.

Since the field of CMOS integrated circuits is broad, it is conventionally divided into digital CMOS circuits and analog CMOS circuits. This textbook is focused on the CMOS digital integrated circuits. However, it should be noted that the boundary between classical digital and analog CMOS design is becoming increasingly blurred, especially with the challenges presented by nanometer-scale fabrication technologies, very low operating voltages, and operating frequencies extending well into the multi-GHz range. Therefore, we attempt to present the analysis and design of digital CMOS integrated circuits from an "analog" point-of-view, i.e., taking into account the analog, non-discrete nature of the devices and circuits that are used to implement digital functions.

The origins of this textbook date back to the early 1990s, when the first two authors were intensively involved in undergraduate- and graduate-level teaching of digital IC fundamentals. At the University of Illinois at Urbana-Champaign, where both of us were teaching at the time, we tried some of the available textbooks on digital MOS integrated circuits for our senior-level technical elective course, ECE382—Large Scale Integrated Circuit Design. Students and instructors alike realized, however, that there was a need for a new book with more comprehensive treatment of CMOS digital circuits. Thus, our textbook project was initiated several years ago by assembling our own lecture notes. Since 1993, we have used evolving versions of this material at the University of Illinois at Urbana-Champaign, at Istanbul Technical University, at Worcester Polytechnic Institute, and at the Swiss Federal Institute of Technology in Lausanne. We are both encouraged by comments from our students, colleagues, and reviewers. The first edition of *CMOS Digital Integrated Circuits: Analysis and Design* was published in late 1995.

Soon after publishing the first edition, we saw the need for updating it to reflect the many constructive comments we were receiving from instructors and students who used the textbook. We intended to include and update important topics such as low-power circuit design and interconnects in high-speed circuit design, as well as the deep submicron circuit design issues, and to provide more rigorous treatment of new developments in memory circuits. We also felt that in a rapidly developing field such as CMOS

digital circuits, the quality of a textbook can only be preserved by timely updates reflecting the state of the art. This realization has led us to embark on the successive revisions of our work, with the second edition appearing in 1998 and the third edition in 2002, to reflect the advances in technology and in circuit design practices.

During the 11 years that have passed since the publication of the third edition in 2002, the domain of CMOS digital integrated circuits has continued to grow and develop at an ever-increasing pace. The advent of nanometer-scale technologies and the widespread use of system-on-chip architectures combining a large number of functional blocks on chip have ushered in dramatic changes in the way digital CMOS integrated circuit design has to be treated. Thus, we came to the conclusion that incremental revisions would no longer do justice for the next edition of this textbook, and that we needed a comprehensive rewriting of virtually all chapters. The author team was expanded by the valuable addition of Professor Chulwoo Kim of Korea University, and an extensive revision was embarked upon. The fourth edition is the outcome of this intensive effort.

*CMOS Digital Integrated Circuits: Analysis and Design* is intended primarily as a comprehensive textbook at the senior level and first-year graduate level, as well as a reference for practicing engineers in the areas of integrated circuit design, digital design, and VLSI. Recognizing that the area of digital integrated circuit design is evolving at an increasingly faster pace, we have made our best effort to present up-to-date materials on all subjects covered. This textbook contains 15 chapters; we recognize that it would not be possible to cover rigorously all of this material in one semester. Thus, we would propose the following based on our teaching experience: At the undergraduate level, coverage of the first 10 chapters would constitute sufficient material for a one-semester course on CMOS digital integrated circuits.

Time permitting, some selected topics in Chapter 11, "Low-Power CMOS Logic Circuits," Chapter 12, "Arithmetic Building Blocks," and Chapter 13, "Clock and I/O Circuits" could also be covered. Alternatively, this book could be used for a two-semester course, allowing a more detailed treatment of advanced issues, which are presented in the later chapters. At the graduate level, selected topics from the first 10 chapters plus the last 5 chapters can be covered in one semester.

The first 8 chapters of this textbook are devoted to a detailed treatment of the MOS transistor with all its relevant aspects; to the static and dynamic operation principles, analysis, and design of basic inverter circuits; and to the structure and operation of combinational and sequential logic gates. Note that the introduction chapter has been significantly expanded to include a detailed presentation of VLSI design methodologies. Since the digital integrated circuit design techniques discussed in the first half of this textbook are directly relevant for digital VLSI and ASIC design, we felt that the context should be presented at the beginning of the book. The issues of on-chip interconnect modeling and interconnect delay calculation are covered extensively in Chapter 6, which provides a complete view of switching characteristics in digital integrated circuits. A separate chapter (Chapter 9) has been reserved for the treatment of dynamic logic circuits, which are used in state-of-the-art VLSI chips. Chapter 10 has been completely revised in both content and presentation; it offers an in-depth presentation of many state-of-the-art semiconductor memory circuits.

Recognizing the increasing importance of low-power circuit design, we dedicate one chapter (Chapter 11) to low-power CMOS logic circuits, which provides a comprehensive coverage of methodologies and design practices that are used to reduce the power dissipation of large-scale digital integrated circuits. Key arithmetic building blocks are presented in Chapter 12, with an emphasis on high-performance multibit adders and multipliers.

Next, Chapter 13 provides a clear insight into the important subjects of clocking and chip I/O design. Critical issues such as ESD protection, clock distribution, clock buffering, and latch-up phenomena are discussed in detail. Finally, the more advanced but important topics of design for manufacturability and design for testability are covered in Chapters 14 and 15, respectively.

We have long debated the coverage of nMOS circuits in this textbook. We have concluded that some coverage should be provided for pedagogical reasons. Thus, to emphasize the load concept, which is still widely used in many areas in digital circuit design, we present basic resistive-load and pseudo-nMOS inverter circuits along with their CMOS counterparts in Chapter 5, while we present pseudo-nMOS logic gates (NAND/NOR) in Chapter 7.

The Online Learning Center for this edition (www.mhhe.com/kang) also contains:

- An Instructors Manual
- Lecture Slides (PowerPoint and PDF)
- Cadence™ Design Tutorial
- Color Plates.



Although an immense amount of effort and attention to detail were expended to prepare the camera-ready manuscript, this textbook may still have some flaws and

mistakes due to erring human nature. We welcome and greatly appreciate suggestions and corrections from readers for the improvement of technical content as well as the presentation style.

## ACKNOWLEDGMENTS TO THE FIRST EDITION

Our colleagues have provided many constructive comments and encouragement for the completion of the first edition. Professor Timothy N. Trick, former head of the department of electrical and computer engineering at the University of Illinois at Urbana-Champaign, has strongly supported our efforts from the very beginning. The appointment of Sung-Mo Kang as an associate in the Center for Advanced Study at the University of Illinois at Urbana-Champaign helped to start the process. Yusuf Leblebici acknowledges the full support and encouragement from the department of electrical and electronics engineering at Istanbul Technical University, where he introduced a new digital integrated circuits course based on the early version of this book and received very valuable feedback from his students.

Yusuf Leblebici also thanks the ETA advanced Electronics Technologies Research and Development Foundation at Istanbul Technical University for their generous support. Professor Elyse Rosenbaum and Professor Resve Saleh used the early versions of the manuscript as the textbook for ECE382 at Illinois and provided many helpful comments and corrections, which have been fully incorporated with deep appreciation. Professor Elizabeth Brauer, currently at Northern Arizona University, has also done the same at the University of Kentucky.

The authors would like to express sincere gratitude to Professor Janak Patel of the University of Illinois at Urbana-Champaign for generously mentoring the authors in writing Chapter 15, "Design for Testability." Professor Patel has provided many constructive comments, and many of his expert views on the subject are reflected in this chapter. Professor Prith Banerjee of Northwestern University and Professor Farid Najm of the University of Illinois at Urbana-Champaign also provided many good comments. We would also like to thank Dr. Abhijit Dharchoudhury for his invaluable contribution to Chapter 14, "Design for Manufacturability."

Professor Duran Leblebici of Istanbul Technical University, who is the father of the second author, reviewed the entire manuscript in its early development phase, and provided very extensive and constructive comments, many of which are reflected in the final version. Both authors gratefully acknowledge his support during all stages of this venture. We also thank Professor Cem Göknar of Istanbul Technical University, who offered very detailed and valuable comments on "Design for Testability," and Professor Uğur Çilingiroğlu of the same university, who offered many excellent suggestions for improving the manuscript, especially the chapter on semiconductor memories.

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Several individuals have contributed their time and efforts to the third edition of our textbook. The authors would like to acknowledge the invaluable contribution of Dr. Seung-Moon Yoo who was instrumental in the extensive revision of the Memory chapter (Chapter 10). His technical insight, his meticulous attention to detail, and his very productive work are truly appreciated. The first author acknowledges the University of California at Santa Cruz for valuable support in his new position as Dean of the School of Engineering, and for enabling him to concentrate on the revision of the manuscript. The appointment of the second author as Full Professor at the Swiss Federal Institute of Technology in Lausanne, Switzerland, has also provided an excellent environment for the completion of the project. The second author gratefully acknowledges Mme. Séverine Eggli for her valuable assistance in revisions, and for typing sections of the text. The authors thank Mr. Tom Vernier and the technical staff of the MOSIS organization for generously providing the SPICE BSIM parameters for the TSMC 0.18 $\mu$m process that were extracted by MOSIS. The authors also acknowledge Dr. Michael W. Davidson of the Florida State University National High Magnetic Field Laboratory, for providing the DEC Alpha chip microphotographs that appear on the cover.

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