

国外电子与通信教材系列

英文版

Mc
Graw
Hill
Education

芯片制造

——半导体工艺制程实用教程

(第六版)

Microchip Fabrication
A Practical Guide to Semiconductor Processing
Sixth Edition

[美] Peter Van Zant 著



电子工业出版社
PUBLISHING HOUSE OF ELECTRONICS INDUSTRY
<http://www.phei.com.cn>

国外电子与通信教材系列

芯片制造

——半导体工艺制程实用教程

(第六版) (英文版)

Microchip Fabrication
A Practical Guide to Semiconductor Processing
Sixth Edition

[美] Peter Van Zant 著

电子工业出版社

Publishing House of Electronics Industry

北京·BEIJING

内 容 简 介

本书是一本介绍半导体集成电路和器件制造技术的专业书籍，在半导体领域享有很高的声誉。本书的范围包括半导体工艺的每个阶段：从原材料的制备到封装、测试和成品运输，以及传统的和现代的工艺。全书提供了详细的插图和实例，每章包含回顾总结和习题，并辅以丰富的术语表。第六版修订了微芯片制造领域的新进展，讨论了用于图形化、掺杂和薄膜步骤的先进工艺和尖端技术，使隐含在复杂的现代半导体制造材料和工艺中的物理、化学和电子的基础知识更易理解。本书的主要特点是避开了复杂的数学问题介绍工艺技术内容；加入了半导体业界的新成果，可以使读者了解工艺技术发展的趋势。

本书可作为高等院校电子科学与技术专业和职业技术培训的教材，也可作为半导体专业人员的参考书。

Peter Van Zant.

Microchip Fabrication: A Practical Guide to Semiconductor Processing, Sixth Edition.

ISBN: 9780071821018. Copyright ©2014 by McGraw-Hill Education.

All Rights reserved. No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including without limitation photocopying, recording, taping, or any database, information or retrieval system, without the prior written permission of the publisher.

This authorized English reprint edition is jointly published by McGraw-Hill Education and Publishing House of Electronics Industry. This edition is authorized for sale in China Mainland.

Copyright © 2014 by McGraw-Hill Education and Publishing House of Electronics Industry.

版权所有。未经出版人事先书面许可，对本出版物的任何部分不得以任何方式或途径复制或传播，包括但不限于复印、录制、录音，或通过任何数据库、信息或可检索的系统。

本授权英文影印版由麦格劳-希尔（亚洲）教育出版公司和电子工业出版社合作出版。此版本经授权仅限在中国大陆销售。

版权©2014 由麦格劳-希尔（亚洲）教育出版公司与电子工业出版社所有。

本书封面贴有McGraw-Hill Education 公司防伪标签，无标签者不得销售。

版权贸易合同登记号 图字：01-2014-6156

图书在版编目（CIP）数据

芯片制造：半导体工艺制程实用教程：第6版 = Microchip Fabrication: A Practical Guide to Semiconductor Processing, Sixth Edition: 英文 / (美) 赞特 (Zant, P. V.) 著. — 北京：电子工业出版社，2014.11

国外电子与通信教材系列

ISBN 978-7-121-24378-3

I. ①芯… II. ①赞… III. ①芯片—半导体工艺—高等学校—教材—英文 IV. ①TN430.5

中国版本图书馆CIP数据核字（2014）第216742号

策划编辑：杨 博

责任编辑：杨 博

印 刷：三河市鑫金马印装有限公司

装 订：三河市鑫金马印装有限公司

出版发行：电子工业出版社

北京市海淀区万寿路173信箱 邮编 100036

开 本：787×980 1/16 印张：35.25 字数：1026千字

版 次：2014年11月第1版（原著第6版）

印 次：2014年11月第1次印刷

定 价：79.00元

凡所购买电子工业出版社图书有缺损问题，请向购买书店调换。若书店售缺，请与本社发行部联系，联系及邮购电话：（010）88254888。

质量投诉请发邮件至zlts@phei.com.cn，盗版侵权举报请发邮件至dbqq@phei.com.cn。

服务热线：（010）88258888。

Preface

From the Preface of the *First Edition*: “As the semiconductor industry becomes more important in the economy, more people will be involved in the industry. It is my intention that *Microchip Fabrication* will serve their needs.”

Indeed the semiconductor industry has grown into a major international industrial segment. The semiconductor materials and equipment industries have also grown into major industrial sectors. This edition has followed the goal of the *First Edition* to serve the training needs of wafer-fabrication workers, whether they be production workers, technicians, professionals in the materials and equipment sectors, or engineers.

The *Sixth Edition* retains the physics, chemistry, and electronic fundamentals underlying the sophisticated manufacturing materials and processes of the modern semiconductor industry. It goes on to profile the state-of-the-art processes that have grown from the simple laboratory production lines of the 1960s. Not every individual process flow can be detailed in an introductory text. But current technologies used in the patterning, doping, and layering steps are explained. The intention of this book is that the reader will gain enough general knowledge to be able to keep abreast of new processes and equipment.

I am indebted to the valuable input from Anne Miller and Dr. Michael Hynes at Semiconductor Services, Bill Moffat the founder and President of Yield Engineering Systems, and Don Keenan, process engineer extraordinaire.

Kudos to Senior Editor Michael McCabe and his staff at McGraw-Hill for their support and guidance. And a thanks to Sheena Uprety, Associate Project Manager at Cengage Publisher Services, and the copyeditor, Ragini Pandey, for turning my manuscript into a ready-for-production text.

And, of course, a shout out to my ever supportive and patient wife, Mary DeWitt. She edited the first edition, has given me encouragement during the writing of every edition, and has lent her eagle eye to this latest edition.

Note to Instructors: If you are an instructor using this book as a textbook, then there is an Instructor’s Manual available at www.mhprofessional.com/mf6e.

Peter Van Zant

Contents

1	The Semiconductor Industry	1
	Introduction	1
	Birth of an Industry	1
	The Solid-State Era	3
	Integrated Circuits (ICs)	4
	Process and Product Trends	5
	Moore's Law	6
	Decreasing Feature Size	6
	Increasing Chip and Wafer Size	8
	Reduction in Defect Density	9
	Increase in Interconnection Levels	10
	The Semiconductor Industry Association Roadmap	10
	Chip Cost	11
	Industry Organization	11
	Stages of Manufacturing	12
	Six Decades of Advances in Microchip Fabrication Processes	14
	The Nano Era	16
	Review Topics	17
	References	17
2	Properties of Semiconductor Materials and Chemicals	19
	Introduction	19
	Atomic Structure	19
	The Bohr Atom	19
	The Periodic Table of the Elements	20
	Electrical Conduction	23
	Conductors	23
	Dielectrics and Capacitors	23
	Resistors	24
	Intrinsic Semiconductors	24
	Doped Semiconductors	25
	Electron and Hole Conduction	26
	Carrier Mobility	28
	Semiconductor Production Materials	29
	Germanium and Silicon	29
	Semiconducting Compounds	29
	Silicon Germanium	31
	Engineered Substrates	31
	Ferroelectric Materials	31
	Diamond Semiconductors	32
	Process Chemicals	32

Molecules, Compounds, and Mixtures	32
Ions	33
States of Matter	34
Solids, Liquids, and Gases	34
Plasma State	34
Properties of Matter	34
Temperature	34
Density, Specific Gravity, and Vapor Density	35
Pressure and Vacuum	36
Acids, Alkalis, and Solvents	37
Acids and Alkalis	37
Solvents	38
Chemical Purity and Cleanliness	38
Safety Issues	38
The Material Safety Data Sheet	39
Review Topics	39
References	39
3 Crystal Growth and Silicon Wafer Preparation	41
Introduction	41
Semiconductor Silicon Preparation	41
Silicon Wafer Preparation Stages	42
Crystalline Materials	42
Unit Cells	43
Poly and Single Crystals	43
Crystal Orientation	44
Crystal Growth	45
Czochralski Method	45
Liquid-Encapsulated Czochralski	47
Float Zone	47
Crystal and Wafer Quality	49
Point Defects	49
Dislocations	50
Growth Defects	50
Wafer Preparation	51
End Cropping	51
Diameter Grinding	51
Crystal Orientation, Conductivity, and Resistivity Check	51
Grinding Orientation Indicators	52
Wafer Slicing	53
Wafer Marking	54
Rough Polish	54
Chemical Mechanical Polishing	55
Backside Processing	55
Double-Sided Polishing	56
Edge Grinding and Polishing	56
Wafer Evaluation	56
Oxidation	57

Packaging	57
Wafer Types and Uses	57
Reclaim Wafers	57
Engineered Wafers (Substrates)	57
Review Topics	58
References	58
4 Overview of Wafer Fabrication and Packaging	59
Introduction	59
Goal of Wafer Fabrication	59
Wafer Terminology	59
Chip Terminology	61
Basic Wafer-Fabrication Operations	63
Layering	63
Patterning	64
Circuit Design	66
Reticle and Masks	68
Doping	69
Heat Treatments	69
Example Fabrication Process	72
Wafer Sort	74
Packaging	75
Summary	75
Review Topics	76
References	76
5 Contamination Control	77
Introduction	77
The Problem	77
Contamination-Caused Problems	80
Contamination Sources	81
General Sources	81
Air	81
Clean Air Strategies	82
Cleanroom Workstation Strategy	83
Tunnel or Bay Concept	85
Micro- and Mini-Environments	86
Temperature, Humidity, and Smog	87
Cleanroom Construction	88
Construction Materials	88
Cleanroom Elements	89
Personnel-Generated Contamination	93
Process Water	94
Process Chemicals	96
Equipment	99
Cleanroom Materials and Supplies	99
Cleanroom Maintenance	100
Wafer-Surface Cleaning	100

Particulate Removal	102
Wafer Scrubbers	102
High-Pressure Water Cleaning	103
Organic Residues	103
Inorganic Residues	103
Chemical-Cleaning Solutions	104
General Chemical Cleaning	104
Oxide Layer Removal	105
Room Temperature and Ozonated Chemistries	106
Water Rinsing	108
Drying Techniques	110
Contamination Detection	112
Review Topics	112
References	113
6 Productivity and Process Yields	115
Overview	115
Yield Measurement Points	115
Accumulative Wafer-Fabrication Yield	116
Wafer-Fabrication Yield Limiters	117
Number of Process Steps	118
Wafer Breakage and Warping	118
Process Variation	119
Mask Defects	120
Wafer-Sort Yield Factors	120
Wafer Diameter and Edge Die	121
Wafer Diameter and Die Size	122
Wafer Diameter and Crystal Defects	122
Wafer Diameter and Process Variations	123
Die Area and Defect Density	124
Circuit Density and Defect Density	125
Number of Process Steps	125
Feature Size and Defect Size	125
Process Cycle Time	125
Wafer-Sort Yield Formulas	125
Assembly and Final Test Yields	128
Overall Process Yields	128
Review Topics	129
References	130
7 Oxidation	131
Introduction	131
Silicon Dioxide Layer Uses	131
Surface Passivation	131
Doping Barrier	132
Surface Dielectric	132
Device Dielectric (MOS Gates)	133
Device Oxide Thicknesses	134

Thermal Oxidation Mechanisms	134
Influences on the Oxidation Rate	137
Thermal Oxidation Methods	140
Horizontal Tube Furnaces	140
Temperature Control System	141
Source Cabinet	143
Vertical Tube Furnaces	143
Rapid Thermal Processing	146
High-Pressure Oxidation	149
Oxidant Sources	151
Oxidation Processes	154
Preoxidation Wafer Cleaning	154
Postoxidation Evaluation	155
Surface Inspection	156
Oxide Thickness	156
Oxide and Furnace Cleanliness	156
Thermal Nitridation	156
Review Topics	157
References	157
8 The Ten-Step Patterning Process—Surface Preparation to Exposure	161
Introduction	161
Overview of the Photomasking Process	162
Ten-Step Process	165
Basic Photoresist Chemistry	167
Photoresist	167
Photoresist Performance Factors	169
Resolution Capability	169
Adhesion Capability	170
Process Latitude	171
Pinholes	172
Particle and Contamination Levels	173
Step Coverage	173
Thermal Flow	173
Comparison of Positive and Negative Resists	173
Physical Properties of Photoresists	175
Solids Content	175
Viscosity	175
Surface Tension	176
Index of Refraction	176
Storage and Control of Photoresists	176
Light and Heat Sensitivity	176
Viscosity Sensitivity	177
Shelf Life	177
Cleanliness	177
Photomasking Processes—Surface Preparation to Exposure	178
Surface Preparation	178
Particle Removal	178

Dehydration Baking	178
Wafer Priming	179
Spin Priming	180
Vapor Priming	180
Photoresist Application (Spinning)	181
The Static Dispense Spin Process	181
Dynamic Dispense	183
Moving-Arm Dispensing	183
Manual Spinners	183
Automatic Spinners	184
Edge Bead Removal	185
Backside Coating	185
Soft Bake	185
Convection Ovens	186
Manual Hot Plates	187
In-Line, Single-Wafer Hot Plates	187
Moving-Belt Hot Plates	187
Moving-Belt Infrared Ovens	188
Microwave Baking	188
Vacuum Baking	188
Alignment and Exposure	189
Alignment and Exposure Systems	189
Exposure Sources	191
Alignment Criteria	191
Aligner Types	193
Postexposure Bake	196
Advanced Lithography	198
Review Topics	198
References	198
9 The Ten-Step Patterning Process—Developing to Final Inspection	201
Introduction	201
Development	201
Positive Resist Development	201
Negative Resist Development	203
Wet Development Processes	203
Dry (or Plasma) Development	206
Hard Bake	207
Hard-Bake Methods	207
Hard-Bake Process	207
Develop Inspect	208
Develop Inspect Reject Categories	209
Develop Inspect Methods	209
Causes for Rejecting at the Develop Inspection Stage	211
Etch	212
Wet Etching	212
Etch Goals and Issues	212
Incomplete Etch	212

Overetch and Undercutting	213
Selectivity	214
Wet-Spray Etching	214
Silicon Wet Etching	214
Silicon Dioxide Wet Etching	215
Aluminum-Film Wet Etching	216
Deposited-Oxide Wet Etching	216
Silicon Nitride Wet Etching	216
Vapor Etching	217
Dry Etch	217
Plasma Etching	218
Etch Rate	220
Radiation Damage	220
Selectivity	220
Ion-Beam Etching	222
Reactive Ion Etching	222
Resist Effects in Dry Etching	223
Resist Stripping	223
Wet Chemical Stripping of Nonmetallized Surfaces	224
Wet Chemical Stripping of Metallized Surfaces	225
Dry Stripping	225
Post-Ion Implant and Plasma Etch Stripping	226
New Stripping Challenges	226
Final Inspection	227
Mask Making	227
Summary	229
Review Topics	229
References	230
10 Next Generation Lithography	233
Introduction	233
Challenges of Next Generation Lithography	233
High-Pressure Mercury Lamp Sources	235
Excimer Lasers	236
Extreme Ultraviolet	236
X-Rays	237
Electron Beam or Direct Writing	238
Numerical Aperture of a Lens	240
Other Exposure Issues	241
Variable Numerical Aperture Lenses	242
Immersion Exposure System	242
Amplified Resist	242
Contrast Effects	243
Other Resolution Challenges and Solutions	244
Off-Axis Illumination	245
Lens Issues and Reflection Systems	245
Phase-Shift Masks	245
Optical Proximity Corrected or Optical Process Correction	245

Annular-Ring Illumination	246
Pellicles	247
Surface Problems	248
Resist Light Scattering	248
Subsurface Reflectivity	248
Antireflective Coatings	249
Standing Waves	249
Planarization	251
Photoresist Process Advances	252
Multilayer Resist or Surface Imaging	252
Silylation or DESIRE Process	254
Polyimide Planarization Layers	255
Etchback Planarization	256
Dual-Damascene Process	256
Chemical Mechanical Polishing	256
Slurry	259
Polishing Rates	259
Planarity	260
Post-CMP Clean	261
CMP Tools	261
CMP Summary	262
Reflow	262
Image Reversal	262
Contrast Enhancement Layers	262
Dyed Resists	264
Improving Etch Definition	264
Lift-Off Process	264
Self-Aligned Structures	264
Etch Profile Control	266
Review Topics	266
References	266
11 Doping	269
Introduction	269
The Diffusion Concept	269
Formation of a Doped Region and Junction	271
The N-P Junction	272
Doping Process Goals	273
Graphical Representation of Junctions	273
Concentration versus Depth Graphs	273
Lateral Diffusion	273
Same-Type Doping	275
Diffusion Process Steps	275
Deposition	275
Dopant Sources	278
Drive-In Oxidation	280
Oxidation Effects	281
Introduction to Ion Implantation	281

Concept of Ion Implantation	283
Ion-Implantation System	284
Implant Species Sources	284
Ionization Chamber	284
Mass Analyzing or Ion Selection	284
Acceleration Tube	286
Wafer Charging	286
Beam Focus	287
Neutral Beam Trap	287
Beam Scanning	287
End Station and Target Chamber	289
Ion-Implant Masks	290
Dopant Concentration in Implanted Regions	291
Crystal Damage	292
Annealing and Dopant Activation	292
Channeling	293
Evaluation of Implanted Layers	294
Uses of Ion Implantation	295
The Future of Doping	297
Review Topics	297
References	298
12 Layer Deposition	299
Introduction	299
Film Parameters	301
Chemical Vapor Deposition Basics	302
Basic CVD System Components	303
CVD Process Steps	305
CVD System Types	305
Atmospheric-Pressure CVD Systems	306
Horizontal-Tube Induction-Heated APCVD	306
Barrel Radiant-Induction-Heated APCVD	307
Pancake Induction-Heated APCVD	307
Continuous Conduction-Heated APCVD	308
Horizontal Conduction-Heated APCVD	309
Low-Pressure Chemical Vapor Deposition	309
Horizontal Conduction-Convection-Heated LPCVD	309
Ultra-High Vacuum CVD	310
Plasma-Enhanced CVD (PECVD)	310
High-Density Plasma CVD	312
Atomic Layer Deposition	313
Vapor-Phase Epitaxy	315
Molecular Beam Epitaxy	315
Metalorganic CVD	317
Deposited Films	318
Deposited Semiconductors	318
Epitaxial Silicon	318
Polysilicon and Amorphous Silicon Deposition	324

SOS and SOI	325
Gallium Arsenide on Silicon	326
Insulators and Dielectrics	326
Silicon Dioxide	326
Doped Silicon Dioxide	327
Silicon Nitride	328
High-k and Low-k Dielectrics	329
Conductors	329
Review Topics	329
References	330
13 Metallization	333
Introduction	333
Deposition Methods	333
Single-Layer Metal Systems	334
Multilevel Metal Schemes	335
Conductors Materials	336
Aluminum	336
Aluminum-Silicon Alloys	336
Aluminum-Copper Alloy	337
Barrier Metals	338
Refractory Metals and Refractory Metal Silicides	338
Plugs	339
Sputter Deposition	340
Copper Dual-Damascene Process	345
Low-k Dielectric Materials	345
The Dual-Damascene Copper Process	346
Barrier or Liner Deposition	348
Seed Deposition	348
Electrochemical Plating	348
Chemical-Mechanical Processing	349
CVD Metal Deposition	349
Doped Polysilicon	349
CVD Refractory Deposition	350
Metal-Film Uses	351
MOS Gate and Capacitor Electrodes	351
Backside Metallization	351
Vacuum Systems	351
Dry Mechanical Pumps	352
Turbomolecular Hi-Vac Pumps	352
Review Topics	353
References	353
14 Process and Device Evaluation	355
Introduction	355
Wafer Electrical Measurements	356
Resistance and Resistivity	356
Resistivity Measurements	356

Four-Point Probe	356
Process and Device Evaluation	358
Sheet Resistance	358
Four-Point Probe Thickness Measurement	358
Concentration or Depth Profile	359
Secondary Ion Mass Spectrometry	359
Optically Modulated Optical Reflection (Thermawave)	360
Physical Measurement Methods	360
Layer Thickness Measurements	360
Color	360
Spectrophotometers or Reflectometry	361
Ellipsometers	363
Stylus (Surface Profilometers)	363
Photoacoustic	365
Four-Point Probe	365
Ultra-Thin MOSFET Gate Thickness	365
Gate Oxide Integrity Electrical Measurement	365
Junction Depth	365
Groove and Stain	365
Scanning Electron Microscope Thickness Measurement	367
Spreading Resistance Probe	367
Secondary Ion Mass Spectrometry	367
Scanning Capacitance Microscopy	368
Carrier Illumination Junction Depth	368
Critical Dimensions and Line-Width Measurements	369
Optical Image-Shearing Dimension Measurement	369
Shape Metrology and Optical Critical Dimension	370
Contamination and Defect Detection	370
1× Visual Surface Inspection Techniques	370
1× Collimated Light	370
1× Ultraviolet	372
Microscope Techniques	372
Automated In-Line Defect Inspection Systems	376
General Surface Characterization	378
Atomic Force Microscopy	378
Scattrometry	380
Contamination Identification	380
Auger Electron Spectroscopy	380
Electron Spectroscopy for Chemical Analysis	381
Time of Flight Secondary Ion Mass Spectrometry	381
Evaluation of Stack Thickness and Composition	382
Device Electrical Measurements	382
Equipment	383
Resistors	383
Diodes	384
Bipolar Transistors	386
MOS Transistors	387

Capacitance-Voltage Profiling	387
Device Failure Analysis—Emission Microscopy	390
Review Topics	390
References	391
15 The Business of Wafer Fabrication	393
Introduction	393
Moore's Law and the New Wafer-Fabrication Business	393
Wafer-Fabrication Costs	394
Overhead	395
Materials	395
Equipment	396
Labor	397
Production Cost Factors	397
Yield	398
Yield Improvements	398
Yield and Productivity	399
Increasing Wafer Diameters	400
Book-to-Bill Ratio	401
Cost of Ownership	402
Automation	402
Process Automation	402
Wafer-Loading Automation	403
Clustering	403
Wafer-Delivery Automation	404
Closed-Loop Control-System Automation	405
Factory-Level Automation	405
Equipment Standards	407
Fab Floor Layout	407
Batch versus Single-Wafer Processing	407
Green Fabs	408
Statistical Process Control	409
Inventory Control	412
Just-in-Time Inventory Control	413
Quality Control and Certification—ISO 9000	414
Line Organization	414
Review Topics	415
References	416
16 Introduction to Devices and Integrated Circuit Formation	417
Introduction	417
Semiconductor-Device Formation	417
Resistors	418
Capacitors	420
Diodes	422
Transistors	424
Field-Effect Transistors	427
Alternatives to MOSFET Scaling Challenges	434