Edited by Xicheng Jiang

Digitally-Assisted Analog and Analog-Assisted Digital IC Design

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Digitally-Assisted Analog and Analog-Assisted Digital IC Design

Achieve enhanced performance with this guide to cutting-edge techniques for digitally-assisted analog and analog-assisted digital integrated circuit design.

- Discover how architecture and circuit innovations can deliver improved performance in terms of speed, density, power, and cost.
- Learn about practical design considerations for high-performance scaled CMOS processes, FinFET devices and architectures, and the implications of FD SOI technology.
- Get up to speed with established circuit techniques that take advantage of scaled CMOS process technology in analog, digital, RF, and SoC designs, including digitally-assisted techniques for data converters, DSP-enabled frequency synthesizers, and digital controllers for switching power converters.

With detailed descriptions, explanations, and practical advice from leading industry experts, this is an ideal resource for practicing engineers, researchers, and graduate students working in circuit design.

Xicheng Jiang is a Distinguished Engineer, and Director of Electrical Design Engineering, at Broadcom Corporation. He is a former Associate Editor of *IEEE Transactions on Circuits and Systems II*, holds more the 30 issued and pending US patents, and is a Fellow of the IEEE.

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To Liu, Lan, and Xiao

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Preface

Digitally-assisted analog and analog-assisted digital techniques are increasingly needed in future circuit and system designs, as FinFET and FDSOI replace planar CMOS technology at advanced process nodes of 20 nm and beyond. The intrinsic features of these new devices are lowering the barrier between the analog and the digital worlds, allowing unprecedented performance to be achieved by assisting digital circuits with analog techniques or analog circuits with digital techniques.

As CMOS technologies scale to smaller nodes, digital designs enjoy obvious benefits in terms of higher speed and lower power consumption. However, scaling doesn't happen so readily or cleanly with analog designs. Analog circuits frequently make use of "digital assistance", which allows simplification of the critical analog circuits that don't scale easily. Digitally-assisted analog techniques, such as calibration, allow for considerable relaxation of the analog performance, which can be used for minimizing both area and power consumption. Another trend is the transition of traditional analog functions to the digital domain. Compared to their analog mixed-signal counterparts, all-digital implementations are scalable, insensitive to noise, and robust against process variations. On the other hand, driven by the worldwide demand for low-power application processors, dynamic voltage/frequency scaling (DVFS) and adaptive voltage scaling (AVS) are typically used to reduce energy consumption in mobile systems. DVFS and AVS are enabled for optimal power management by analog techniques that monitor the on-die process, voltage and temperature variations.

The objective of this book is to discuss practical design considerations in high-performance scaled CMOS processes, established circuit techniques that take advantage of scaled CMOS process technology in analog, digital, RF, and system-on-chip (SoC) designs, and the outlook for the future in the context of challenges and solutions.

The book consists of nine chapters. Chapter 1 overviews the history of transistor scaling in recent 20 years. Several traditional scaling implications like short-channel effects, followed by the ever-increasing impacts of process variation and parasitic elements are revisited. This chapter also introduces several design issues specific to the recent nano-scale transistors, which include well proximity, shallow trench isolation (STI) stress-induced performance variation, aging effects, and so on.

Chapter 2 presents FinFETs from devices to architectures. It surveys different types of FinFETs, various FinFET asymmetries and their impact, and novel logic-level and architecture-level trade-offs. It also reviews analysis and optimization tools that are available for characterizing FinFET devices, circuits, and architectures.

Chapter 3 starts with an introduction of fully depleted silicon on insulator (FDSOI) devices. The chapter focuses on the advantages and the challenges in analog and digital design of FDSOI. Implementation of FDSOI technology in high-volume manufacturing (HVM) is then discussed along with the recent progress in improving FDSOI device performance and design for mobile applications. The competition and augmentation of FDSOI along with device architectures such as FinFETs are discussed. Finally, the technology roadmap for extending FDSOI beyond 10 nm in conjunction with future material and device innovations is proposed.

Chapter 4 takes a detailed look at the recent trend of DSP-enabled frequency synthesizers and its challenges. The basic principles and overheads of such phase lock loop (PLL) architectures are identified. Moreover, various emerging circuit and algorithmic techniques that leverage this digital intensive architecture are described.

Chapter 5 describes several digital-processing techniques to enhance the raw analog performance of pipeline and SAR ADCs. These techniques address most of the analog circuit metrics such as linearity, timing accuracy, component matching and when non-ideal their impact on the overall converter performance. To some extent, these works demonstrate that digitally-assisted techniques can be either more power-efficient or simpler to implement (or both) than their conventional counterparts.

Chapter 6 discusses the challenges of process variation that confront mm-wave transceivers in terms of attaining suitable yield and RF performance for commercialization, and looks at self-healing techniques that can be incorporated into the design of RF front ends to mitigate these effects. Specifically discussed will be self-healing techniques for optimizing transmitter output power, self-healing techniques for optimizing linearity and distortion, and finally self-healing techniques for synthesizer operation.

Chapter 7 gives an overview of some of the main digital design challenges for mobile SoCs in advanced process nodes, including low-power operation, process variability, power-supply noise, heat management, and aging. It describes how critical-path monitors and process sensors can be used to lower the supply voltage in the presence of inter-die and intra-die process variations. It presents the voltage regulation techniques that are commonly used for mobile SoCs or that will be particularly suitable for on-chip integration in the future. Obviously, voltage regulation can reduce, but not completely eliminate, the power-supply noise. Because of this, the techniques used to manage the residual noise, including droop detection and adaptive clocking, or to avoid generating too much noise when turning power switches on or off are discussed in detail. Finally, the chapter discusses mixed-signal techniques to design temperature and aging sensors.

Chapter 8 presents digitally-assisted RF techniques, and categorizes architectures and algorithms in use. The relationship between RF systems and analog circuit performance metrics is explored carefully. This step is essential to properly identify the most critical analog impairments and to properly guide design trade-offs between potential mitigation strategies. Hopefully, the reader will find value in this background system-level material before a discussion of detailed circuit design.

Chapter 9 starts with the basic operations of a switching power converter, the converter systems' parameters, modes, and control methodologies. The three main

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functional blocks of a digital controller for a switching power converter, i.e., ADC, digital compensation, and digital pulse-width modulator, are discussed in detail. The rest of the sections in this chapter go through different existing implementations of these three functional blocks. A literature review of existing digital controllers for buck converter systems is also given. This helps the reader to weigh up the pros and cons of the existing approaches and how the digital controllers are actually designed.

I am most grateful for these vital contributions. The short timescale for producing this book made considerable demands on the authors and many of them put in a tremendous effort in the final rush to get material ready. Their professionalism and dedication will be long remembered.

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Xicheng Jiang
Los Angeles, December 2014

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