Physical Design for 3D Integrated Circuits

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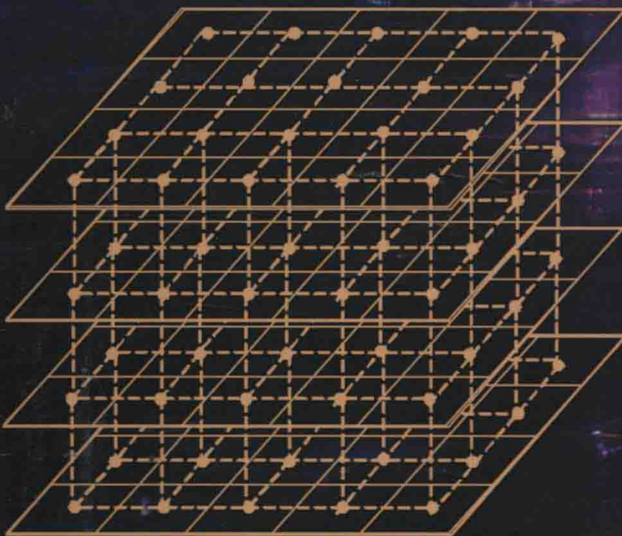

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Preface

Three-dimensional (3D) stacking and 2.5D interposer side-by-side integration are very attractive contenders as we head toward an incommensurate return of interconnects and packaging technology. As demand for on-chip functionalities and requirements for low power operation continue to increase as a result of the emergence of mobile, wearable, and Internet of Things products, 3D/2.5D integration has been identified as inevitable in moving forward. The advent of 3D/2.5D integration is a direct result of active research in academia, research laboratories, and industry over the past decade. Today, 3D/2.5D integration takes many forms, depending on the applications. At the time of this writing, there are already commercial products driven by the needs for form factor and density.

As a direct result of many years of active research, there is substantial documentation on 3D/2.5D technology. A book dedicated to the physical design for 3D integrated circuits (ICs), however, is lacking. The idea for a book on physical design for 3D ICs dates back more than a year ago. While the initial idea was to write a book, we soon realized that such an endeavor would be extremely challenging given the various expertises in this field. We revisited the plan and decided to edit a book instead, with contributions from experts in academia, research laboratories, and industry. After careful planning, we identified and invited contributions from an impressive lineup of highly qualified researchers. The task took a full year from planning, writing, editing, and printing.

This book aims to unveil how to effectively and optimally design such 3D circuits. It also presents the design tools for 3D circuits, while exploiting the benefits of 3D technology. Initially, an overview of physical design challenges with respect to conventional 2D circuits is provided, and then each chapter is dedicated to provide an in-depth look into each physical design topic. *Physical Design for 3D Integrated Circuits* is the first book to analyze the design tools for 3D ICs covering all design aspects and explaining the challenges and solutions unique for 3D circuits. This book is particularly beneficial to researchers and engineers who are already working or are beginning to work on 3D technology.

This book would not have been possible without a team of highly qualified and dedicated people. We are particularly grateful to Kris Iniewski for initiating this undertaking and for his encouragement. Nora Konopka and Jessica Vakili worked alongside us and provided us with the necessary editorial support. Aida Todri-Sanial is grateful for the continued support for her work on 3D integration from the French National Research Agency (ANR) and strong collaborations with CEA-LETI, France. Chuan Seng Tan is grateful for the continued support for his work on 3D integration in Singapore from the Ministry of Defense (MINDEF), the Ministry of Education (MOE), the Agency for Science, Technology and Research (A*STAR), and the National Research Foundation (NRF). This book would not have been possible without this extended research support. Last but not least, we are extremely thankful to the authors who accepted our invitation and contributed chapters to this book.

We hope that the readers will find this book useful in their pursuit of 3D/2.5D technology. Please do not hesitate to contact us if you have any comments or suggestions.

Aida Todri-Sanial dedicates this book to her family. Chuan Seng Tan dedicates this book to his wife and sons.

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Aida Todri-Sanial
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Editors

Aida Todri-Sanial earned a PhD in electrical and computer engineering at the University of California, Santa Barbara, in 2009. She is currently a research scientist (Chargée de Recherché) at CNRS (French National Center for Scientific Research) and a member of the Microelectronics Department at Laboratoire d'Informatique, de Robotique, de Microelectronique de Montpellier (LIRMM), where she is the group leader of Integration and Design of Energy-Aware Circuits and Systems. Prior to joining CNRS, she was an R&D engineer at Fermilab. She also has several visiting research positions at Cadence Design Systems, Mentor Graphics, IBM TJ Watson Research Center, and STMicroelectronics. Dr. Todri-Sanial has received several awards, including the CNRS Scientific Excellence Award (PES) 2012, the John Bardeen Fellow in Engineering at Fermilab 2009, and Best Teaching Assistant at the University of California, Santa Barbara. She has published more than 100 papers in very-large-scale integration design area. She serves on the technical program committees for the IEEE (Emerging Technologies Track), IEEE ISQED, IEEE NEWCAS, IEEE ISVLSI, IEEE GLSVLSI, and as an expert reviewer for IEEE/ACM DAC. She also serves as a technical reviewer for *IEEE Transactions on VLSI*, Computers, CAD, CAS-I, CAS-II, TNS, and IET. She is an associate editor for the *IEEE Transactions on Very Large Scale Integration* journal. She is also engaged with European agencies, such as the European Platform of Women Scientist (EPWS) and the European Association for Women in Science, Engineering and Technology (WiTEC). She is a member of the IEEE and the ACM.

Chuan Seng Tan earned a BE in electrical engineering at the University of Malaya, Malaysia, in 1999. Subsequently, he earned an ME in advanced materials at the National University of Singapore under the Singapore-MIT Alliance (SMA) program in 2001. He then joined the Institute of Microelectronics, Singapore, as a research engineer where he worked on process integration of strained-Si/relaxed-SiGe heterostructure devices. In the fall of 2001 he began his doctoral work at the Massachusetts Institute of Technology, Cambridge, Massachusetts, and earned a PhD in electrical engineering in 2006. He was the recipient of the Applied Materials Graduate Fellowship for 2003–2005. In 2003, he interned at Intel Corporation, Oregon. He joined Nanyang Technological University, Singapore, in 2006 as a Lee Kuan Yew postdoctoral fellow, and since July 2008 he has held the inaugural Nanyang assistant professorship. In February 2014 he was promoted to associate professor (with tenure). His research interests are semiconductor process technology and device physics. He is working on the process technology of three-dimensional integrated circuits (3D ICs). He has edited two books, *Wafer Level 3-D ICs Process Technology* and *3D Integration of VLSI Systems*. He has numerous publications on 3D technology. He is a committee member of the International Conference on Wafer Bonding, IEEE-3DIC, IEEE-EPTC, IEEE-ECTC, ECS-Wafer Bonding, SSDM, and ISTDM. He is an associate editor for Elsevier's *Microelectronics Journal (MEJ)*. He is a member of the IEEE.

Krzysztof Iniewski is managing R&D at Redlen Technologies Inc., a start-up company in Vancouver, Canada. Redlen's revolutionary production process for advanced semiconductor materials enables a new generation of more accurate, all-digital, radiation-based imaging solutions. He is also a president of CMOS Emerging Technologies Research Inc. (www.cmosetr.com), an organization of high-tech events covering communications, microsystems, optoelectronics, and sensors. He also has held numerous faculty and management positions at the University of Toronto, the University of Alberta, Simon Frazer University, and PMC-Sierra Inc. He has published more than 100 research papers in international journals and conferences. He holds 18 international patents

granted in the United States, Canada, France, Germany, and Japan. He is a frequent invited speaker and has consulted for multiple organizations internationally. He has written and edited several books for CRC Press, Cambridge University Press, IEEE Press, Wiley, McGraw-Hill, Artech House, and Springer. He seeks to contribute to healthy living and sustainability through innovative engineering solutions. He can be reached at kris.iniewski@gmail.com.

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