III-V Integrated Circuit Fabrication Technology

Shiban Tiku Dhrubes Biswas



III-V Integrated Circuit Fabrication Technology

Shiban Tiku Dhrubes Biswas

Published by

Pan Stanford Publishing Pte. Ltd. Penthouse Level, Suntec Tower 3 8 Temasek Boulevard Singapore 038988

Email: editorial@panstanford.com

Web: www.panstanford.com

British Library Cataloguing-in-Publication Data

A catalogue record for this book is available from the British Library.

III-V Integrated Circuit Fabrication Technology

Copyright © 2016 by Pan Stanford Publishing Pte. Ltd.

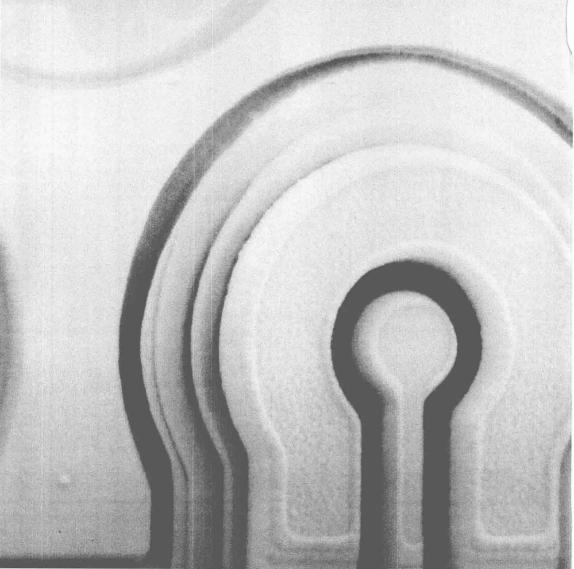
All rights reserved. This book, or parts thereof, may not be reproduced in any form or by any means, electronic or mechanical, including photocopying, recording or any information storage and retrieval system now known or to be invented, without written permission from the publisher.

For photocopying of material in this volume, please pay a copying fee through the Copyright Clearance Center, Inc., 222 Rosewood Drive, Danvers, MA 01923, USA. In this case permission to photocopy is not required from the publisher.

ISBN 978-981-4669-30-6 (Hardcover) ISBN 978-981-4669-31-3 (eBook)

Printed in the USA

III-V Integrated Circuit Fabrication Technology



Preface

In this Internet age, practicing engineers still need a book that they can keep on their desk. This book is aimed for them and also graduate students and engineers new to the field of III-V semiconductor integrated circuit (IC) processing. This book specifically addresses the needs of students who know semiconductor theory but lack detailed processing knowledge. The content is chosen on the basis of the needs of students as seen by a teacher and the needs of practicing engineers dealing with processing issues as seen by an experienced process engineer. GaAs processing has reached a mature stage, a long way from a few decades ago, when it was more of an art than a science. New semiconductor compounds are emerging that will dominate future materials and device research; however, the processing techniques used for GaAs will still remain relevant. This book covers all aspects of the current state of the art of III-V processing, with emphasis on heterojunction bipolar transistors (HBTs), the volume leader technology, having grown due to the explosive growth of wireless technology. The book's primary purpose is to discuss processing; only necessary equations are derived and device behavior is discussed for the purpose of understanding device figures of merit and electrical parameters that engineers need to understand and control. All aspects of processing of active and passive devices, from crystal growth to backside processing, including lithography, etching, and film deposition. are covered. New material systems based on GaN are playing a larger role on the development side; although the etching chemistries, deposition materials, and temperature regimes are different, similar principles apply. The most promising structures of these material systems and devices are covered in the book.

The book covers semiconductor material basics, physics of devices used in semiconductor IC processing, and all the processing technologies used in III–V semiconductor fabrication. In the discussion, differences with silicon IC processes are emphasized. Crystal growth and particularly epitaxy are discussed in depth because of the special role played by them and device structures

made possible by them. Photolithography, ion implantation, wet and plasma etching, and deposition of films are covered in detail. Thermal processes and diffusion are discussed to the level needed for III-V processing. Schottky and ohmic contact physics and processing are discussed from a practical point of view for controlling these in high-volume production. All the device technologies currently in use in the III-V semiconductor marketplace are discussed in depth, including recently introduced bipolar field-effect transistor (BiFET) and bipolar high-electron-mobility transistor (BiHEMT) technologies. Device types that are emerging and expected to be important in the near future, like metal-oxide-semiconductor field-effect transistors (MOSFETs), are also introduced. Passive devices and interconnects are covered, being integral to monolithic microwave integrated circuit (MMIC) fabrication. Also, backside processing, which is absolutely necessary for high efficiency, is described in detail and wafer-scale bumping is introduced, being critical to future higher-frequency needs. Characterization of films and semiconductor layers, as well as device parameter measurement, is covered in detail, Reliability issues relevant to III-V semiconductors are discussed. Finally, emerging GaN devices and microelectromechanical systems (MEMS) are briefly described.

Most published books on the market emphasize III-V device physics. No new processing book has been published in a decade. Published books are old and cover mostly FET processing. Ralph Williams's book, Modern GaAs Processing, is over 20 years old and does not cover processing technologies in detail. S. K. Ghandhi's book, VLSI Fabrication Principles: Silicon and Gallium Arsenide, covers processing techniques in detail but IC processing very briefly. This book is also old, published in the 1980s, Fazal Ali's book, HEMTs and HBTs: Devices, Fabrication and Circuits, covers fabrication very broadly and was also published in 1991, over 20 years ago. Baca and Ashby's book, Fabrication of GaAs Devices, has a narrow focus, specializing in cleaning and passivation; basic IC processing techniques are not covered. It was published in 2005, a decade old now.

This (present) book covers all aspects of processing, from crystal growth to backside processing. It covers the current volume production device types, HBTs, HEMTs, etc. The book is not restricted to GaAs; other emerging III-V materials are covered, too.

Epigrowth, device structure, and processing discussions are connected together through different chapters. Processing techniques relevant to III-V IC fabrication are described as they are used in III-V processing facilities in high-volume production. Process flows are illustrated by step-by-step block diagrams. Scanning electron microscopy (SEM) pictures of actual devices are included. where needed. This is one book to find any topic relevant to III-V processing. Practical process problems and ways to handle these are described

The current understanding of III-V processing has come a long way from the era when GaAs processing was based on practical knowledge and company trade secrets. This book attempts to connect practice on the fabrication floor to current scientific understanding.

> Shiban Tiku **Dhrubes Biswas**



Acknowledgments

The earlier books on GaAs and III–V semiconductor materials processing were written in an era when GaAs was considered the "technology of the future." This present work, although inspired by those, is aimed at fulfilling the needs of this era in which the technology is well established and perhaps becoming the "technology of the past," while paving the way for future technologies. Many minds and hands have contributed to this work. I am indebted to all my teachers over the years, who left an indelible mark on my life. I also thank the people of India for the almost free education I received.

This book would not have been possible without support from Skyworks Solutions' management, Ravi Ramanathan, Nercy Ebrahimi, and Andy Hunt, and IP council Donald Bollella, who weighed the benefits of contributing to the III–V industry worldwide over the risk of disclosing trade secrets. A lot of data came from my fellow engineers at Skyworks and the CS MANTECH community in general. Early feedback from Martin Brophy (Avago) and Peter Asbeck (UCSD) encouraged me. In particular, help from the following Skyworks colleagues is acknowledged: Heather Knoedler, Jens Riege, Dave Crawford, Ravi Ramanathan, Mike Sun, Jiro Yota, Pete Zampardi, Lance Rushing, Cristian Cismaru, Sam Mony, Lam Luu, and Manjeet Singh. Constant support from my wife, Sushma, and son, Vikram, helped me during difficult times. I am also thankful to Archana Ziradkar of Pan Stanford Publishing for systematic editorial help and to Barron Miller for drafting of many of the figures.

Shiban Tiku

Contents

refa	ice			xxiii	
	owledgi	ments		xxvii	
1.	Semico	nductor	Basics	1	
-	1.1	Introdu		1	
		1.1.1	GaAs Device Applications	2	
	1.2	GaAs Ci	rystal Structure	3	
	1.3	Bonding in III–V Semiconductors			
		1.3.1	Bonding in a Doped Crystal	9	
	1.4	Energy	Band Structure	9	
		1.4.1		13	
		1.4.2	Free Carrier Concentration and		
			Fermi Level	14	
		1.4.3	Energy Levels in Doped Semiconductors	17	
		1.4.4	Impurities in GaAs	20	
			1.4.4.1 Specific impurities	22	
	1.5	Crystal	Crystal Defects		
		1.5.1	Point Defects	24	
		1.5.2	Dislocations	25	
		1.5.3	Other Defects	27	
	1.6	Other P	ner Properties		
2.	GaAs D	evices		31	
	2.1 p-n and Metal-Semiconductor Junctions			31	
		2.1.1	p-n Junction Physics	31	
			2.1.1.1 <i>I–V</i> characteristics	33	
			2.1.1.2 Space charge and junction		
			capacitance	36	
		2.1.2	Metal-Semiconductor Junctions	38	
			2.1.2.1 Junction physics	39	
			2.1.2.2 Junction characteristics	43	
	2.2	MESFETs			
		2.2.1	Basic MESFETs	45	
		2.2.2	Low-Noise FETs	50	
		2.2.3	FETs for Digital Logic Circuits	51	

	2.3	HEMIS	and PHE	MTS	52
		2.3.1	Device	Operation	54
	2.4	Bipolar	Junction	Transistors	54
		2.4.1	Phenon	nenological Description of	
			the BJT		55
		2.4.2	Current	-Voltage Characteristics	
			of a BJT		60
	2.5	HBT Pr	inciples o	of Operation	61
		2.5.1	_	ansport Equations	62
		2.5.2		Gain and Injection Efficiency	63
		2.5.3		of Merit for HBTs	65
	2.6	PIN Die	_		66
	2.7	IMPAT'	Γ		68
		2.7.1	Read-Ty	pe IMPATT	69
	2.8	Gunn D	iodes	~	69
	2.9	MOSFE	T		70
		2.9.1	Metal-I	nsulator–Semiconductor	
			Devices		71
		2.9.2	I-V Cha	racteristics	73
	2.10 Remarks on Ap		ks on App	lications	76
•	21			tal Carrelland Commenced	
3.	B. Phase Diagrams and Crystal Growth of Compound Semiconductors			79	
					79 79
	3.1		Diagrams		79
		3.1.1	Introdu		
		3.1.2		liagram Types	80
				Isomorphous phase diagram	81
				Eutectic diagrams	81
		242		Peritectic diagrams	82
	0.0	3.1.3		ent Transformation	83
	3.2		Growth	W	84
		3.2.1		Materials and Compounding	0.5
			Method		85
		3.2.2	_	Crystal Growth	86
			3.2.2.1	Bridgman/gradient freeze	0.7
			0000	technique	87
			3.2.2.2	Liquid-encapsulated	
				Czochralski method	88
			3.2.2.3	Vertical boat and vertical	00
				gradient freeze methods	89

			3224	Vapor pressure-controlled	
			0.2.2.1	Czochralski method	91
		3.2.3	InP Crys	stal Growth	91
	3.3		-	stivity Control	92
	5,5	3.3.1		o-Type Crystals	94
		5.5.1	ii ana p	Type crystais	71
4.	Epitaxy	/			97
	4.1	Liquid-	Phase Ep	itaxy	98
	4.2	Vapor-F	hase Epi	taxy	99
		4.2.1	System	Configuration	99
		4.2.2	VPE Che	emistries for GaAs	101
			4.2.2.1	Substrate orientation	101
			4.2.2.2	Halide process Ga-AsCl ₃ -H ₂	101
			4.2.2.3	Hydride process	
				Ga-AsH ₃ -HCl-H ₂	103
		4.2.3	MOCVD		103
			4.2.3.1	Process control and	
				mechanisms	105
			4.2.3.2	MOCVD sources	110
			4.2.3.3	Doping	110
			4.2.3.4	HBT growth	114
			4.2.3.5	Volume production	115
			4.2.3.6	Specific materials	117
			4.2.3.7	Selective epitaxy	119
			4.2.3.8	In situ monitoring of	
				epigrowth	119
	4.3	Molecul	ar Beam	Epitaxy	120
		4.3.1	System	Description	120
		4.3.2	MBE So	urces	122
			4.3.2.1	RHEED intensity oscillation	123
		4.3.3		Materials	124
				AlGaAs	124
			4.3.3.2	InGaAs	124
				InGaAlAs	124
				GaN and related alloys	124
		4.3.4	Doping		125
		4.3.5	HBT Gro		126
				AlGaAs HBT	126
			4.3.5.2	InGaP HBT	127

			4.3.5.3 InP HBT	127
			4.3.5.4 GaN HBT	128
		4.3.6	PHEMTs	128
	4.4	Atomic	Layer Epitaxy	129
		4.4.1	GaAs on Silicon Substrates	130
	4.5	Epilayer	Characterization	132
	4.6		ing Remarks	132
5.	Photoli	thograph	ny	137
	5.1	Introdu	ction	137
	5.2	Mask M	aking	138
	5.3	Basics o	f Printing/Imaging	139
		5.3.1	Typical Etch Photoresist Process	143
		5.3.2	Lift-Off Photoresist Process	143
	5.4	Photore	sist	145
		5.4.1	Resolution and Contrast	147
		5.4.2	Sensitivity	148
		5.4.3	Optical Photoresist Reaction Mechanism	149
		5.4.4	Image Reversal of a Positive Photoresist	149
		5.4.5	Negative Resists	150
		5.4.6	Resolution Improvement	152
	5.5	Physics	of Photolithograpy	152
		5.5.1	Diffraction	152
	5.6	Step and	d Repeat Projection Aligner	156
	5.7	Pattern Registration		
	5.8	Resist Processing		
		5.8.1	Prebake Dehydration	157
		5.8.2	Adhesion Promoter	157
		5.8.3	Resist Coating	158
		5.8.4	Soft Bake	158
		5.8.5	Exposure	159
		5.8.6	Standing Waves and Other	
			Interference Effects	160
		5.8.7	Developing	162
		5.8.8	De-scum	163
		5.8.9	Postbake	163
		5.8.10	Stripping	163
	5.9	Electron	Beam Lithography	164
	5.10	X-Ray Lithography		
	5.11	Process	Monitoring	166

Dielectric Passivation

188

6.6.3

	Plasm	a Proces	sing and Dry Etching	191			
	7.1	Plasma	a Processing	191			
		7.1.1	Plasma Basics	191			
		7.1.2	Glow Discharge Plasma	192			
		7.1.3	Voltage Distribution	195			
		7.1.4	Interaction of Ions with a				
			Surface/Sputter Yield	199			
	7.2	Dry Et	ching	202			
		7.2.1	Problems with Wet Etching	202			
		7.2.2	Advantages of Dry Etching	202			
	7.3	Plasma	Plasma Etch Systems				
		7.3.1	Reaction Basics	204			
		7.3.2	Rate Equation	206			
		7.3.3	Process Parameters	207			
		7.3.4	Plasma Etch System Types	208			
			7.3.4.1 Barrel reactor	208			
			7.3.4.2 Parallel-plate planar reactor	209			
			7.3.4.3 Downstream reactor	211			
			7.3.4.4 High-density plasma reactor	211			
			7.3.4.5 ECR	212			
			7.3.4.6 ICP	212			
			7.3.4.7 Ion milling	213			
	7.4	Etch Pi	rocesses	214			
		7.4.1	Etch Rate and Selectivity	215			
			7.4.1.1 Loading	215			
			7.4.1.2 Selectivity	216			
			7.4.1.3 Uniformity	216			
			7.4.1.4 Microuniformity	217			
		7.4.2	CD and Etch Profile	217			
	7.5		Plasma Etching of Materials Used in III–V IC				
		Proces	0	218			
		7.5.1	Selective Etches	219			
			Silicon Nitride and Oxide Etching	221			
		7.5.3	Metal Etching	222			
			7.5.3.1 Refractory metals	224			
			7.5.3.2 Aluminum	224			
			7.5.3.3 Gold/copper	224			
			7.5.3.4 Organic films	225			
	7.6		spect-Ratio Etching	225			
		7.6.1	Through-Wafer Via Etching	225			