CMOS AND BEYOND

Logic Switches for Terascale Integrated Circuits

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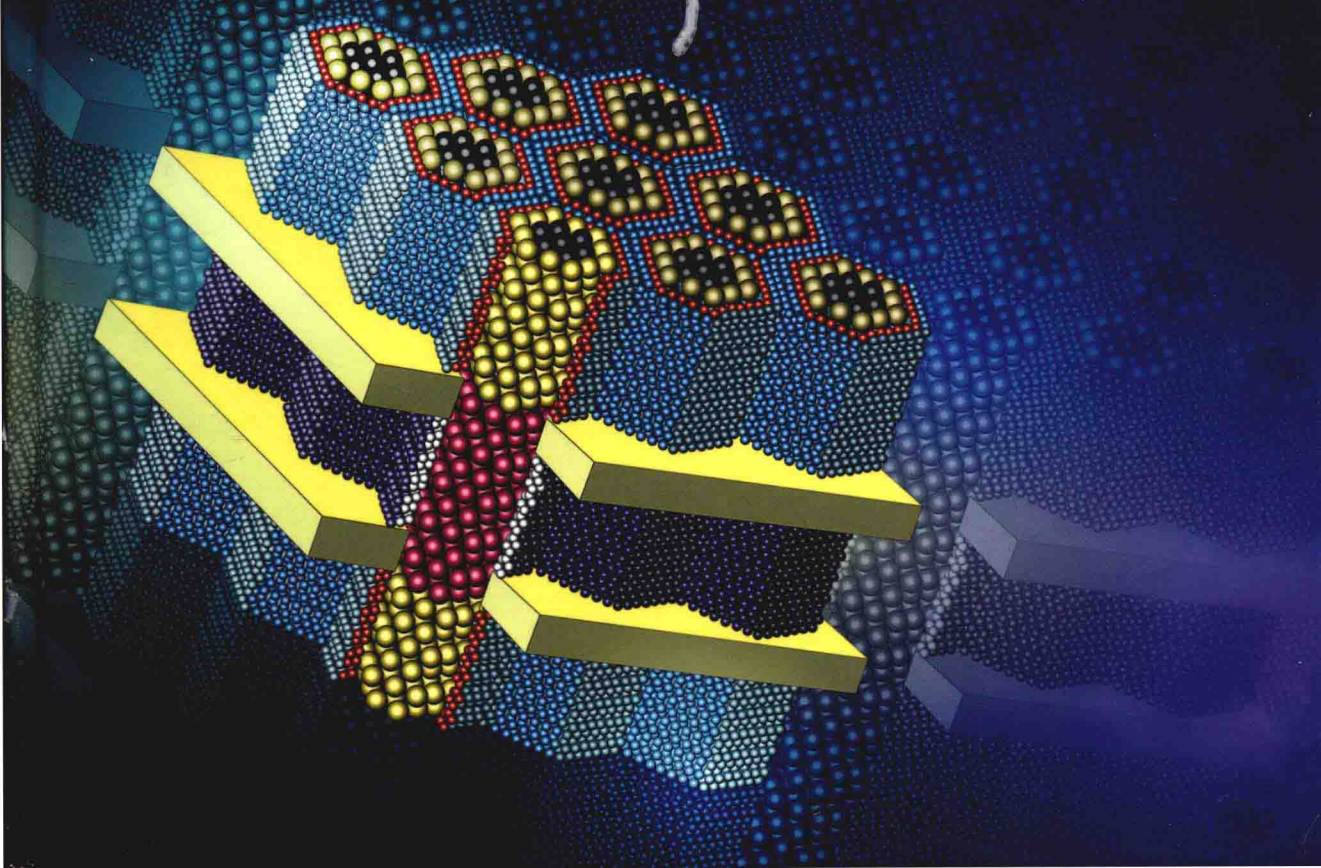
and Kelin Kuhn



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CMOS and Beyond

Get up to speed with the future of logic switch design with this indispensable overview of the most promising successors to modern CMOS transistors.

Learn how to overcome existing design challenges using novel device concepts, presented using an in-depth, accessible, tutorial-style approach. Drawing on the expertise of leading researchers from both industry and academia, and including insightful contributions from the developers of many of these alternative logic devices, new concepts are introduced and discussed from a range of different viewpoints, covering all the necessary theoretical background and developmental context.

Covering cutting-edge developments with the potential to overcome existing limitations on transistor performance, such as tunneling field-effect transistors (TFETs), alternative charge-based devices, spin-based devices, and more exotic approaches, this is essential reading for academic researchers, professional engineers, and graduate students working with semiconductor devices and technology.

Tsu-Jae King Liu is the TSMC Distinguished Professor in Microelectronics, Department of Electrical Engineering and Computer Sciences at the University of California, Berkeley. A co-inventor of the FinFET, she has been awarded the IEEE Kiyo Tomiyasu Award (2010), the Electrochemical Society Thomas D. Callinan Award (2011), and the SIA University Researcher Award (2014). She is a Fellow of the IEEE.

Kelin Kuhn is the Mary Upson Visiting Professor at Cornell University. She retired from Intel Corporation in 2014, where she was an Intel Fellow and Director of Advanced Device Technology in the Technology and Manufacturing Group at Intel Corporation. At Intel she was responsible for research on new device architectures and has been awarded two Intel Achievement Awards, one for high-k metal-gate (2006) and one for Trigate (2008), as well as the IEEE Paul Rappaport Award (2013). She is a Fellow of the IEEE.

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Preface

Steady miniaturization of CMOS (complementary metal–oxide–semiconductor) transistors – the predominant type of electrical switches used in digital integrated circuit "chips" – has yielded continual improvements in the performance and cost-per-function of electronic devices over the past four decades. This relentless miniaturization has resulted in ubiquitous information technology with dramatic global impact on virtually every aspect of life in modern society.

CMOS technology is reaching a state of maturity wherein continued transistor scaling will not be as straightforward in the future as it has been in the past. This is already apparent from the slowdown in certain aspects of scaling (e.g., chip supply voltage scaling, transistor off-state leakage current scaling, and so on). Clearly, improved switch designs will be needed to sustain the growth of the electronics industry beyond the next decade. A wide variety of alternative switch designs are being discussed in the research community, many of which use operating principles dramatically different from those of conventional CMOS transistors. Unfortunately, papers published by the research community in rapidly developing fields are rarely tutorial. Thus, much of this important new information is not readily comprehensible to the mainstream electronics community.

To help address this communication gap, we approached recognized experts in the research community with requests to create tutorial essays in their area of speciality. This book organizes these essays into sections, beginning with background information on the power–performance trade-off (motivating steep sub-threshold swing devices), continuing with tunneling-based devices, alternative field effect devices, and spin-based (magnetic) devices. It closes by reviewing the challenges of interconnects for these evolving new switch designs.

The first section reviews chip design considerations and benchmarks various alternative switching devices, with particular emphasis on devices with steeper sub-threshold swing. In Chapter 1, Elad Alon introduces the concepts underlying historical transistor scaling and analyses the key trade-offs between density, power, and performance which drive modern CMOS chip designs. Circuit design techniques such as power gating and parallelism are reviewed in context of constraints for continued dimensional scaling. The energy-efficiency limit for CMOS technology due to the 60 mV/dec sub-threshold swing limitation is discussed in relation to the potential benefit of beyond-CMOS devices with steeper sub-threshold swings. In Chapters 2 and 3, Zachery A. Jacobson and Kelin Kuhn review and benchmark a broad range of alternative devices being

explored in the research community. These chapters focus on electronic (as opposed to magnetic) devices that either incorporate new materials or mechanisms for enhanced switching behaviour. Chapter 2 briefly reviews the history and operating principles of these devices, while Chapter 3 benchmarks them with respect to drive current, energy efficiency, fabrication cost, complexity, and memory cell area. In Chapter 4, Asif Islam Khan and Sayeef Salahuddin explore the idea of overcoming the 60 mV/dec sub-threshold swing limit by incorporating a ferroelectric layer within the gate stack of a CMOS transistor. They discuss both the theory and recent experiments which support the possibility of achieving CMOS transistors with negative small-signal capacitance.

The second section covers device designs which utilize quantum mechanical tunneling as the switching mechanism to achieve steeper sub-threshold swing. In Chapter 5, Sapan Agarwal and Eli Yablonovitch assess the promise of tunnel field effect transistors (TFETs) in light of the requirements for simultaneous steep sub-threshold swing, large on/off-current ratio, and high on-state conductance. The authors explore the impact of p-n junction dimensionality and discuss various design trade-offs and the advantages of lateral, vertical, and bilayer implementations. Recent experimental data is evaluated in light of the various design requirements. In Chapter 6, Alan Seabaugh, Zhengping Jiang, and Gerhard Klimeck continue the discussion on TFETs, but with a focus on III-V semiconductor material systems. Design trade-offs for homojunction versus heterojunction III-V systems and challenges for achieving high performance with p-channel TFETs are discussed, along with non-idealities of particular relevance to III-V systems (such as traps, interface roughness, and alloy disorder). In Chapter 7, Qin Zhang, Pei Zhao, Nan Ma, Grace (Huili) Xing, and Debdeep Jena further extend the TFET discussion by evaluating the potential for TFETs built with graphene and two-dimensional semiconductor materials. In-plane tunneling and inter-layer tunneling devices are reviewed, and recent experimental results are assessed in relation to theoretical understanding. In Chapter 8, Dharmendar Reddy, Leonard F. Register, and Sanjay K. Banerjee review a novel tunneling device, the bilayer pseudospin field effect transistor (BiSFET). The BiSFET relies on the possibility of room temperature excitonic (electron-hole) superfluid condensation in two dielectrically separated graphene layers. Formation of a room temperature condensate is essential for BiSFET operation, and the authors discuss the key physics and challenges of creating such a condensate. BiSFET compact models and circuit designs are also discussed and used to project performance benefits over CMOS.

The third section covers devices that employ alternative approaches to achieving steeper switching behaviour. In Chapter 9, You Zhou, Sieu D. Ha, and Shriram Ramanathan discuss the possibility of making devices from electron correlated materials, which can transition between insulator and metal phases. The authors discuss the physics of the metal–insulator transition, with particular emphasis on the vanadium dioxide (VO_2) system. Mott FET devices, solid-state VO_2 FETs and ionic liquid-gated VO_2 FETs are reviewed and circuit architectures which exploit these devices are discussed. In Chapter 10, Paul M. Solomon, Bruce G. Elmegreen, Matt Copel, Marcelo A. Kuroda, Susan Trolier-McKinstry, Glenn. J. Martyna, and Dennis M. Newns introduce piezoelectronic transistor (PET) devices. The PET is essentially a solid-state relay

in which a piezoelectric element provides the mechanical force and a piezoresistive element transduces the mechanical force to electrical switching. The basic physics of piezoelectric and piezoresistive materials are discussed, along with process integration challenges. PET dynamics, compact models, and circuit designs are also discussed and used to project performance benefits over CMOS. In Chapter 11, Rhesa Nathanael and Tsu-Jae King Liu discuss nanoscale electromechanical relays as logic switches. Relays use mechanical movement to physically short or open an electrical connection between two contacts, and have the ideal characteristics of zero off-state leakage current, abrupt sub-threshold swing, and low gate leakage. The authors review materials requirements and process integration challenges specific to nanorelays, describe a variety of relay designs that provide for more compact implementation of complex logic circuits, and discuss scaling methodologies.

The fourth section covers devices that use magnetic effects or electronic spin to carry information. These can be used to implement nanomagnetic logic (wherein small magnets are used to construct circuits), spin torque logic, or spinwave logic (wherein electron spin is the information token). In Chapter 12, György Csaba, Gary H. Bernstein, Alexei Orlov, Michael T. Niemier, X. Sharon Hu, and Wolfgang Porod discuss the possibility of making circuits out of small single-domain magnets. The switching properties of single-domain nanomagnets are introduced and various clocking schemes are discussed. A full-adder structure is benchmarked against CMOS and design issues in nanomagnetic logic are reviewed. In Chapter 13, Dmitri E. Nikonov and George I. Bourianoff introduce the possibility of making majority gate logic circuits using the spin torque effect. In these devices the combined action of spin torques from the various inputs transfers enough torque to switch the magnetization of the output. Detailed simulations of in-plane and perpendicular spin torque switching are reviewed. An adder circuit is discussed and benchmarked against CMOS. In Chapter 14, Alexander Khitun analyses the possibility of using spin waves for logic functions. A spin wave is a collective oscillation of spins in a spin lattice around the direction of magnetization. The physics of spin wave devices is introduced and experimental results discussed. Various spin wave circuits and architectures are reviewed and benchmarked against CMOS.

A critical (but frequently neglected) issue in assessment of beyond CMOS devices is the interconnect architecture. Creating a fabulous new switch is valueless if it cannot be connected to other active or passive devices! This is particularly relevant for magnetic and spin-based devices as they do not (typically) interface directly to conventional electronic devices. Thus, in Chapter 15, Shaloo Rakheja, Ahmet Ceyhan, and Azad Naeemi close this book with a comprehensive evaluation of the interconnect considerations for advanced logic devices. This includes both interconnect options for emerging charge-based device technologies and interconnect options for spin-based technologies.

Our hope is that these essays will help to bridge the gap between research on emerging devices and their practical implementation in terascale integrated circuits by the mainstream semiconductor community.

Contents