Large Scale Integration

Devices, Circuits, and Systems

Edited by

M. J. Howes
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Series Preface

The Oxford Dictionary defines the word revolution as 'a fundamental reconstruction'; these words fittingly describe the state of affairs in the electronic industry following the advent of solid state devices. This 'revolution', which has taken place during the past 25 years, was initiated by the discovery of the bipolar junction transistor in 1948. Since this first discovery there has been a worldwide effort in the search for new solid state devices and, although there have been many notable successes in this search, none have had the commercial impact which the transistor has had. Possibly no other device will have such an impact; but the commercial side of the electronics industry stands poised, awaiting the discovery of new devices as significant perhaps as the transistor.

Research and development in the field of solid state devices has concerned itself with two important problems. On the one hand we have device physics, where the aim is to understand in terms of basic *physical concepts* the mode of operation of the various devices. In this way one seeks to optimize the technology in order to achieve the best performance from each device. The second aspect of this work is to consider the important contribution of the circuit to the operation of a device. This problem has been called *device circuit interaction*. It is a great pity that in the past these two major aspects of the one problem have been tackled by separate groups of scientists with little exchange of ideas. In recent years, however, this situation has been somewhat remedied, the improvement being due directly to the very rigorous system specifications demanded by industry. Such demands constantly require greater performance from devices, which can only be brought about by coordinated team work.

The objective of this new series of books is to bring together the two aspects of this problem: device physics and device circuit interactions. We hope to achieve, by coordinated co-authorship of leading experts in the respective fields, a varied and balanced review of past and current work. The

books in the series will cover many aspects of device research and will deal with both the commercially successful and the more speculative devices. Each volume will be an in-depth account of one or more devices centred on some common theme. The level of the text is designed to be suitable for the graduate student or research worker wishing to enter the field of research concerned. Basic physical concepts in semiconductors and elementary ideas in passive and active circuit theory will be assumed as a starting point.

M. J. HOWES
D. V. MORGAN

University of Leeds
December 1978

Preface

The transistor and its many and varied solid state derivatives offer many potential advantages to the electronics industry. These include small size, low power consumption, and suitability for mass production. The full extent of these advantages can, however, only be realized when the transistor is fabricated as part of a fully integrated circuit. Thus, by the end of the late 1950s and only a decade after the development of the bipolar transistor it was recognized that it should be possible to incorporate on the same silicon chip not only a number of transistors and diodes but also other key electronic components, such as resistors, capacitors, and interconnections. The result is the now familiar integrated circuit (IC) and at the present time ICs incorporating 10^5 active components on a semiconductor chip ($5 \times 5 \times 0.25$) mm in size are commercially available. This technology is termed Large Scale Integration (LSI). Current research work is aimed at extending the technology to very large scale integration (VLSI) with device dimensions at the submicron level.

The impact of this science on the future is by any standards likely to be massive. It has, for example, initiated the current microprocessor revolution which has in a few years affected all aspects of Western societies. In this the fifth volume in the series on solid state devices and circuits we cover all aspects of present day LSI systems. The first chapter presents an introduction to the topic. This is followed by two chapters (2 and 3) dealing with the two basic device structures, BJTs, and FETs. LSI circuits with their extensive array of components present the engineer with a formidable problem in terms of design and testing—this topic is covered in Chapter 4. Chapter 5 considers in detail the basis of LSI technology whilst Chapter 6 deals with memory and design technology. In the final chapter consideration is given to custom design of circuits.

The editors wish to thank most warmly the authors contributing to this volume. They are particularly indebted to Professor A. E. Ash FRS (Univer-

sity College, London) and Dr John Mavor (University of Edinburgh) for their valuable advice and encouragement in preparing this volume. It is a pleasure to thank our wives Jean (Morgan) and Dianne (Howes) for their assistance in checking and correcting the text.

M. J. HOWES
D. V. MORGAN

University of Leeds
February 1980

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CHAPTER 1

Introduction

D. H. ROBERTS

In the late 1950s, only a decade after the development of the transistor, it was recognized that within the same single crystal chip of silicon it should be possible to fabricate not only a modest number of transistors and diodes, but also the other key electronic components, resistors and capacitors. This concept was initially termed the silicon solid circuit and later the silicon integrated circuit (SIC). In the past two decades the technology has developed to the point where SICs containing approximately 100,000 active components are commercially available. Such SICs consist of a single crystal chip of silicon, typically $5 \times 5 \times 0.25$ mm in size, mounted in a package of typical dimensions $2 \times 1 \times 0.5$ cm, from which the one 'micro' aspect of this technology is self-evident.

Indeed the original incentive to develop this technology stemmed from the twin needs of reducing the size of electronic equipment while simultaneously increasing both the complexity and its reliability.

After one or two false starts using alternative technological approaches, the electronics industry, or more specifically the semiconductor industry, homed in on the use of silicon technology as the way to improve simultaneously the size, the reliability, and the complexity or sophistication of electronics equipment.

At this stage nothing has been said about two key parameters, cost and performance. In fact, however, what has happened is that the changes in technology and design which were introduced in the interest of size reduction and reliability improvement, have *ipso facto* led to dramatic reductions in cost and improvement in performance. It is the cost reduction in particular which has led to the much publicized concept of the pervasiveness of silicon technology, the point being not simply the increased penetration of silicon integrated circuits in the electronic industry, but also both their use in roles previously served by mechanical or electromechanical products (e.g. watches and telecommunications switching) and in totally new applications which

were not previously economically practicable (e.g. pocket calculators and sophisticated telephone handsets).

1.1 PROGRESS TO DATE

This can be seen in Figures 1.1–1.3, which deal respectively with the performance of digital circuits (using power-delay product as the figure of merit), the increased complexity of state-of-the-art products (over the past 15 years), and the subsequent price per logic gate over the same period. A direct result of that progress is the availability at this time of 16 K bit per chip memory products, and microprocessors.

The current state of the art in complexity terms can be seen in Figure 1.2. In terms of various performance criteria it can be represented by such examples as:

(i) Power delay product: values below 0.1 pJ are achievable with gate delays of a few tens of nanoseconds.
(ii) Gate delay: on-chip gate delays of better than 0.25 ns are achievable.
(iii) Counter input frequency: divide by four circuits operating with inputs above 2 GHz have been made.
(iv) Wideband amplifiers, amplifiers with useful flat gain up to 1 GHz are now available.
(v) Power and voltage: these tend to be chip area–cost limited. Current performance is at the 10–20 W and 100 V level.

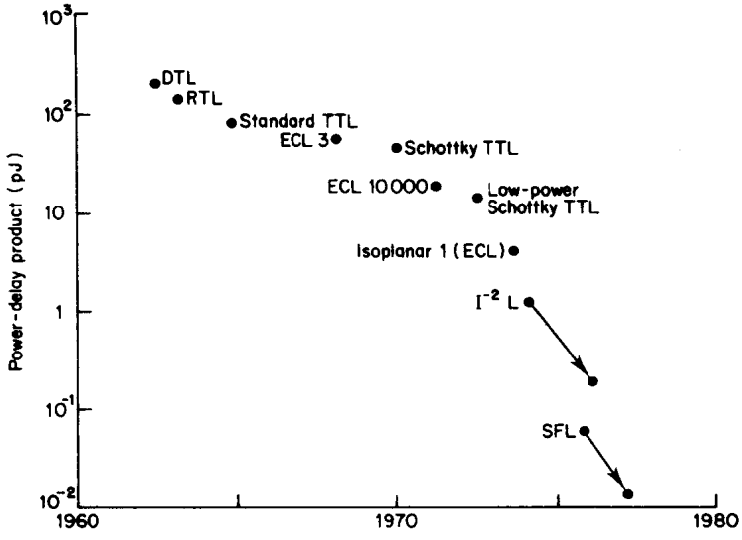

Figure 1.1. Power-delay product versus time. (Reproduced by permission of *Phil. Trans. Roy. Soc., London A*, **289**, 93–101 (1978))

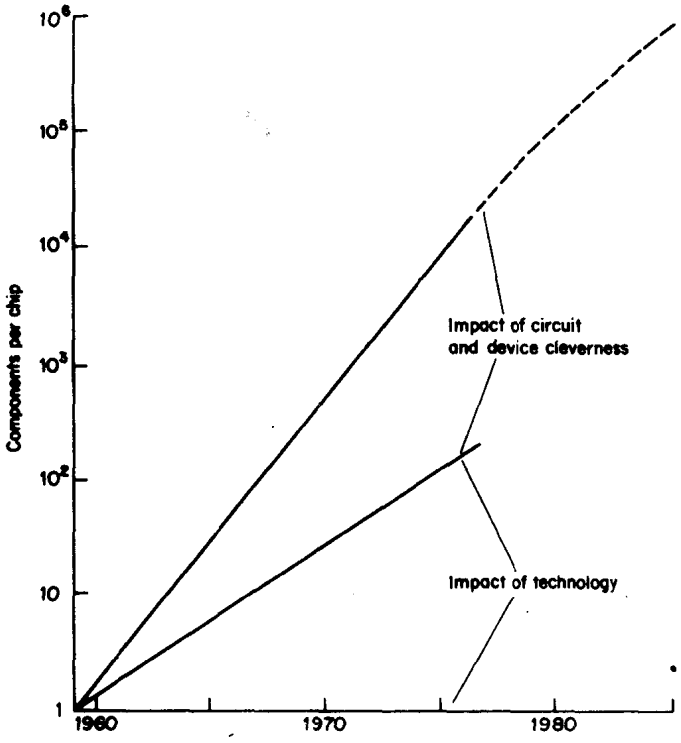

Figure 1.2. Complexity versus time. (Reproduced by permission of the IEE from *Electronics and Power*)

(vi) Memory retention: optimized EAROM circuits should give 10 year memory retention.

While in terms of device complexity there would appear to be two orders of magnitude available for extension in the next few years, in the case of performance the available 'stretch factor' would appear to be more like a factor of 2. There appear to be two reasons for this:

(a) the fact that basic limitations, such as carrier velocity, are becoming significant.

(b) The fact that alternative materials–techniques offer a competitive solution to the same system need. This will be enlarged upon below.

1.2 DESIGN DECISIONS

These start with a full appreciation of the cost impact of SIC technology. The cost of a SIC is a function of the design and development cost, amortized over the production volume, the manufacturer's efficiency in processing silicon, and in assembling and testing the finished product. The precise relation is

given in Equation 1.1:

$$C_N = D + c + NS/n + N(P + A + T), \tag{1.1}$$

where C_N is the cost of N devices, D the cost of design, c the special capital, S the silicon slice processing, n the good chips per slice, P the package, A the assembly operation and T the test operation. Further examination of that relation shows that simple SICs are cost-dominated by package, assembly and testing costs, while the cost of complex SICs is determined primarily by silicon processing (the percentage yield of 'good' product being the dominant factor), and design. This leads to the curve given in Figure 1.4, from which can be identified a broad minimum, toward the optimum scale of integration (OSI), which represents that level of chip complexity which leads to minimum full-time equipment costs.

As is to be expected from the trends illustrated in Figure 1.2, OSI is dramatically time-dependent, leading to the curves shown in Figure 1.5. These curves deal with the situation where the production volume is sufficient for the design cost to be insignificant. Increasingly this is not the case and the cost-effectiveness of DESIGN needs further consideration.

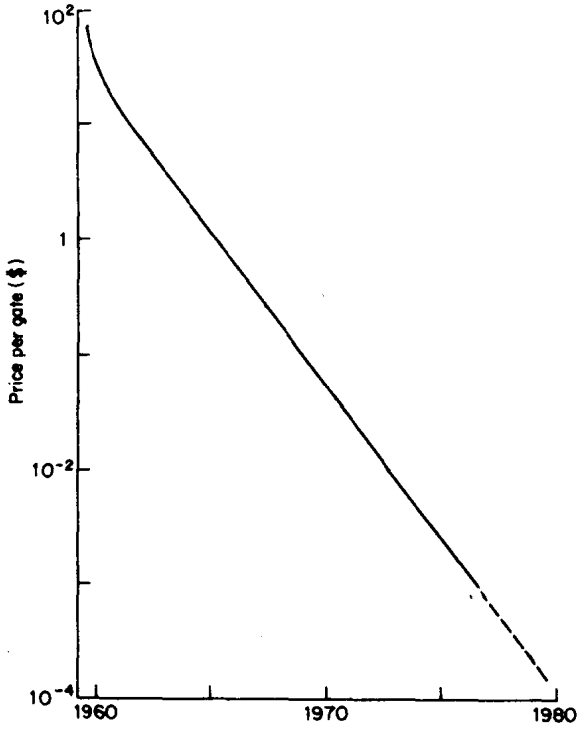

Figure 1.3. Price per gate versus time. (Reproduced by permission of the IEE from *Electronics and Power*)

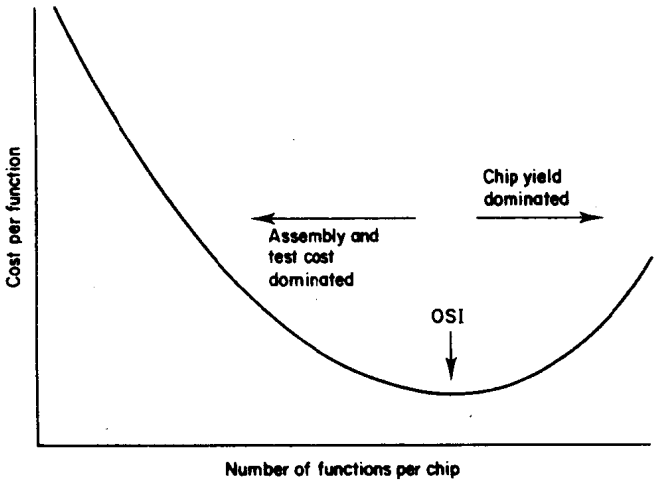

Figure 1.4. Cost versus complexity. (Reproduced by permission of *Phil. Trans. Roy. Soc., London A*, **289**, 93–101 (1978))

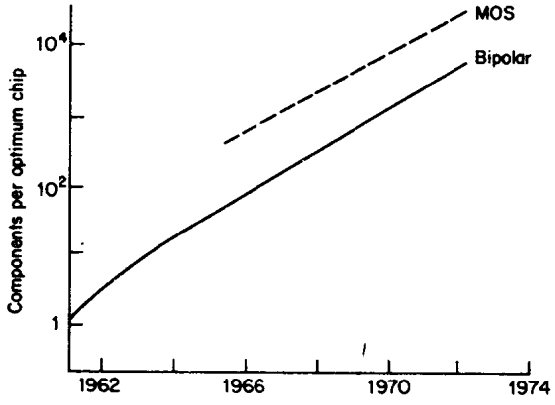

Figure 1.5. 'OSI' versus time. (Reproduced by permission of *Phil. Trans. Roy. Soc., London A*, **289**, 93–101 (1978))

1.2.1 The reality of custom design

In using silicon integrated circuits there are three design options available to the equipment–system designer:

ROUTE (i) DESIGN INVOLVEMENT AT SILICON CHIP LEVEL—CUSTOMIZED CHIP

ROUTE (ii) DESIGN INVOLVEMENT AT MICROPROCESSOR LEVEL—CUSTOMIZED PROGRAM

ROUTE (iii) DESIGN INVOLVEMENT AT THE PCB LEVEL—CUSTOMIZED PCB

The relationship of these 3 design routes is illustrated in Figure 1.6. It is to be expected that in complex systems all 3 design routes will be in use, each selected as the optimum solution to the particular sub-system need. In order that this process of optimization can be performed efficiently there are three key needs:

1. Efficient CAD methodology from system down to chip level, tied into automatic test.

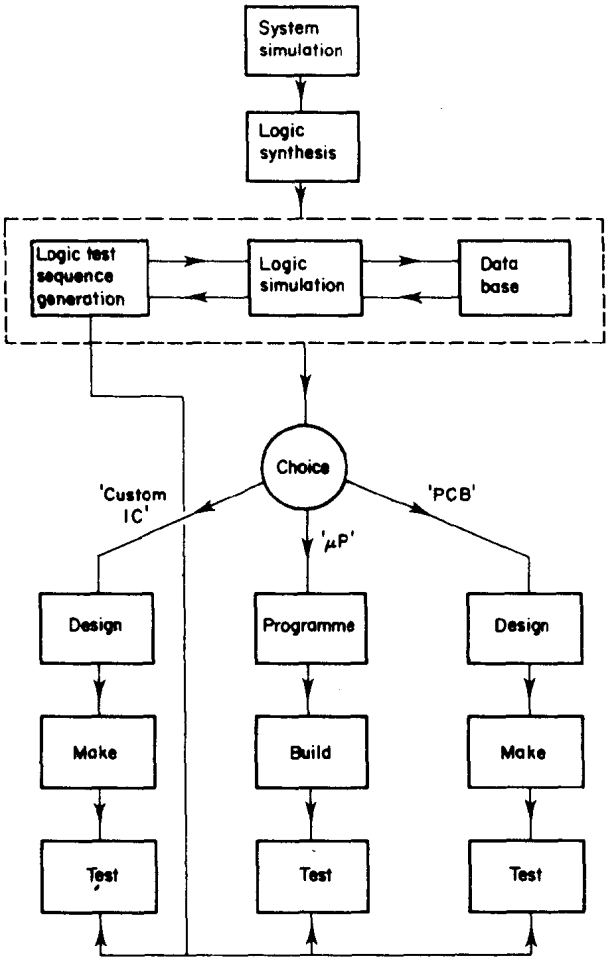

Figure 1.6. Integrated design system for programmable electronics

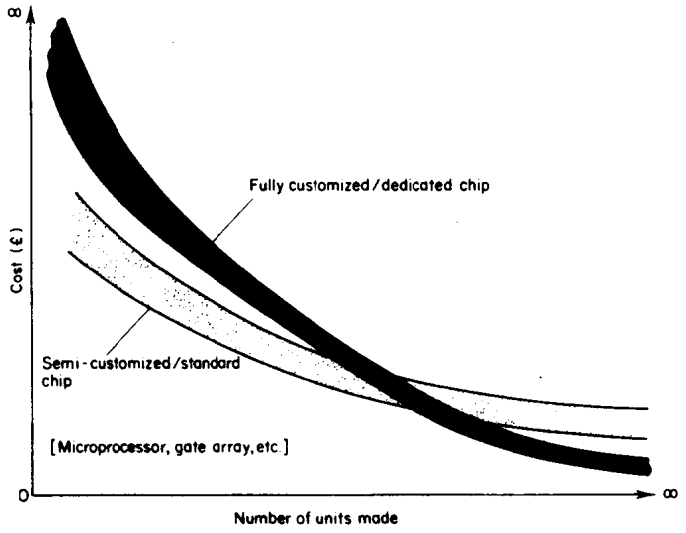

Figure 1.7. Example of cost/volume choices—modest performance digital ICs

2. Data base support for CAD. This data base needs to contain sufficient information for cost and performance trade-offs to be built into the system simulation stage. It needs to know the shape of the curves indicated in Figure 1.7 for example.

1.2.1.1 Design evolution

Adequate recognition is needed of the time-dependent factors in design route optimization. Two illustrations:

(i) The shape of the curves given in Figure 1.7 are strongly time dependent and subject to change in terms of such parameters as trade off between chip cost, assembly and test costs, and low volume launch costs—dependent on CAD efficiency.

(ii) One can easily imagine 4 alternative design routes in which the use of a standard microprocessor is the preferred first step:
   (a) Standard micro → Customized micro
   (b) Standard micro → Customized non-programmable
   (c) Standard micro → Standard micro (same)
   (d) Standard micro → Standard micro (Mark '*N*')

   In each case the use of a standard microprocessor during the design, pre-production and early production phases can be desirable as well as essential.