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Technologies and Tradeoffs

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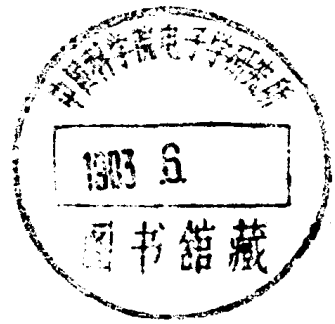

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Preface

VHSIC is an acronym that stands for very high speed integrated circuit(s) and refers to large-scale digital integrated circuits with typical logic-gate propagation delays below 1 nanosecond. Historically bipolar technology was first to enter into this speed range; however, metal oxide silicon (MOS) and gallium arsenide (GaAs) technologies are now also available.

In addition to the challenge of technology, VHSIC presents the challenge of complexity. Placing about 20,000 logic gates onto an integrated-circuit chip presents a design problem with a complexity that limits the application of the *custom-logic* approach of assembling a chip layout one logic gate at a time. This limitation is alleviated by the introduction of the *functional cell* (also known as macrocell, library-cell, mosaic-cell, polycell, standard cell): an assembly of logic gates into a functional unit such as a multibit arithmetic-logic unit (ALU), a multibit multiplier, or a programmable logic array (PLA). Another approach is provided by the *gate array*: a fixed array of logic gates that can be interconnected as required.

The aim of this book is to explore the tradeoffs among custom logic, functional cells, and gate arrays, as well as among the bipolar, MOS, and GaAs technologies—with the principal goal of providing guidance for the user. The specific circuits discussed use 1 μm transistor geometries and include emitter-coupled logic (ECL) and integrated injection logic (I^2L) in the bipolar technology, *n*-channel MOS (NMOS) logic and complementary MOS (CMOS) logic in the MOS technology, and depletion-mode logic and enhancement-mode logic in the GaAs technology.

Following an introductory chapter, three chapters deal with the bipolar, MOS, and GaAs technologies, and the remaining chapters are concerned with the application of these technologies to gate arrays, custom logic, and

functional cells. To gain visibility, simple explicit expressions are used wherever possible, even when their use leads to ~30% errors in propagation delays.

The text includes 47 worked examples on realistic applications, as well as 68 unworked problems to aid self-study. Answers to selected problems are also given.

ARPAD BARNA

Stanford, California
May 1981

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† Denotes optional material

ONE

Preliminaries

This chapter provides a short historical overview of the origins of very high speed integrated circuits (VHSIC). It also summarizes various capacitance relations for later use.

1.1 HISTORICAL OVERVIEW

In the wake of investigations on semiconductor diodes in the early 1940s came the invention of the transistor in 1948.[1] During the 1950s transistors found many applications in the electronics industry; the decade also heralded the invention of the integrated circuit.[2] Commercially available digital integrated circuits of the 1960s used bipolar silicon technology and provided for the widespread use of transistor–transistor logic (TTL) and emitter-coupled logic (ECL) circuits.

The 1970s witnessed the introduction and rapid spread of various metal oxide silicon (MOS) technologies, leading to larger and more complex integrated circuits, such as semiconductor memories and microprocessors. These circuits have been utilized in a variety of applications, both within and outside the traditional areas of electronics. Complexity of the largest circuits has increased by about a factor of 2 every two years.[3]

Semiconductor technology also found applications in high-speed circuits. Transistors with gain-bandwidth products of several hundred megahertz were introduced in the late 1950s, and they quickly led to transistor circuits operating at nanosecond speeds.[4] Because of their lower power consumption, small size, and greater reliability, circuits utilizing transistors have gradually replaced the majority of circuits using vacuum tubes.

Unfortunately, the penetration of integrated-circuit technology into the realm of high-speed circuits has been quite slow. Small-scale ECL integrated circuits with propagation delays of ≈ 2 nsec were introduced in the mid 1960s, and some with propagation delays of ≈ 1 nsec in the late 1960s. The complexity of such ECL chips increased to hundreds of logic gates in the 1970s.

The slow evolution of high-speed integrated circuits has been a disappointment to the users of high-speed circuits. To alleviate this situation, an increasing number of instrument and computer manufacturers have established semiconductor operations dedicated to their own needs, while many other users have waited for the situation to improve. However, by the late 1970s it became clear that the general availability of high-speed integrated circuits would not improve significantly unless some positive action was taken.

The VHSIC program started in the late 1970s, primarily to increase the availability of high-speed integrated circuits for military use. In addition, as hoped, the VHSIC program has also catalyzed work that is applicable to nonmilitary use as well, including considerations of design and technology tradeoffs that provided the impetus for writing this book.

1.2 CAPACITANCES

This section summarizes capacitances of various structures for use in later chapters. Capacitances due to fringing fields are included when applicable.[5, 6]

1.2.1 Two Parallel Plates

Two views of this configuration are shown in Figure 1.1. When the entire space between and in the vicinity of the plates is filled by material with a relative dielectric constant ε_r, the capacitance between the two plates can be approximated as

$$C=\varepsilon_0\varepsilon_r\frac{(L+0.8H)(W+0.8H)}{H}, \tag{1.1a}$$

provided that

$$L\geq 0.5H, \tag{1.1b}$$

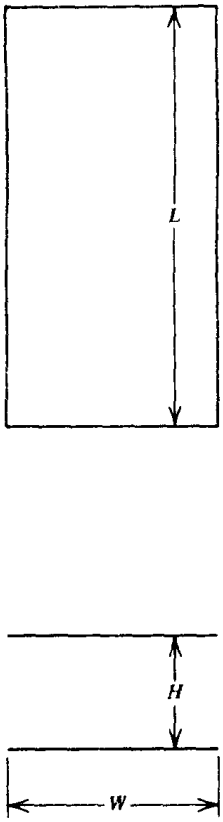

Figure 1.1 Two parallel plates, each with width W and length L, separated by a distance H.

and that

$$W \geq 0.5H. \tag{1.1c}$$

In eqs. (1), C is the capacitance in farads (F), $\varepsilon_0 = 8.85 \times 10^{-12}$ F/m, and L, W, and H are in meters (m).

Example 1.1 An integrated circuit uses a two-level metal system. The two levels are separated by silicon dioxide (SiO_2) with a thickness of $H = 1$ μm and $\varepsilon_r = 3.9$. Compute the interlevel capacitance between two parallel lines in the configuration of Figure 1.1 with widths of $W = 3$ μm and lengths of $L = 1$ mm. As a crude approximation, assume that the metal lines have zero thicknesses.

First we check whether the conditions of eqs. (1.1b) and (1.1c) are met. We can see that eq. (1.1b) is satisfied:

$$L = 1 \text{ mm} \geq 0.5H = 0.5 \times 1 \text{ μm} = 0.5 \text{ μm}.$$

Also, eq. (1.1c) becomes

$$W=3\ \mu\text{m}\geq 0.5H=0.5\times 1\ \mu\text{m}=0.5\ \mu\text{m},$$

which is also satisfied. Thus we proceed with eq. (1.1a):

$$\begin{aligned}C&=\varepsilon_0\varepsilon_r\frac{(L+0.8H)(W+0.8H)}{H}\\&=8.85\times 10^{-12}(\text{F/m})\\&\quad\times 3.9\frac{(10^{-3}\ \text{m}+0.8\times 10^{-6}\ \text{m})(3\times 10^{-6}\ \text{m}+0.8\times 10^{-6}\ \text{m})}{10^{-6}\ \text{m}}\\&=0.13\times 10^{-12}\ \text{F}=0.13\ \text{pF}.\end{aligned}$$

1.2.2 Plate Above Plane

Two views of this configuration are shown in Figure 1.2. Note that the plane is infinite in all directions. When the entire space above the plane is filled by material with a relative dielectric constant ε_r, the capacitance between the plate and the infinite plane can be approximated as

$$C=\varepsilon_0\varepsilon_r\frac{(L+1.6H)(W+1.6H)}{H} \tag{1.2a}$$

provided that

$$L\geq H, \tag{1.2b}$$

and that

$$W\geq H. \tag{1.2c}$$

Again, capacitance C is in farads when L, W, and H are in meters, and $\varepsilon_0=8.85\times 10^{-12}$ F/m.

Example 1.2 An integrated circuit uses a two-level metal system. The two levels are separated by silicon dioxide (SiO_2) with a thickness of $H=1$ μm and with $\varepsilon_r=3.9$. Compute the interlevel capacitance between a large plane in one level and a line in the other level, if the line

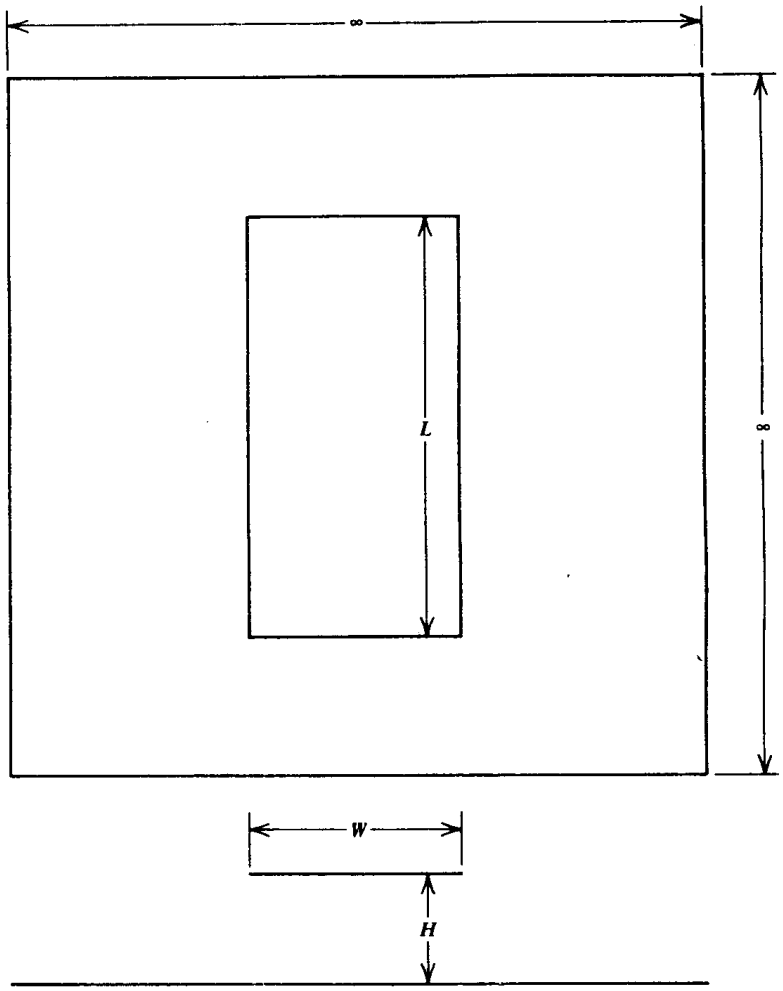

Figure 1.2 A plate with width W and length L at a height H above an infinite plane.

has a width of $W=3$ μm and a length of $L=1$ mm. As a crude approximation, assume that the metal line has zero thickness.

First we check whether the conditions of eqs. (1.2b) and (1.2c) are met. We can see that eq. (1.2b) is satisfied:

$$L=1 \text{ mm} \geq H=1 \ \mu\text{m}.$$

Also, eq. (1.2c) becomes

$$W=3 \ \mu\text{m} \geq H=1 \ \mu\text{m},$$

which is also satisfied. Thus we proceed with eq. (1.2a):

$$C=\varepsilon_0\varepsilon_r\frac{(L+1.6H)(W+1.6H)}{H}$$

$$=8.85\times10^{-12}(\text{F/m})$$

$$\times3.9\frac{(10^{-3}\text{ m}+1.6\times10^{-6}\text{ m})(3\times10^{-6}\text{ m}+1.6\times10^{-6}\text{ m})}{10^{-6}\text{ m}}$$

$$=0.16\times10^{-12}\text{ F}=0.16\text{ pF}.$$

1.2.3 Plate Between Two Planes

Two views of this configuration are shown in Figure 1.3. Note that both planes are infinite in all directions and that the two planes are electrically connected by means not shown in the figure. When the entire space between the two planes is filled by material with a relative dielectric constant ε_r, the capacitance between the plate and the two planes can be approximated as

$$C=\varepsilon_0\varepsilon_r\frac{2(L+0.9H)(W+0.9H)}{H}, \tag{1.3a}$$

provided that

$$L\geq0.5H, \tag{1.3b}$$

and

$$W\geq0.5H. \tag{1.3c}$$

Again, capacitance C is in farads when L, W, and H are in meters, and $\varepsilon_0=8.85\times10^{-12}$ F/m.

Example 1.3 An integrated circuit uses a metal system that consists of three levels separated by SiO_2 layers with $\varepsilon_r=3.9$ and with thicknesses of $H=1$ μm. Compute the capacitance from a line in the second level to large ground planes in the first and third levels. The line has a width of $W=3$ μm and a length of $L=1$ mm and can be approximated as having zero thickness.

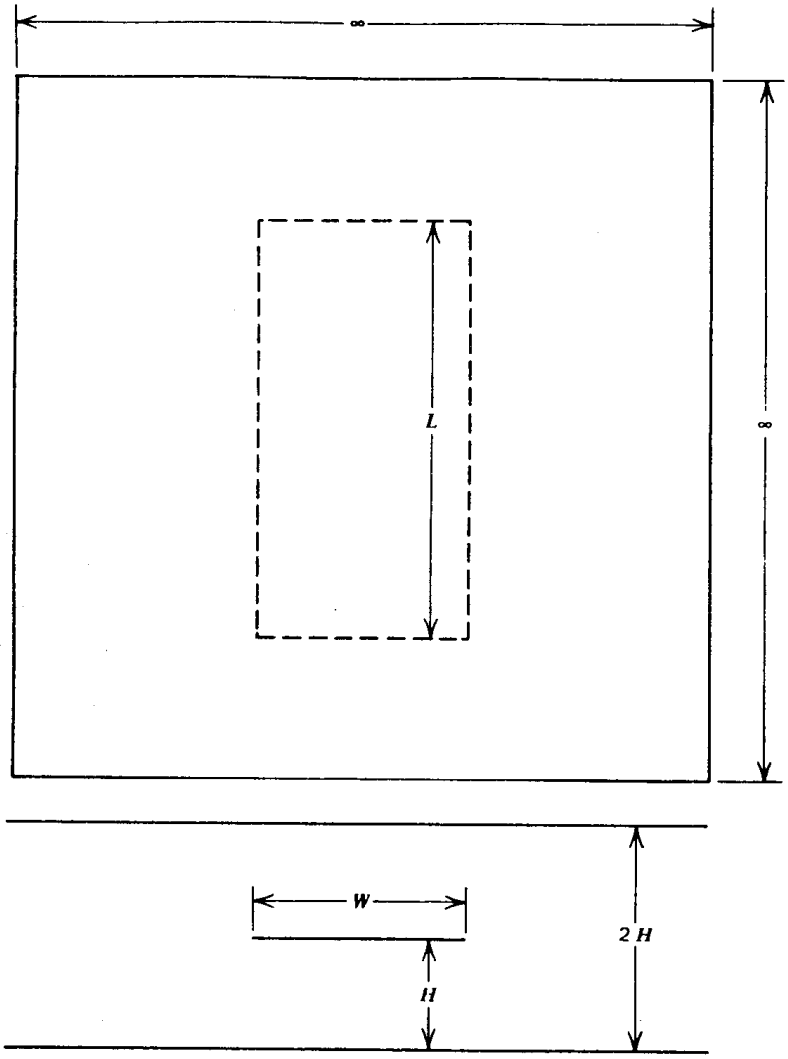

Figure 1.3 A plate with width W and length L halfway between two infinite planes separated by a distance $2H$.

First we check whether the conditions of eqs. (1.3b) and (1.3c) are met. We can see that eq. (1.3b) is satisfied:

$$L = 1 \text{ mm} \geq 0.5H = 0.5 \times 1 \ \mu\text{m} = 0.5 \ \mu\text{m}.$$

Also, eq. (1.3c) becomes

$$W = 3 \ \mu\text{m} \geq 0.5H = 0.5 \times 1 \ \mu\text{m} = 0.5 \ \mu\text{m},$$

which is also satisfied. Thus we proceed with eq. (1.3a):

$$C=\varepsilon_0\varepsilon_r\frac{2(L+0.9H)(W+0.9H)}{H}$$

$$=8.85\times10^{-12}(\text{F/m})$$

$$\times3.9\times2\frac{(10^{-3}\text{ m}+0.9\times10^{-6}\text{ m})(3\times10^{-6}\text{ m}+0.9\times10^{-6}\text{ m})}{10^{-6}\text{ m}}$$

$$=0.27\times10^{-12}\text{ F}=0.27\text{ pF}.$$

1.2.4 Two Coplanar Strips

Two views of this configuration are shown in Figure 1.4. The quantity $C/[\varepsilon_r(L+W+D)]$ is shown in Figure 1.5 as a function of W/D. Capacitance C is in picofarads and the pF/m scale applies when L, W, and D are in meters; capacitance C is in femtofarads and the fF/mm scale applies when L, W, and D are in millimeters.

Example 1.4 An integrated circuit uses a metal system with line widths of $W=3$ μm and with spacings between lines of $D=2$ μm.

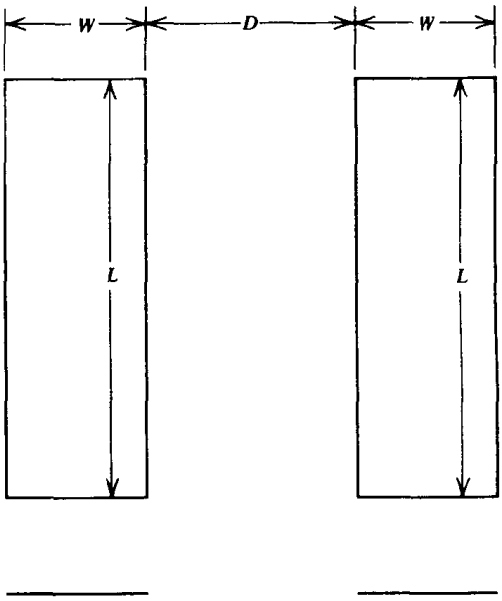

Figure 1.4 Two coplanar strips each with width W and length L, separated by a distance D.

Compute the capacitance between the two parallel coplanar lines with lengths of $L=1$ mm. As crude approximations, assume that the entire space surrounding the lines is filled by SiO_2 ($\varepsilon_r=3.9$) and that the metal lines have zero thicknesses.

We have $W/D=3\ \mu m/2\ \mu m=1.5$. From Figure 1.5 we get

$$\frac{C}{\varepsilon_r(L+W+D)}=15\ \text{fF/mm}.$$

Thus the capacitance

$$C=15(\text{fF/mm})\times 3.9(1\ \text{mm}+3\times 10^{-3}\ \text{mm}+2\times 10^{-3}\ \text{mm})=59\ \text{fF}.$$

When the strips of Figure 1.4 are sandwiched between two different materials with relative dielectric constants ε_{r1} and ε_{r2}, then

$$\varepsilon_r=\frac{\varepsilon_{r1}+\varepsilon_{r2}}{2} \tag{1.4}$$

should be used for ε_r.

Example 1.5 An integrated circuit incorporates the metal structure of Figure 1.4 with $W=1\ \mu m$, $D=4\ \mu m$, and $L=10\ \mu m$. The structure is

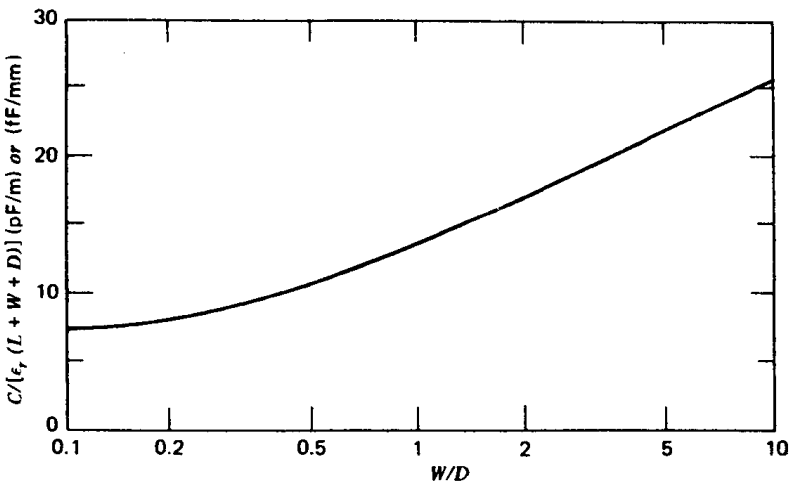

Figure 1.5 $C/[\varepsilon_r(L+W+D)]$ as a function of W/D for the configuration of Figure 1.4.