1985年
世界集成电路大全

7

上海交通大学微机研究所·南洋电脑开发总公司

1985年世界集成电路大全

7 商业产品

上海交通大学微机研究所　　南洋电脑开发总公司

1985年10月

1985

IC MASTER

VOLUME I

MIC-PC/XT

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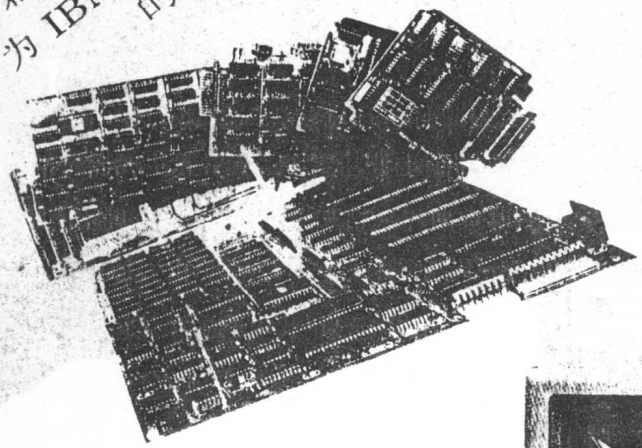
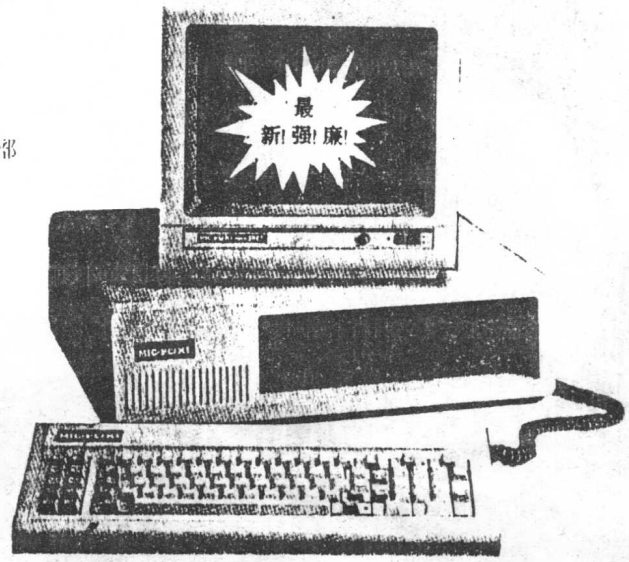


IBM-PC/XT 及各种兼容机的软件和扩充硬件均可在本系统中顺利运行

中西文多用戶系统，IBM-PC 网络及其他多种局部网络支持，数百种中西文的科技，文教，管理，商业，计算机辅助设计和图像处理软，硬件任君选择维修服务点遍布海外，解除用戶后顾之忧

可用人民币购买也可用美元订购，保用一年基本系统包括 512 K内存，360 K软盘 135 W开关电沅，IBM-PC 兼容键盘单色高分辨率显示器及显示打印卡，可用中文，期货售价人民币七仟元起，美元售价九百元起。可增配 10M/20 20 M 溫盘，也可换用采色显示器……，欢迎来函来电垂询。



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国外维修：香港思沅电脑有限公司
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出版说明

一. <<1985年世界集成电路大全>>是根据美国最新出版的<<1985 IC MASTER>>一书编印而成的。<<大全>>的页号编排完全按原著编印的。现发现本书的每一册都有些空页，可能由于原著者为了便于修订、补充本书内容而留有余地等原因所之，特此说明，并把每一册空页列表如下：

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1	209-299	4	3191-3300
	433-449		3488-3499
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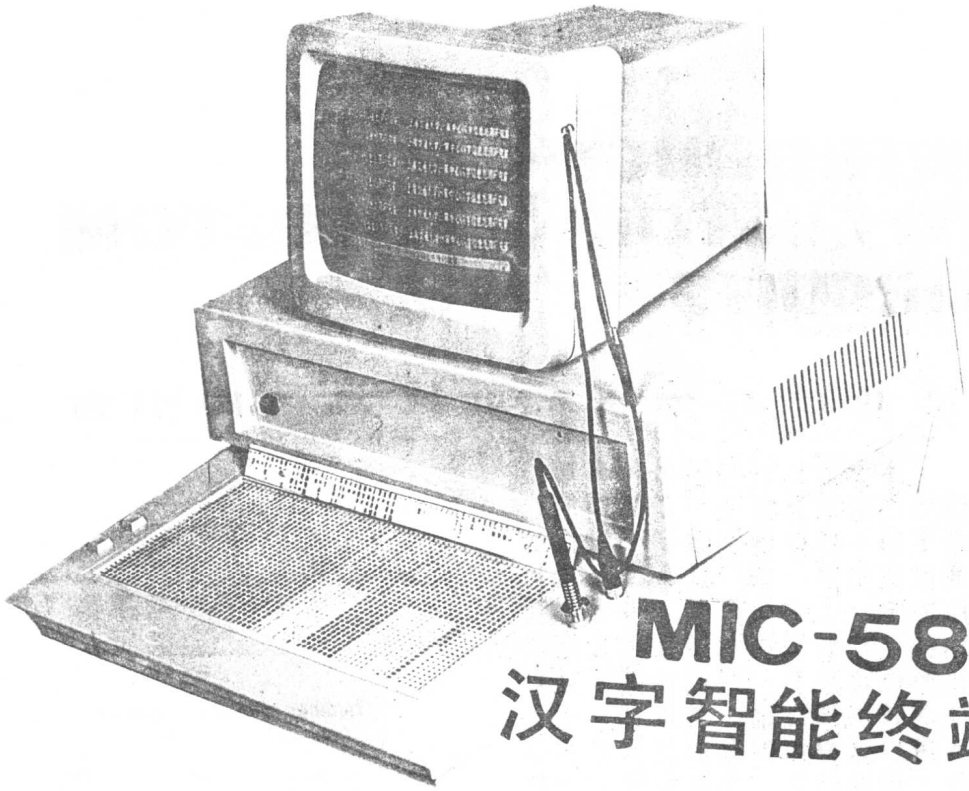
	502-505		
	524-600		
	710-799		
2	882-1000	5	3602-3700
	1566-1599		3996-4101
3	1663-1800	6	4147-4300
	2063-2099		4590-4699
	2118-2200	7	4761-4900
	2219-2299		5151-5200
	2340-2500		
	2519-2600		
	2693-2800		
	2987-3100		

二. 本书按器件产品的分类，增印了第七册《商业产品》。

三. 在本书的第七册后面附有最新出版的二份《IC大全》修订本(IC UPDATE)。



MIC-58C
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中华人民共和国国家经济委员会颁发的

“1983年优秀新产品”奖

上海交通大學

INTRODUCTION TO CUSTOM/SEMICUSTOM CIRCUITS

商业产品与半商业产品电路引言

本章节所介绍的各种公司提供的产品及其服务·产品指的是数字的、线性的和数字/线性的商品化电路·在<<IC大全>>选择指南中，公司是按其字母顺序排列的·在各公司名下面列出所提供的设计服务、产品功能、处理技术和测试性能·并且也列出了从用户处反馈回来的从系统到器件方面的信息·为其它使用者概要地提供了对商业产品电路的某些选择依据·

半商业产品门阵列，线性/数字阵列，标准元件以及可偏程序逻辑都包含在适当安排的器件制造厂商的细目中，在半商业产品部分与电路有关的特性参数为不标准的·因此在同一制造厂商的产品中，对一些参数作比较更为有用·有关制造厂商的数据资料中经常会提供某些附加的性能信息，从而帮你进行必要的选择·

Detailed Product Information provided by:

The manufacturers listed above have provided detailed information on their latest and most significant product...

EINFÜHRUNG KUNDEN-SPEZIFISCHE ICs

Deiser neue Abschnitt beschreibt Dienstleistungen und produkte von Herstellern, die digitale, lineare und kombinierte digital/lineare kundenspezifische Schaltkreise anbieten. Die Firmen werden in alphabetischer Reihenfolge genannt und anhand ihrer Fähigkeit zum Schaltkreis- Entwurf, ihrer Produktionsanlagen, Prozeβtechniken und Testmöglichkeiten beschrieben. Die verschiedenen Möglichkeiten des Anwenders im Hinblick auf dessen Angaben sind durch eine Auflistung der vom Hersteller gewünschten technischen Details erläutert. Diese können von einer Gundkonzeption bis zu einem bekannten, funktionierenden Bauelement reichen.

Die enthaltenen halb-spezifischen (semicustom) Bauteile enthalte Gatter- und Zellen-Arrays, die durch die letzte Masek zum kundenspezifischen Schaltkreis werden. Feldprogrammierbare Bauteile sind in diesem Abschnitt auch enthalten.

INTRODUCTION AUX CIRCUITS FAITS SUR COMMANDE

Nouvelle cette année, cette Section décrit les services et produits fournis par des sociétés fabriquant sur mesure des circuits digitaux, linéaires, digitaux/linéaires. Le Guide Général de Sélection offre sur plusieurs pages un tableau indiquant par fabricant les services offerts, les équipements disponibles, les systèmes technologiques, et les procédés de test utilisés. Les possibilitiés de collaboration entre le fabricant et le client sont également indiquées dans ce même tableau.

Les produits partiellement faits sur mesure comprende "portes" et "cellules de mémoire" qui sont individualisées par un procéde final d'interconnexion. Les appareils programmables à l'extérieur sont aussi considérés dans cette Section.

INTRODUCCIÓN A LOS CIRCUITOS POR PEDIDO

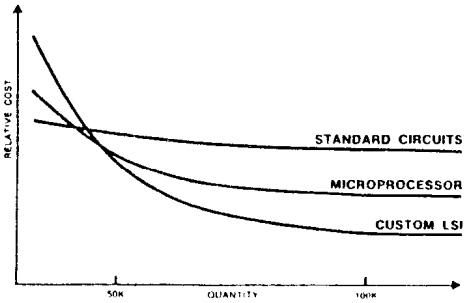
Esta sección, nueva para este año, describe servicios y productos de compañías que ofrecen circuitos por pedido, sea digital, lineal y digital/lineal combinado. Apareciendo en orden alfabético el la Guía Maestra de Selección, las compañías se caracterizan por descripciones de servicio de deseño, taller de producción, technologia de processos y capacidad de distintas pruebas. Opciones de contribución por el operador en los proyectos de circuitos por pedido, están delineados en la lista de nivel de asistencia del operador preferido por el fabricante que abarca de concepto de sistema a pieza comprobada buena.

Componentes a pedido limitado incluyen redes de puertas y celdas electrónicas que son "a pedido" en el proceso final de interconección. Componentes programables en el campo tambien están incluidos seccion.

カストムサーキットへの案内

本年新たに加わったこのセクションにはディジタル，リニア，双方兼ねたカストム回路を供給するメーカーのサーヴィスと製品を掲載しています。メーカー名はＡＢＣ順にマスターセレクションガイドにのっていますが，そのメーカー毎に，デザイン，製造設備，プロセス技術，テスト能力を示してあります。カストムサーキットに関するメーカー側のカストマー参加希望はシステムの概念から良く知られている製品の良品迄戦略を記載しています。

Options for Going Custom



Standard circuits are recommended for production volumes below 1000 units. Intermediate volume applications may benefit best from customizing through software, such as with microprocessors. Custom chips have the lowest cost at high-volume production. Source: National Semiconductor

For many applications, standard integrated circuits may be inappropriate from the standpoints of cost, size, power consumption or reliability. Moreover, unique features demanded by proprietary products often require entirely new circuit configurations. As a result, customized ICs are assuming an increasingly important role in system design.

Custom IC suppliers report that the chief benefits enjoyed by nearly all custom-circuit users are low-cost parts and cost savings resulting from reduced printed-circuit board space, parts handling, inventory, testing requirements and system maintenance. Obtaining these benefits requires careful consideration of the many options provided by both custom ICs and other approaches which ultimately effect economics.

For example, in addition to standard and custom parts, options for implementing new system designs include semicustom ICs, microcomputers, custom microcomputers, a mixture of microcomputers and custom ICs, or a mixture of all of these. The system development strategy used depends largely upon marketing objectives and may require staged system development, first with standard ICs, then with semicustom ICs and, finally, full custom units. Or, the strategy may dictate developing standard or semicustom prototype systems with concurrent verification of a full custom design.

Another option is to alter a standard microprocessor and other standard circuits, rather than using a full custom design. Customizing standard products can reduce the design costs, turnaround time and risks of a full custom design. In some cases, semicustom or custom circuits can replace microprocessors which have been used in dedicated, mostly controller-type applications. Or, a custom circuit may be a direct integration of several standard ICs, such as op-amps, comparators and resistor networks.

All approaches require up-front decisions involving design, prototype and production turnaround times, volume/cost tradeoffs, alternate sourcing, circuit configuration and process technologies, and the user/supplier interface. The most critical factor, however, is cost.

The cost of a nonstandard IC includes expenses for design and tooling, wafer and chip processing, packaging and testing.

Design and Tooling: Until recently, IC users had just two options for implementing new designs: standard parts and full custom circuits. When standard parts were inadequate, a user had to commit to great production volumes to amortize high development costs. Additionally, development times often extended well over a year, and chances of initial success were relatively slim. However, custom suppliers have minimized these drawbacks by devising new customizing techniques to the extent that few custom circuits now are developed entirely from scratch.

Full Custom: In this approach the circuit designer draws from a collection of time-tested circuit modules and components to customize a chip. These elements of known performance are located on the chip with the assistance of CAD equipment to form optimized interconnect patterns, thereby minimizing chip area and thus cost. Full custom design gives the most efficient use of silicon chip area. Although design turnaround time has been longer than other options, advanced CAD techniques are closing the gap.

Semicustom: This approach produces custom circuits by interconnecting repetetive patterns of preprocessed circuit elements on a chip called a *masterslice*. Because a masterslice is processed just short of the final interconnect pattern, the same part is mass-produced for use by all customers with customizing occuring at the final interconnect stage.

Gate arays are masterslices containing repetitive patterns of transistors connected as logic gates. *Device arrays* are patterns uncommitted transistors and resistors. The next level *of customization uses an array of unconnected transistors and* resistors called *cells*. Each cell can be interconnected internally to provide a specific logic function, and each cell on the chip interconnected into a customized system. The repertoire of allowable cell functions is called the *cell library*.

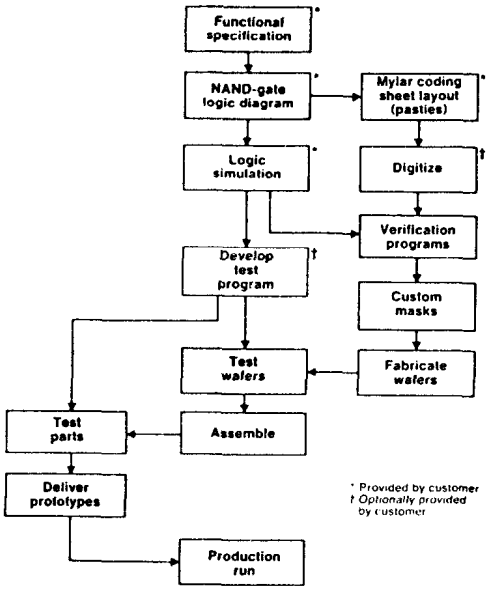
Interconnect design for masterslices can be manual or computer-aided. In all cases, the masterslice approach minimizes design turnaround time. Complex *custom-cell library circuits* can be obtained in about 18 weeks or less in prototype form; prototypes from gate arrays typically are available in about nine weeks.

One major disadvantage of masterslice circuits has been low circuit density. Circuit and device arrays require channels and alleys for routing interconnects. And because a single pattern must accommodate many different system designs, considerable interconnect routing space can be left unused after the chip is designed. Conversely, in a full custom design, unused space can be minimized. Consequently, a masterslice can be three times larger than an equivalent full-custom chip costing 20% to 60% less.

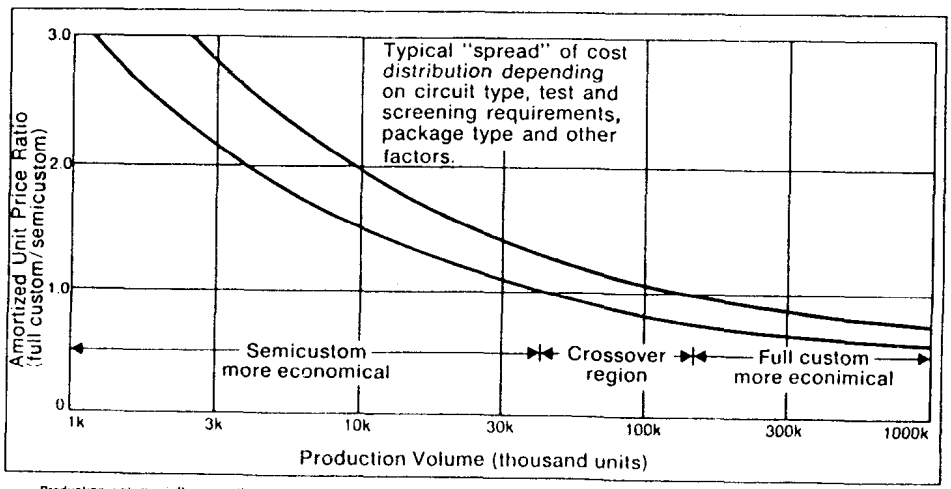
But masterslice manufacturers are increasing circuit densities to bring unit cost closer to that of full-custom circuits purchased in high volume. Circuits with two and three layers of interconnects are being developed to allow more efficient use of chip area. Triple interconnect-level masterslices are already used in a recent generation of IBM computers. So while full-custom designers are reducing design turnaround time, masterslice proponents are reducing unit cost.

Production: *IC houses that process custom circuits basically* sell a production service, not a design service. Most are concerned first with recovering design costs and then making profit on the volume production of parts. The general rule of thumb calls for total production volume representing at least ten times the supplier's design cost.

Some firms may accept a smaller production volume if engineering costs can be lowered. The customer may satisfy this requirement by using a design specialty firm or the in-house



Developing a custom IC is a multistage process. The degree of user involvement varies between companies. This diagram outlines the development of a custom chip designed from a cell library. Source: Signetics



Production volume influences the choice between full-custom and semicustom parts. However, other considerations (such as design turnaround time) may be overriding factors. Source: Eaar

engineering staff. Specialty firms provide services such as design, mask-making, assembly and testing. In many cases a design house controls the evolution of an IC through tooling, fabrication and final delivery.

Selecting a fabrication process based solely on chip cost is not entirely straightforward. For any given process, all wafers cost about the same regardless of circuit complexity. The cost of a chip is determined chiefly by yield, which tends to decrease with chip-area increase. Thus, chip cost varies directly with chip area.

Cost comparison between processes is more complex. Older processes do not necessarily produce higher yields than newer process techniques. And although processes involving more fabrication steps tend to have higher production cost per wafer, a more complex process may also allow circuit designs that produce smaller chips. Similarly, wafers fabricated by newer processes that involve expensive production equipment are usually costly. But, improved processes, although expensive, can produce high yields which tend to lower the die cost. The process must therefore be chosen to get the lowest chip cost consistent with meeting performance requirements.

Packaging: A standard package can cost from a few cents to several dollars. In many custom designs, package cost can be the largest part of unit cost, especially if a custom package is required.

Testing: This cost can be a large portion of the total unit cost. So care must be taken to design the chip for minimum testing requirements. Testing costs depend on the type of test equipment used and the amount of time required to test. Ideally the simplest and most widely available equipment should be used.

Testing cost can range from $50 per hour to several hundred dollars per hour. The manner in which tests are specified can vary test time per part from a few seconds to a minute. It is not economically feasible to test many complex digital circuits for every possible combination of inputs and outputs. And unless complex random logic is designed with testing in mind, it may not be possible to test the final product adequately.

Testing should be considered early in the design phase to minimize cost. Usually it is possible to select a process technology or circuit configuration that eliminates the need for some parametric tests. If timing requirements are critical, for example, using one of the faster process technologies or circuit configurations can eliminate testing speed parameters. Similarly, using a superior process for linear circuits could eliminate the need to test for offset voltages in op-amps.

Terminology

Assembly: Process of mounting a chip into a package and connecting the chip terminal pads to package terminals.

CAD: Computer-aided design. CAD includes computerized equipment that performs circuit simulation, logic simulation, automatic circuit and logic drawing, topological digitizing, topology construction on a CRT terminal, design rule checking and test generation.

Cell: Circuit performing a digital or linear function that is repeatedly used to design an LSI/VLSI chip.

Cell library: Collection of predesigned cell functions stored in a CAD data base. Custom LSI/VLSI devices can be designed by choosing appropriate cells from the library and locating them on a chip to minimize interconnects and maximize performance. The cells are computer characterized for performance much like SSI and MSI ICs with data sheets for each cell.

Custom circuit: In general, a component whose manufacture is under the exclusive control of a customer. The term can refer to full-custom, customized-standard or semicustom parts. In semicustom parts most of the mask layers are common to many customers, and only the final interconnect patterns are special. A customized part is a modification of a standard part to the requirements of a customer. Full-custom parts normally are fabricated from masks configured for the customer.

Design rules: Collection of rules that define minimum dimensions of device topological structures. Design rules also express process-parameter design limits such as gain factor, threshold level, oxide thickness and capacitance.

Die: Rectangular piece of semiconductor material into which electrical circuits have been fabricated. Also called a chip. Plural is dice.

Digitized data base: Recorded digital data representing a topological drawing of an SSI, MSI, LSI or VLSI device. The data include locations and dimensions of rectangles that make up individual circuit elements and interconnects.

Feature size: Dimensions of rectangles, lines and spacings in in an IC topological design.

Gate: Basic digital-logic element producing a binary output depending on the logic state of various inputs.

Gate array: Regular pattern of circuit components on a chip, connected to form regular patterns of gates. The gates are not interconnected until the customer specifies the chip function.

Gate equivalent: Basic unit of measure for digital circuit complexity based on the number of elementary logic gates needed to provide the same circuit function.

LSI: Large-scale integration. Device design integrating from 100 up to thousands of gate equivalents on a chip.

Macrocell array: Regular pattern of grouped, unconnected circuit components. Macrocells are formed into standard logic elements by interconnecting the components to provide specific circuit functions. Interconnects between the cells are specified to perform a specific chip function. The formation of the cell functions and cell interconnects are unique to the customer.

MSI: Medium-scale integration. Device design integrating from 10 to 100 gate equivalents on a chip.

Masterslice: In general, a partially processed chip containing circuit elements for customizing through final metal interconnect patterns. Can refer to gate, device or cell arrays.

Pastie: Scaled decal (usually transparent) representing both function and dimensions of an IC building block such as a gate, flip-flop or I/O buffer. Pasties are a commonly used tool for designing LSI/VLSI chips from a cell library. Each cell type has pastie equivalents.

SSI: Small-scale integration. ICs containing fewer than ten logic-gate equivalents.

Silicon gate: MOS design in which the gate is made of silicon instead of metal. Silicon gate MOS is faster and more dense than metal-gate MOS.

VLSI: Very-large-scale integration. Device design integrating thousands of gate equivalents on a chip.

Cost: Intense activity in both gate arrays and associated development tools should make the gate-array concept extremely cost competitive with other design approaches. Typical costs for the development of a gate array and a full-custom IC are shown in the accompanying tables.

New gate arrays are currently in widespread development by IC manufacturers; CMOS products with up to 8,000 gates and emitter-coupled-logic (ECL) devices with 100-picosecond gate delays have already been developed. Although most of the attention has been concentrated on CMOS, many bipolar technologies are not being neglected.

Gate arrays are available in a number of bipolar technologies including ECL, Schottky TTL, integrated injection logic, integrated Schottky logic (ISL), and Schottky transistor logic (STL). Gate delays for these devices can be as low as 0.8 nanoseconds. Gate array chips are also available in NMOS and combination CMOS/NMOS versions.

Availability of computer-aided-design (CAD) tools and software support are helping both semicustom and custom products gain acceptance. In some cases, IC suppliers permit customers to use the supplier's in-house CAD facilities. Training courses, running three to five days, are also being offered by many IC manufacturers.

Custom IC cost factors.

Before Process Assembly

- Orders: Issues & Tracking
- Specific Documentation
- Orders: Issues & Tracking
- Purchase Prices
- Cost of Capital
- Inventory: Storage Space/Handling
- Incoming Inspection
- PC Board Space
- Power Consumption

After PC Assembly

- Test: Board
- Failure Diagnostic
- Test Active/Passive Components
- Repair
- Re-Test
- Re-Inventory

Typical costs for the development of a 1000-gate array.

	min.	max.
1. Tooling Development		
A) Circuit Conversion	$500	$1500
B) Layout	$2.5K	$5K
C) Digitization, PG Tape, Masks, 20 prototype units in ceramic DIP, bench tested	$9K	$13K
2. Preproduction		
A) Test Program Development	$4K	$8K
B) Test hardware		
Personality Board	$1K	$2K
Probe Card	$100	$200
Special Supplies, Signal Generator	*	*
Burn-In Board	$500	$2500
Other	*	*
C) Production Qualification Units (Optional)		
Burned-In, Temperature Tested 100 units	3K	$6K
883B Environmental Screening	Extra	
TOTAL	$18K	$40K

* Depends on application

Typical development costs for a full-custom integrated circuit.

		min.	max.
1. Tooling Development			
A) Circuit to LSI Conversion			
B) Layout			
C) Digitization, PG Tape, Masks		$20K	$200K
2. Engineering Evaluations: 5 wafers			
Working Plates	Per Plate	$50	$100
Bipolar: 1-Layer Metal	4-6 weeks	$3K	$6K
2-Layer Metal	6-8 weeks	$5K	$10K
Pt Schottky Diodes - week extra			
CMOS: 1 Poly, 1 Metal	6-8 weeks	$3K	$5K
Same, 4 Micron	6-8 weeks	$4K	$6K
May need several iterations, usually 2 to 4			
3. Prototypes			
A) Establish Waferbank			
30-45 Wafers from Several Runs		$10K	$30K
B) First Look Samples			
100 Untested Dice Packaged in Ceramic Sidebraze		$600	$1500
C) Test Program Development		$5K	$30K
D) Test Hardware			
Personality Board		$1K	$2K
Probe Card		$100	$200
Special Supplies, Signal Generators		*	*
Burn-In Board		$500	$2500
Other		*	*
E) Production Qualification Units (if desired)			
Burned-In, Temperature Tested 100 Units		$3K	$6K
883B Environmental Screening		Extra	
TOTAL		$40K	$280K

* Depends on application

Comparison. The relative ranking of risk factors for alternative design approaches is shown at the right. These ratings will vary depending on the selected suppliers for custom, cell library, gate array or non-LSI devices. Therefore, this chart should be used only as a guide. In the case of linear designs, risks are greater than for digital counterparts. Unless the various circuit blocks assembled from a cell library are compatible with each other from the standpoint of processing, the overall performance of the chip can be less than expected. For instance, the breakdown voltage, beta, sheet resistance, implant dosage, and epi thickness requirements, to say nothing of the starting material, may be mutually exclusive. Also, NPN and PNP transistor configurations cannot both be optimized for performance as is possible with discrete devices.

Comparisons of advantages of various design approaches. A rating of 1 indicates best. (Numbers in parenthesis apply to linear designs.)

	Full Custom	Cell Library	Gate Array	Non-LSI
Design Costs	4(3)	3(4)	2	1
Design Time	4(3)	2(4)	3(2)	1
Mask Costs	4	4	2	1
Redesign Flexibility	4	3	2	1
Test Program Costs	3	3	2	1
Circuit Purchase Price	1	2	3	4
System Power Required	1	2	2	4
Reliability	1	2	2	4
PC Board & Costs	1	2	2	4
Production Labor	1	2	2	4
Security	1	3	2	4
Added Features/ Board	1	3	3	4

CUSTOM CONSIDERATIONS

Benefits provided by custom, related to cost factors, are described in the following paragraphs:

Specification Documentation: Since a single custom IC can replace as many as 100 MSI circuits (plus assorted external active and passive components, such as decoupling capacitors, diodes, and transistors), paperwork needed is greatly reduced.

Purchasing: The purchasing function is not a "free" activity in any company. It costs money to issue purchase orders, and to track them through various delivery dates and procedures with phone calls and computer time. The lower parts count significantly reduce this paper load.

Purchase Price: Depending on the complexity of the chip, the price for a custom device can be lower, at, or above that of all the components to be replaced. It is important to count all of the passive peripheral components involved, such as sockets, resistors, capacitors, inductors, and perhaps even connector pins to the outside.

Cost of Capital: This cost varies with prevailing interest rate. If a company has to borrow development money, usually at about three or four percent over prime rate, then this interest is also an expense incurred by the project. But even if cash is available, there still may be an opportunity cost. This is the income that could have been earned if the cash had been used on short-term projects (such as buying more inventory — provided the sales to turn the inventory over exists).

Inventory: Once the material is in the plant, it has to be handled (including counting, sorting, and paperwork), and stored. Usually, storage space is predefined, and, since it already exists, it is not considered to be an additional expense. However, one has to remember that real estate value on a per-footage basis is substantial and that other departments might make a more cost effective use of any space available. Hence, an additional cost is incurred for each additional component that has to be stored and accounted for. Also, components may become obsolete before the inventory is used up. Custom ICs contribute to decreasing inventory expenses.

Incoming Inspection: Unless pre-aged and pre-screened components are bought to prevent early failures (infant mortality), it is advantageous to inspect active components as they come in. Again, a reduction in the number and variety of devices to be tested adds to profits.

Printed Circuit Board Space: Fewer components mean less space needed to mount them, less auxiliary components, less artwork for interconnect lines, fewer holes to be drilled, and less insertion time and effort — as well as a smaller board.

Power Consumption: The power consumption of the entire system is usually dramatically reduced, making savings possible with lowered power supply and cooling requirements.

MASTER SELECTION GUIDE

CUSTOM/SEMICUSTOM

Manufacturer	Advanced Micro Devices	Alphatron	AMCC
FOR DETAILED DATA SEE:	(Page 4901)		(Page 4907)
Customized Standard Circuits			
Gate Array	Programmable Array Logic		ECL, TTL, Mixed
Chip Density Range (equiv. gates)	200 to 800	Up to 4400 2-input gates	250 to 3500 gates
Cell Library		CMOS	ECL, TTL, Mixed
Design Kit Available	Yes	Yes	Yes
Full Custom Circuits Digital		Silicon- or metal-gate PMOS, NMOS, CMOS	ECL, TTL, Mixed
Linear		Silicon- or metal-gate PMOS, NMOS, CMOS	
Combined Digital/Linear		Silicon- or metal-gate PMOS, NMOS, CMOS	
Provide Design Assistance	Yes	Yes	Yes
Acceptable Customer Input (in order of preference)		Alphamap layout logic diagram functional description block diagram.	Functional specification, logic diagram, test vectors, PG Tape, Tegas Tape.
Design Aids	AMPALASM-20 software for Boolean equation generation. AMPLPL software provides similar capability for advanced products.	Logic simulation, breadboard assistance, design rule checks, decals.	Logic simulation, timing verification, design rule checks, electrical rule checks, portable library on EWS, auto place, auto route, training session, design center.
Production	In-house	Wafer production procured from outside foundries. Testing done in-house.	In-house
Preferred Delivered Product	Ceramic and plastic DIPs, leadless chip carriers, dice; all available in commercial and military.	Any upon request	Packaged devices
Test Program Generation		Yes	Yes
Production Test	100% dc, ac and functional testing. Burn-in, thermal shock, environmental, MIL.	Functional, parametric, burn-in, thermal shock, environmental, MIL.	Functional, parametric, AC, burn-in, thermal shock, envornmental, MIL-STD-883.
Electrical Test Systems Available	Xincom, Accutest	In-house designed, customer-supplied, or outside service.	Sentry VIII, Sentry XXI
Comments	Commercial programmers available Software output JEDEC PLDTF. Most complex programmable logic parts available.	Multiple sourcing. Cell library and design rule handbook.	Mixed I/O (ECL/TTL) capability. ECL 10K & 100K or both capability. MSI and custom macros available. Second sourced.