APPLICATIONS OF LINEAR INTEGRATED CIRCUITS

By Eugene R. Hnatek

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EUGENE R. HNATEK

DCA Reliability Laboratory Inc.

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Preface

The purpose of this book is to provide applications-oriented information and ideas for linear ICs. The first sections of each chapter will present the reader with general characteristics of various devices including a definition of specifications and their application significance. This is followed by a collection of applications. In many cases these applications show the use of specific IC types. The same basic design considerations, however, apply to any IC of the same general characteristics.

To give more insight into device properties, the first two chapters consist of general information dealing with processes, components, and design principles. This background information will give the user a better understanding of linear IC operation and more specifically will help the user anticipate the result of any nonspecific operating situation in which they might be used. Such a situation is more likely in linear ICs than in other IC forms since a much wider range of functions and operating environments is encountered.

Until recent years, linear ICs have been restricted mostly to building block devices, that is, devices that can be used in a wide variety of functions with the addition of external discrete components. During this period, the typical devices available were operational amplifiers, video amplifiers, comparators, differential amplifiers, etc. The number of devices designed for a specific end use were comparatively few. The last few years have seen a large expansion in the range and performance of linear IC components while current pricing gives them the economic edge over discrete designs. This is shown significantly by the penetration linear ICs are making into new and varied designs such as timers, phase-locked loops, preamplifiers, etc.

This trend will accelerate as the penetration of linear ICs expands into wider markets. New technologies will give an increased range of components so that almost any function feasible in discretes will be possible in monolithic form. The general exception will be when fundamental physical limitations, such as power dissipation, prevail. Outside such physical limitations, the use of ICs in linear functions will become predominant.

A wide variety of functional linear ICs have been developed to provide a powerful array of components for analog circuit design. This book is dedicated to providing

application ideas and basic principles which when clearly understood can lead to successful, reliable, and practical circuit designs.

I should like to thank my friends at National Semiconductor Corporation, especially Charles Signor, for permission to use portions of their applications literature. Additionally, I should like to thank my two typists for their painstaking hours in preparing this manuscript—my mother, Mrs. Vlasta Hnatek, and my sister-in-law, Mrs. Robert Banks. Finally, I would like to thank my editor, George Novotny, for his time and Alan Boston and Angelo Pestarino for their encouragement during the preparation of this manuscript. A special thanks also goes to Mike Economy.

Although every effort has been made to provide meaningful applications information, the author will assume no responsibility for the use of the circuits described herein and make no representation as to freedom of patent infringement.

San Jose, California *Eugene R. Hnatek*

Contents

Chapter 1

Linear Integrated Circuit Technology

MATERIALS PROCESSING

The first step in making an IC is to design a circuit which can be integrated by using a set of rules, some of which are described in Chapter 2. Masks are then created which represent the patterns of various layers of material to be diffused. The next step is to "grow" a cylinder of silicon. Various diameters of this cylinder are currently used, but in general the range is between 2 and 3 in. Wafers 10 mils thick are then cut from the cylinder as seen in Figure 1-1.

Since each wafer can contain 250 or more circuits, the surface must be highly uniform. To accomplish the uniformity required, the wafers are polished to produce a mirror-smooth surface. Molecular structure of the surface material as well as other surface characteristics are important to circuit performance. This requirement is satisfied by growing additional semiconductor material, an oxide, on the top surface of the wafer by a method known as *epitaxy*.

A coating of photographic emulsion, called photoresist, is now put onto the wafer. The mask which corresponds to the first layer of material to be diffused is placed in an optical jig along with the wafer. An ultraviolet (uv) light passing through the mask forms a photographic image of the mask on the wafer. Portions of the photoresist exposed to the light polymerize. The wafer is then developed and washed in a way similar to photographic film. Emulsion that is not polymerized becomes dissolved in the developing process. The remaining polymerized emulsion forms a protection against diffusion.

The wafers are then placed into a diffusion furnace and under the conditions of temperature (900°C) and time (1 to 6 hr) certain materials such as phosphorus, arsenic, or boron are diffused into the exposed patterned areas in order to achieve the desired electrical characteristics. Temperature, time, amount and type of diffusants, depth of diffusion, and rate of diffusion are all critical factors. Temperatures in the furnace, for example, are controlled to better than ± 0.5°C.

Figure 1-1. Individual wafers after cutting and polishing.

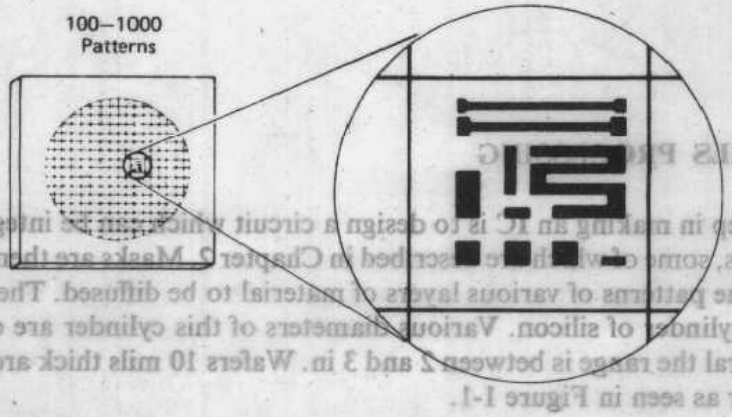

Figure 1-2. More than 250 identical circuits are processed on a single wafer.

Figure 1-3. A typical diffusion furnace.

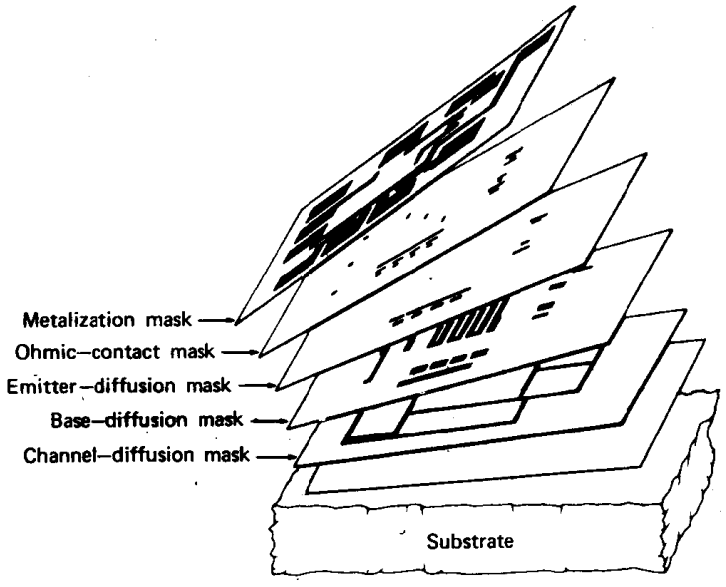

Figure 1-4. The series of overlaying masks used in integrated circuit processing.

These three basic steps,

1. Exposure to light through a mask
2. Development
3. Diffusion

are repeated using different masks resulting in an IC which consists of a series of overlaying patterns, Figure 1-4. A "metal mask" is the final pattern. It serves as the interconnecting links between the individual components on the chip. Figure 1-5 graphically illustrates the major steps in the processing of an IC.

Once the above processes have been completed, each circuit on the wafer is tested under computer control and circuits which fail the test are marked. The wafer is then cut into individual "die" or "chips."

The final major step before testing and shipment is packaging. A variety of package types is available all of which provide three principal characteristics:

1. Protection of the die from a hostile ambient environment such as mechanical abuse, dust, and corrosive elements
2. Thermal dissipation of heat generated during operation
3. A convenient means for electrically connecting the chip to an external circuit

LINEAR PROCESSES

Integrated circuits are divided into three general categories: (1) Linear, (2) digital, and (3) metal oxide semiconductor (MOS). Distinctly different design and process techniques are used for each type. The main difference between linear processes and other IC processes is their diversity. While digital circuits are commonly restricted to low-voltage switching, linear circuits may be fabricated with anything from switching to linear characteristics, high or low voltages, high or low frequency, or

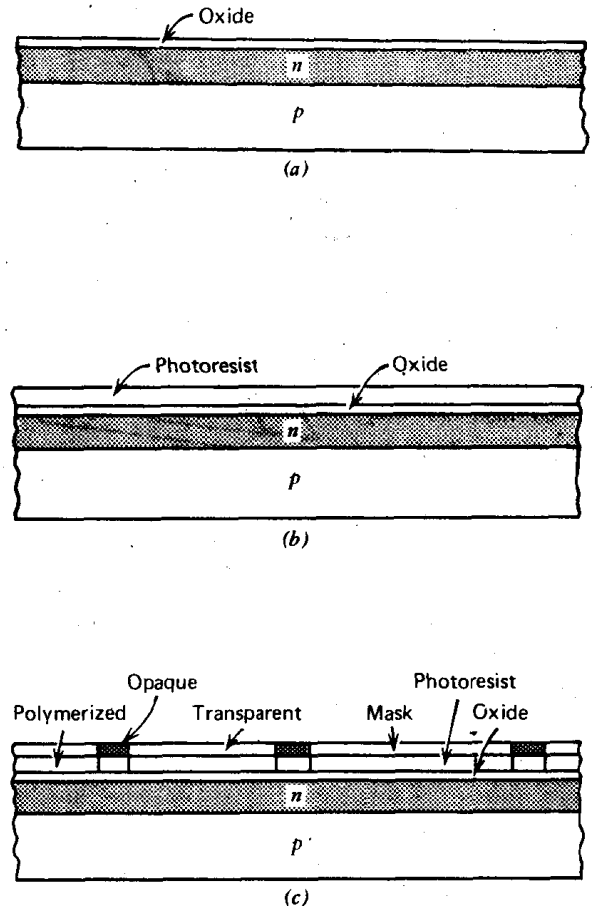

Figure 1-5. Major integrated circuit processing steps: (*a*) Starting material is a slice of *p*-type silicon, between 2 and 3 in. in diameter and a few mils thick. In an epitaxial reactor, a thin layer of *n*-type silicon is grown on the slice. Then an oxide layer is grown. (*b*) The entire top surface is covered with a layer of photoresist. (*c*) The mask containing the isolation pattern is placed on top, and the photoresist is exposed to uv light. The portions of the photoresist exposed to the light polymerize; the rest can be dissolved. (*d*) The oxide that is not protected by the polymerized photoresist is etched away. (*e*) The *p*-type dopant is diffused through the windows. The diffused regions connect with the underlying *p* region (the substrate) and form isolation pockets in the epitaxial layer. The edge of the junction is under the oxide. (*f*) The diffusion windows are closed with a new oxide layer, and the slice is again covered with photoresist. (*g*) The photoresist is exposed through the mask which outlines all shallow *p* regions, and the oxide is again etched away in the unexposed areas. (*h*) The *p*-type dopant is diffused into the unprotected regions, and the slice is covered with another oxide layer. (*i*) Again the slice is covered with photoresist. The resist is exposed through the mask, which outlines all shallow *n* regions, and the oxide is etched away in the unpolymerized areas. (*j*) A shallow layer of high *n*-type dopant concentration is diffused into the unprotected areas. (*k*) Another oxide layer is grown. (*l*) The slice is covered with photoresist for the fourth time. The resist is exposed through a mask in the areas where contact to the devices must be made, and the unprotected oxide is removed. (*m*) The entire slice is covered with a thin metal film. (*n*) With one more series of photolithographic steps, the portions of the metal layer not needed for interconnection are removed.

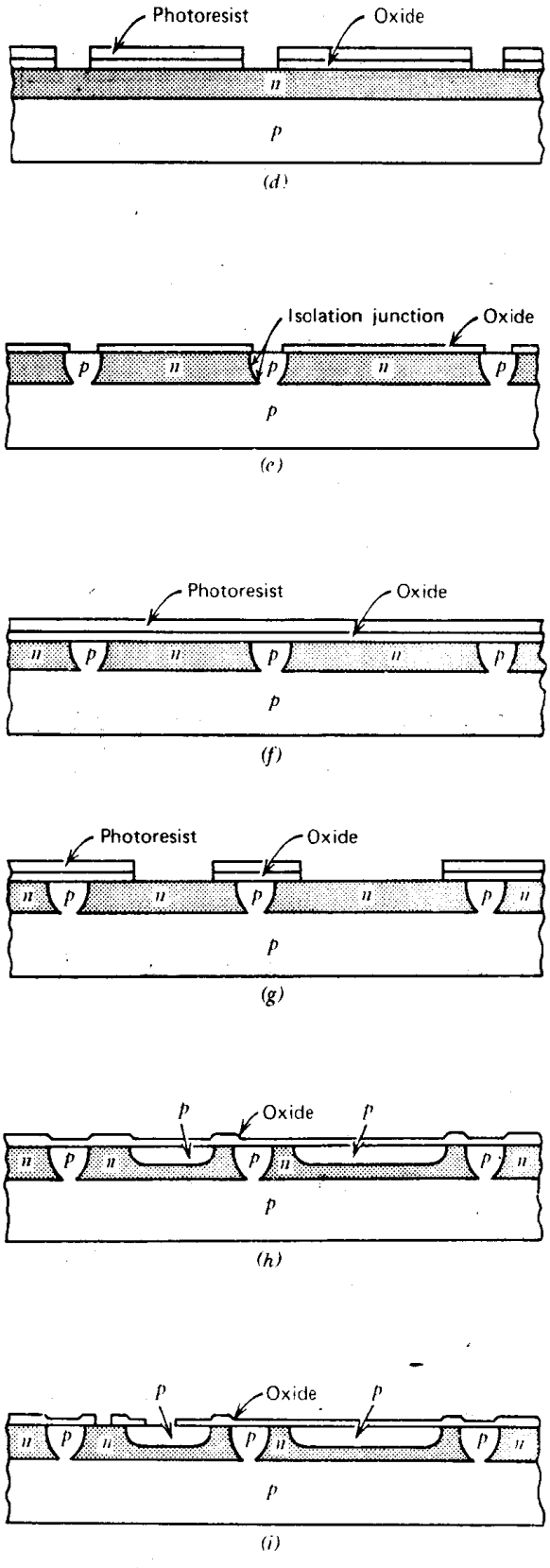

Figure 1-5. *Continued*

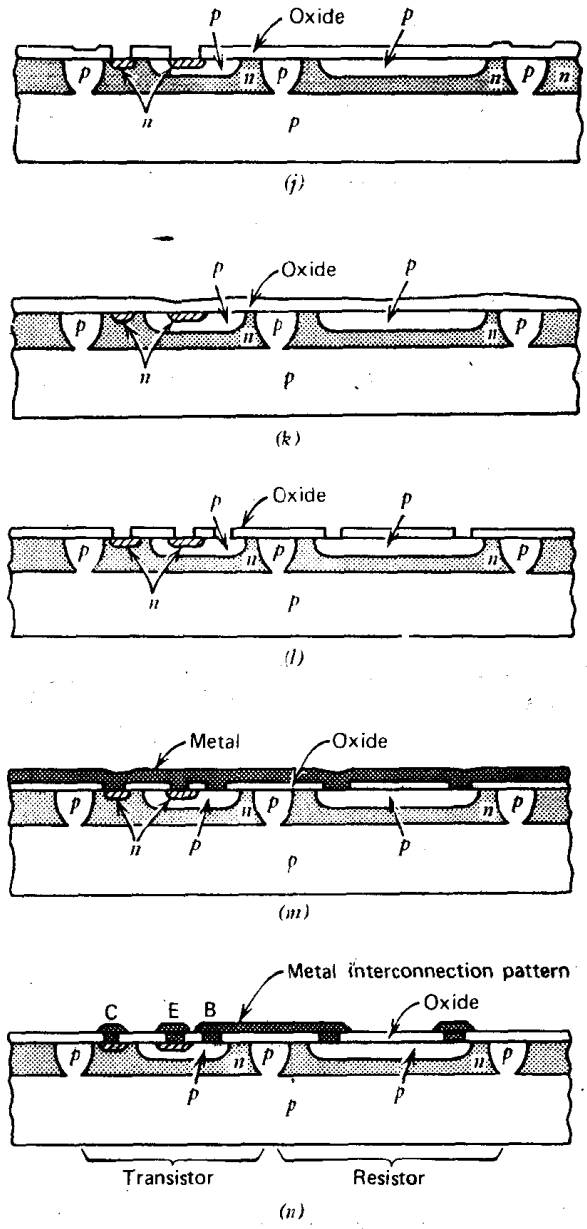

Figure 1-5. *Continued*

any combination of these properties. To cope with this range of applications, the following processes are frequently used:

Epitaxial	0.25 Ω-cm gold-doped and nongold-doped
	0.5 Ω-cm gold-doped
	1.0 Ω-cm Schottky and nonSchottky
	2.5 Ω-cm
	5.0 Ω-cm
Dielectric	2 to 15 Ω-cm

All epitaxial processes are similar. The main difference is the resistivity of the deposited epitaxial layer in which the components are formed. This difference

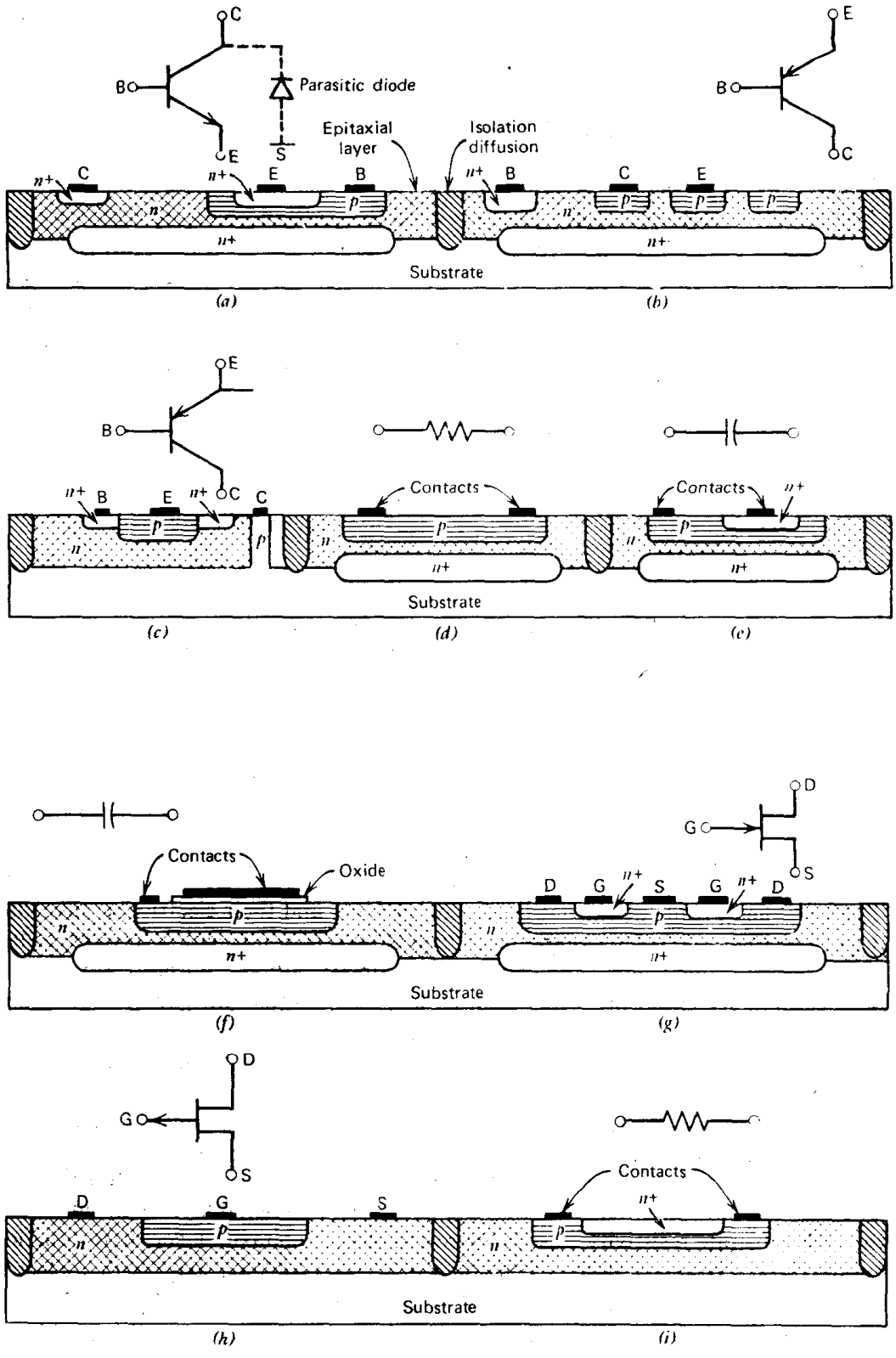

Figure 1-6. (*a*) An *npn* transistor, (*b*) a lateral *pnp* transistor, (*c*) a vertical *pnp* transistor, (*d*) a base resistor, (*e*) a junction capacitor, (*f*) an oxide capacitor, (*g*) a *p*-channel J FET, (*h*) an *n*-channel J FET, and (*i*) a pinch resistor.

allows for higher voltage breakdowns, lower saturation voltages, etc. For instance, the 5 Ω-cm process is used for operational amplifiers and regulators because it gives the 50 V LV_{CEO} (latch-up voltage, collector-to-emitter, with the base open) transistor breakdowns required. Since the phase-lock loops need only 20 V, the 2.5 Ω-cm process is adequate. Also, the saturation voltages are lower than for the 5.0 Ω-cm process.

Transistor breakdown is not the only consideration in choosing a process. In products where fast switching is required, either the gold-doped or Schottky processes are used. Gold-doping is used where medium- and high-current operation is involved. Schottky technology is desired where lower currents or higher transistor breakdowns

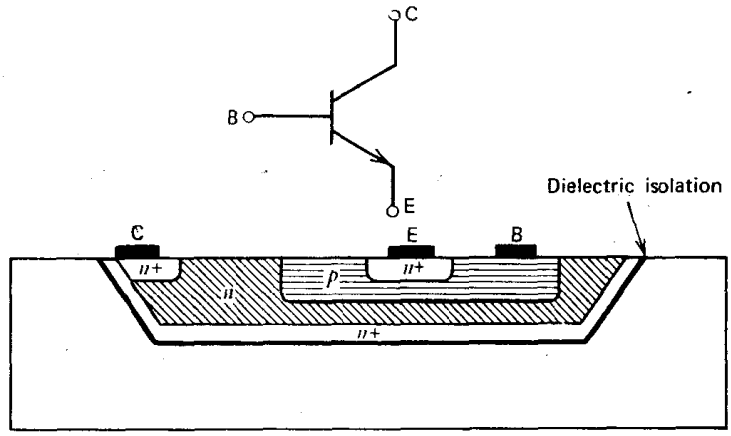

Figure 1-7. Sidewall *npn* transistor using dielectric isolation process.

are needed. As explained in detail later, the dielectric process is used where *npn* transistor breakdowns over 50 V are required.

A simplified profile of various linear components and their electrical equivalents is given in Figure 1-6. The components formed by junction isolation have parasitics associated with them such as the collector to substrate diode in Figure 1-6*a*. These can occasionally cause problems such as fault conditions and parasitic coupling. Dielectric isolation eliminates some of these parasitics. The capacitive elements remain although they can be reduced to a lower value. The profile of a typical *npn* transistor using dielectric isolation is shown in Figure 1-7.

The most important feature of dielectric isolation is the ability to make high-voltage devices. This is possible because the resistivity of the *n*-type region is not restricted to a maximum of about 5 Ω-cm as in junction isolation. Resistivity of junction isolation is limited because a highly resistive epitaxial layer is incompatible with the substrate resistivity. Also, the growth of such epitaxial layers in production quantities is extremely difficult. Neither of these problems exist with dielectric isolation. Collector resistivities of up to 15 Ω-cm are possible. Breakdowns become essentially surface-limited and are comparable to those seen with discrete planar transistor values.

Unless costly extra processing is used, the vertical *pnp* and the *n*-channel FET which are used in junction isolation are not available in dielectric processing. The loss of the vertical *pnp* is serious. Though its use is restricted to the emitter-follower

configuration, it has the advantages of good frequency response and good high-current beta. The *n*-channel field-effect transistor (FET) is used primarily in biasing circuits where it can be arranged to supply the bias circuit starting current. The circuit parameters can then be made independent of supply voltages.

LINEAR INTEGRATED CIRCUIT COMPONENTS

Transistors

It is instructive to compare, in a general manner, discrete transistors with those manufactured in ICs. The most important differences for *npn* transistors are the parasitic substrate diode (transistor) and the top contact collector, as seen in Figure 1-8.

The magnitude of the parasitic *pnp* beta depends upon the process and geometry used, but it ranges from about five for high-resistivity processes to very much less than one for gold-doped processes. The parasitic *pnp* only becomes active when the *npn* transistor goes into saturation. Normally such effects are not important, but in some circuit configurations latching effects may be observed. That is, a positive feedback path may be established which is self-sustaining. Alternatively, or perhaps coincidently, this path may cause high currents to flow. These potential problems are easily avoided with judicious layout procedures. The effect of the top contact is to increase the saturation resistance. In small signal devices this is not really significant, but at higher currents (around 500 mA) this becomes an economic factor as the die area must be increased and yields drop.

At the expense of some extra processing, *npn* transistors with very high beta may be made. The processing steps used are the same as for the regular *npn* but the emitter is diffused longer to give a very narrow base width. If regular beta *npn*s are made at the same time, complications in the masking sequence occur.

The *pnp* transistors available, both lateral and vertical, are different than discrete *pnp*s. The names *lateral* and *vertical* are derived from the mode of transistor action that occurs in the two components. Referring to Figures 1-6*b* and 1-6*c*, it can be seen that in the lateral *pnp* current flows laterally from emitter to collector through

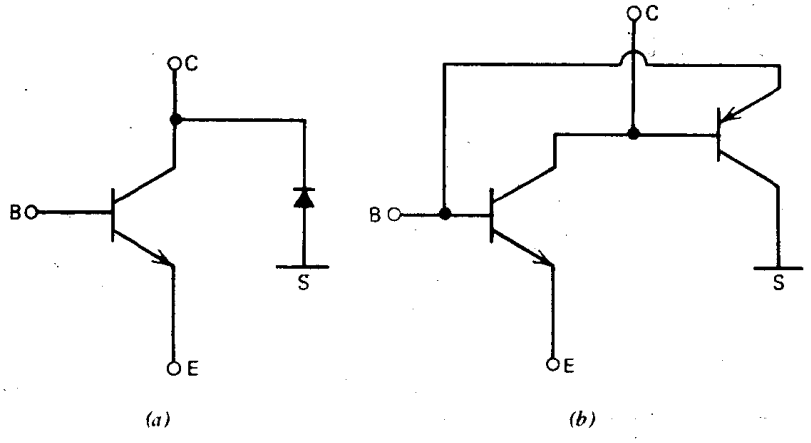

Figure 1-8. *npn* transistor parasitics shown as (*a*) diode and (*b*) *pnp* transistor.

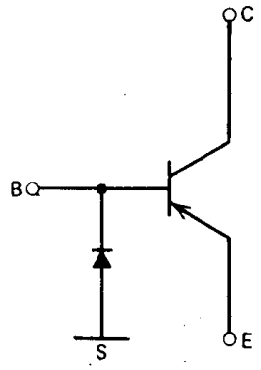

Figure 1-9. Lateral *pnp* transistor parasitic diode.

the *n*-epitaxial region. The presence of the buried-layer diffusion reduces to a comparatively low-level collection by the isolation area. It is not eliminated entirely, however, which gives rise to the parasitic diode shown in Figure 1-9. The vertical *pnp* is similarly constructed but in this case the buried-layer diffusion is omitted resulting in isolation diffusion acting as the collector.

Frequency response is the primary difference between these devices. The lateral *pnp* is restricted to frequencies below 1 to 2 MHz while the vertical *pnp* upper range is around 10 to 20 MHz. Another important feature of the lateral *pnp* is its comparatively low beta range and the low current at which beta peaks. In addition, the lateral *pnp* collector can be split to give multiple collector devices as shown in Figure 1-10. This configuration can also be used to give fairly precise values of beta by tying one of the collectors to the base.

Recent process development allows the addition of Schottky barrier devices to monolithic design (Figure 1-11). The advantage is very fast-switching circuits without gold-doping. With this technique, the properties of nongold-doped devices can be maintained while switching speeds are greatly improved. This is very desirable in devices containing analog and digital circuitry such as voltage comparators.

Resistors

Resistors can be made from any of the *n*- or *p*-type layers. In practice the base and emitter diffusions are generally used. At times the "epilayer" in the dielectric isolation process (the bulk material) is also used.

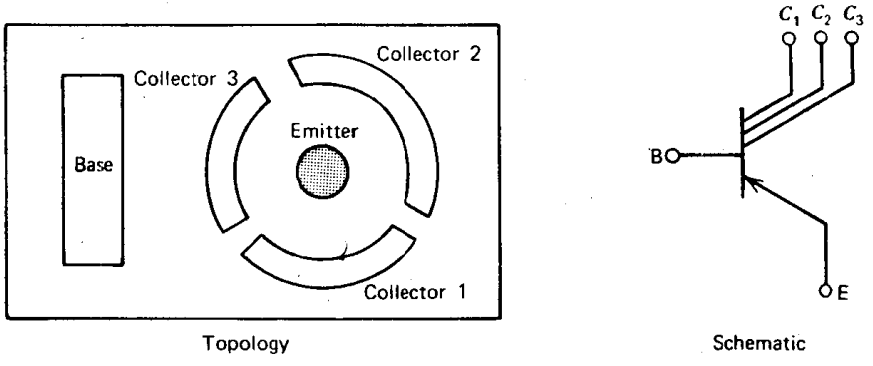

Figure 1-10. Multiple collector lateral *pnp*.