

Testability of Electronic Circuits



Testability of Electronic Circuits

Manfred Weyerer and Gerald Goldemund

Translated by Klaus Selke



Carl Hanser Verlag



Prentice Hall

First published in German 1988 by
Carl Hanser Verlag, Munich, under the title
*Prüfbarkeit elektronischer Schaltungen: Grundlagen,
Verknüpfung und Anwendung von CAD und CAT*
by Manfred Weyerer and Gerald Goldemund

This edition first published in English 1992 by
Carl Hanser Verlag, Munich, and
Prentice Hall International (UK) Ltd
66 Wood Lane End, Hemel Hempstead
Hertfordshire HP2 4RP

© Carl Hanser Verlag, 1988, 1992

All rights reserved. No part of this publication may be
reproduced, stored in a retrieval system, or transmitted,
in any form, or by any means, electronic, mechanical,
photocopying, recording or otherwise, without prior
permission, in writing, from the publisher.
For permission within the United States of America
contact Prentice Hall Inc., Englewood Cliffs, NJ 07632.

Typeset in 10 $\frac{1}{2}$ pt Times
by MHL Typesetting Ltd, Coventry

Printed and bound in Great Britain by
Dotesios Ltd, Trowbridge, Wiltshire.

Library of Congress Cataloging-in-Publication Data

Weyerer, Manfred.

[*Prüfbarkeit elektronischer Schaltungen*. English]

Testability of electronic circuits / Manfred Weyerer and Gerald
Goldemund; translated by Klaus Selke.
p. cm.

Translation of: *Prüfbarkeit elektronischer Schaltungen*.

Includes bibliographical references and index.

ISBN 0-13-911801-2: \$32.00

1. Electronic circuits — Testing. 2. Digital electronics — Testing.
3. Electronic circuit design. I. Goldemund, Gerald. II. Title.

TK7868.D5W4313 1992

621.381'5 — dc20

92-23385
CIP

British Library Cataloguing in Publication Data

Weyerer, Manfred

Testability of electronic circuits.

I. Title II. Goldemund, Gerald
621.3815

ISBN 0-13-911801-2

Foreword

It is with pleasure that I introduce this book to you, for the importance of testability in future designs cannot be overstressed. Indeed, the most technically elegant design, from a functional viewpoint, is absolutely useless if its functionality cannot be verified in a high-quality, timely and profitable manner.

Manfred and Gerald, in this translation of their original German language book, have not only covered many of the essential testability guidelines previously published in my books, but have also added valuable information on failure types and causes, logic simulation, and the linking of the design environment to manufacturing, test and repair activities via electronic networks.

This book is an excellent text for both the novice in testability design and the electronic design engineer of any skill or experience level. It is my hope that circuit designers in particular will take the information in this book not only to heart but to their workstations. For it is the designer who must implement the guidelines contained herein if new products are to be brought to market more quickly and manufactured more competitively in an increasingly global marketplace.

Testing electronic circuits in the face of ever increasing complexity is becoming more and more difficult. The only viable solution to this expensive problem is the implementation of as many as possible of the techniques described in this book. For without including the three basic testability attributes — partitioning, control and visibility — we may find that we have been so clever in designing new products that we can never verify their performance to a quality level that will allow us profitably to ship them to customers.

Jon Turino
Campbell, CA

List of Abbreviations

A/D	Analog/Digital
ADC	Analog/Digital Converter
ALU	Arithmetic Logic Unit
ANSI	American National Standards Institute
ARINC	Aeronautical Radio Inc.
ASCII	American Standard Code for Information Interchange
ASIC	Application Specific Integrated Circuit
ATE	Automatic Test Equipment
ATLAS	Abbreviated Test Language for All Systems
ATPG	Automatic Test Program Generator
BILBO	Built-In Logic Block Observation
BIT	Built-In Test
BITE	Built-In Test Equipment
BSC	Binary Synchronous Communication
C	Capacity
CAD	Computer-Aided Design
CADIF	CAD Independent Format
CAE	Computer-Aided Engineering
CAM	Computer-Aided Manufacturing
CAP	Computer-Aided Planning
CAQ	Computer-Aided Quality Assurance
CAR	Computer-Aided Repair
CAT	Computer-Aided Testing
CATV	Common Antenna Television, Cable TV
CAX	All Computer-Aided Applications
CCITT	Comité Consultatif International de Télégraphie et Téléphonie
CEPT	Committee of European Post and Telecommunications
CIM	Computer-Integrated Manufacturing

CMOS	Metal Oxide Semiconductor (Complementary)
CPU	Central Processing Unit
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
D/A	Digital/Analog
DAC	Digital/Analog Converter
DFT	Design For Testability
DIL	Dual-In-Line
DIN	Deutsche Industrie-Norm
DIS	Draft International Standard
EBCDIC	Expanded Binary Coded Decimal Interchange Code
ECL	Emitter Coupled Logic
EDIF	Electronic Design Interchange Format
EGC	Equivalent Gate Count
EPBX	Electronic Private Branch Exchange
ESPRIT	European Strategic Programme for Research and Development in Information Technology
FET	Field-Effect Transistor
FF	Flip-Flop
FOF	Factory of the Future
FTAM	File Transfer, Access and Management
GKS	Graphic Kernel System
HDLC	High-level Data Link Control
HI	High
IC	Integrated Circuit
ICS	Inhouse Communication Systems
IEC	International Electrotechnical Commission
IEEE	Institution of Electrical and Electronic Engineers
IGES	Initial Graphics Exchange Specification
ISDN	Integrated Service Digital Network
ISO	International Standardization Organization
L	Inductance
LAN	Local Area Network
LCD	Liquid Crystal Display
LED	Light Emitting Diode
LFSR	Linear Feedback Shift Register
LIF	Low Insertion Force
LO	Low
LSI	Large Scale Integration
LSIC	Large Scale Integrated Circuit
LSSD	Level-Sensitive Scan Design
LS(TTL)	Low Power Schottky TTL
L(TTL)	Low Power TTL
MAP	Manufacturing Automation Protocol

MATE	Modular Automatic Test Equipment
MIL-STD	Military Standard
MKSA	Metre-Kilogram-Second-Ampère
MMS	Manufacturing Message Service
MODEM	Modulator-Demodulator
MOS	Metal Oxide Semiconductor
MRCA	Multi Role Combat Aircraft (Tornado)
MSI	Medium Scale Integration
MSIC	Medium Scale Integrated Circuit
MTBF	Mean Time Between Failure
MTD	Mean Time to Detect
MTR	Mean Time to Replace
MTTR	Mean Time To Repair
MTT	Mean Time to Test
MTW	Mean Time to Wait
NBS	National Bureau of Standards
NMOS	Metal Oxide Semiconductor (N-Channel)
OEM	Original Equipment Manufacturer
OSI	Open System Interconnection
PABX	Private Automatic Branch Exchange
PAL	Programmable Array Logic
PBX	Private Branch Exchange
PC	Personal Computer
PCB	Printed Circuit Board
PIA	Programmable Input Adapter
PIO	Parallel Input-/Output Port
PMOS	Metal Oxide Semiconductor (P-Channel)
PN	Pseudo-random Noise
PRBS	Pseudo-random Binary Sequencer
PROM	Programmable Read Only Memory
R	Resistor
RAM	Random Access Memory
ROM	Read Only Memory
SA	Signature Analysis
S-A-0	Stuck-At-Zero, Stuck-At-Low
S-A-1	Stuck-At-One, Stuck-At-High
SAR	Signature Analysis Register
SDI	Scan Data Input
SDLC	Synchronous Data Link Control
SET	Standard d'Exchange et de Transfert
SI	Système International d'Unités
SIO	Serial Input-/Output Port
SMD	Surface Mounted Device

SOS	Silicon On Sapphire
SRL	Shift Register Latch
SSI	Small Scale Integration
SSIC	Small Scale Integrated Circuit
STEP	Standard for Exchange of Product Definition Model
S(TTL)	Schottky TTL
T, t	Time
TCP	Transmission Control protocol
TISS	Tester Independent Support System Software
TP	Test Point
TTL	Transistor–Transistor Logic
TURINO	Totally Universal Reset Initialization and Nodal Observation
VHSIC	Very High Speed Integrated Circuits
VLSI	Very Large-Scale Integration
VLSIC	Very Large-Scale Integrated Circuits
WAN	Wide Area Network
X	Undefined Logic State
Z	High Impedance
ZIF	Zero Insertion Force

Contents

Foreword xi

List of Abbreviations xii

1 Basics and Development of Electrical Measuring and Testing Techniques 1

- 1.1 Testing — an interactive process between humans and their environment 1
- 1.2 The development of electrical measurement and testing technology 4
 - 1.2.1 The International System of Units (SI system) 5
 - 1.2.2 Principal processes in electrical metrology 6
 - 1.2.3 Measurement and stimulation equipment in electronic testing 7
- 1.3 The combination of testing and process technologies — automatic test equipment (ATEs) 10
 - 1.3.1 Information processing in a test procedure 11
 - 1.3.2 Use of computers in testing 11
 - 1.3.3 Standardized process interfaces 13
 - 1.3.4 Software for automated testing 14

2 Technological and Economic Importance of Testability in Testing Processes 17

- 2.1 Accessibility of circuits for testing 17
 - 2.1.1 Passive methods 17
 - 2.1.2 Active methods 19

2.2	Adaptation of test objects for automatic testing	19
2.2.1	In-circuit test and functional testing	20
2.2.2	The problem of testability in error correcting circuits	21
2.2.3	Visual testing methods	22
2.3	Economic aspects of testing	23
2.3.1	How much does testing cost?	23
2.3.2	Importance of testing for the lifetime costs of electronic products	25
2.3.3	Cost minimization and preservation of resources	27
3	Failure Types, Causes and Frequencies	29
3.1	Reliability considerations	29
3.1.1	Rate of failure and MTBF	29
3.1.2	The effect of MTBF and failure rates	31
3.1.3	Availability	31
3.2	Failure types and causes in digital circuits and their functionality (functional failures)	32
3.2.1	Static failures (Stuck-at failures)	32
3.2.2	Dynamic faults	33
3.2.3	Intermittent faults	34
3.3	Fault types and fault causes in digital circuits during manufacture	35
3.3.1	Processing faults	36
3.3.2	Population faults	36
3.4	Failure frequencies	37
4	Partitioning Electronic Products	38
4.1	Partitioning at equipment level	38
4.1.1	Functional partitioning at equipment level	39
4.1.2	Physical partitioning	41
4.2	Partitioning at assembly level	42
4.2.1	Functional partitioning at assembly level	42
4.2.2	Physical partitioning	43
4.2.3	Partitioning at logic families (technologies)	43
4.2.4	Partitioning by separation of supply voltages	44
4.3	Functional modularity and its influence upon exchangeability	45
5	Test Points	51
5.1	Passive test points (measurements)	52

5.2	Active test points (stimulation)	52
5.3	Active and passive test points	53
5.4	Characteristics of test points	53
5.5	Choice of test points	54
5.6	Multiplex method	56
5.7	Safety considerations at test points	59
5.7.1	Device safety	60
5.7.2	Operator safety	60
5.8	Mechanical construction of test connectors	60
5.8.1	Device connectors	60
5.8.2	Module connectors	61
5.9	Practical examples of the introduction of active and passive test points in digital electronics	62
5.9.1	Practical applications of passive test points	63
5.9.2	Practical realization of active test points	66
6	Structured Design	82
6.1	Scan-path method for synchronous circuits	82
6.2	Shift-register method for asynchronous circuits	85
6.3	Level-sensitive scan design (LSSD)	87
6.4	Random access scan logic	90
6.5	Scan set logic	91
6.6	Advantages and disadvantages of scan methods	91
6.6.1	Disadvantages of scan design	92
6.6.2	Advantages of scan design	92
7	Built-in Test	93
7.1	Signature analysis	94
7.1.1	General description of signature analysis	94
7.1.2	Operating principle	94
7.1.3	Timing diagrams	95
7.1.4	Representations	96
7.1.5	Parallel signature analysis	97
7.1.6	Signal considerations	98
7.1.7	Advantages and disadvantages of signature analysis	99

7.2	BILBO	100	
7.3	The TURINO method	102	
7.4	The standard testability bus	104	
7.4.1	Introduction	104	
7.4.2	Fundamentals	104	
7.4.3	Requirements for a standardized testability bus	105	
7.4.4	Functional and physical description	105	
7.4.5	Application examples for a normed testability bus	107	
7.4.6	Summary	112	
8	Testing Problems in LSI and VLSI Circuits		113
8.1	General considerations	113	
8.2	Historical and technical background	113	
8.3	Highly integrated circuits — advantages and disadvantages for testability	116	
8.3.1	Problems of testing building blocks populated with LSIC and VLSIC	118	
8.3.2	Advantages of testing building blocks populated with LSIC and VLSIC	118	
8.4	Test points in building blocks populated with LSI and VLSI	120	
8.4.1	Introduction of active test points in the control of LSI and VLSI circuits	120	
8.4.2	Introduction of passive test points for the observation of LSI and VLSI circuits	130	
8.5	Software initialization	134	
9	Guidelines for the Development of Analog Circuits		135
9.1	Guidelines for the development of low frequency circuits	135	
9.2	Guidelines for the development of high frequency circuits	136	
10	'Design for Testability' for Hybrid Building Blocks		137
10.1	General considerations	137	
10.2	Advantages of hybrid technology	137	
10.3	Applications for hybrid building blocks	138	
10.4	BIT techniques for hybrid building blocks	138	

10.5	Improvement of testability in hybrid building blocks	138
10.5.1	Design for testability of digital elements in hybrid circuits	139
10.5.2	Design for testability of analog elements in hybrid circuits	139
11	Generation of Programs for Digital Test Objects	140
11.1	General considerations	140
11.2	Simulation techniques	140
11.3	Application of simulation	142
11.3.1	Simulation of behaviour of fault-free logic (logic simulation)	142
11.3.2	Simulation of behaviour of logic with faults (fault simulation)	143
11.4	Automatic generation of test programs	146
11.4.1	General considerations	146
11.4.2	Testability analysis of digital circuits	148
11.4.3	Test screening	148
11.5	Further advantages of testability analysis	150
11.5.1	Automatic generation of test patterns	150
11.5.2	Computer-aided generation of digital pattern generation	153
11.5.3	Application of special testing techniques	154
12	CAE, CAM, CAD, CAT and CAR Combined	155
12.1	Computer-aided design and manufacturing processes	155
12.1.1	Clarification of terminology	155
12.1.2	Structure of a CAE workstation	157
12.1.3	Methods and CAE materials for the design of electronic components, modules and systems	160
12.1.4	Interfaces for <i>open</i> systems	164
12.2	Networks	166
12.2.1	Standards, communication interfaces and protocols	166
12.2.2	Local area networks	174
12.2.3	Digital exchanges	177
12.2.4	Comparison of LANs and digital exchanges	178
12.3	CAR structures	180
12.3.1	Considerations of the CAR process	180
12.3.2	Design and testing connection	182

13 Design for Testability — the Necessary Link Between Design and Testing	190
13.1 General considerations	190
13.2 The current situation in testing technology	192
13.3 Manufacture and testing — increasingly inseparable	192
13.4 Integration of CAT and CAD	195
13.4.1 Utilization of modular concepts with standardized computers at the workstation	196
13.4.2 Utilization of CAD and CAT systems networking	196
13.5 The future	197
Appendix 1	199
Steps for improving the testability of electronic circuits (checklist)	199
Appendix 2	211
The most important circuits and their test points	211
Appendix 3	217
Characteristic advantages and disadvantages of various technologies	217
Logic symbols and their algebraic representation	217
Bibliography	219
Index	225

1

Basics and Development of Electrical Measuring and Testing Techniques

1.1 TESTING — AN INTERACTIVE PROCESS BETWEEN HUMANS AND THEIR ENVIRONMENT

Testing environmental conditions is one of the natural instincts in all higher forms of life, and it is one of the prerequisites for their survival. Man, the highest form of life, is equipped with sense organs which enable him to survive in his natural environment. However, man does not possess the *best* sensors by any means — many other creatures have sensors which far exceed human ones in terms of sensitivity, resolution, bandwidth, robustness, etc.; and the superiority of humans compared to other creatures can hardly be explained by the high quality of their sensors — rather, it is the combination of sensing *and* intelligence which gives them the advantage.

During the last century, as in many other areas of technology, an evolutionary development took place in instrumentation, with instruments emerging in response to a need for simple sensors for the observation and comprehension of electrical phenomena. The methods used were refined to the limits of the physically possible and any extensions of instrumentational ability seemed unlikely in the foreseeable future. Only since the advent of powerful computers have *intelligent* sensors been realized in modern instrumentation.

Intelligent sensors, supported by computers, can carry out further complex processing of data so that it is possible, for example, to increase considerably the overall measurement accuracy by correlating data from several different types of sensor. Correlating data with previously stored results or experiences further asserts the information content of the data (Figures 1.1 and 1.2).

Early sensor technology was limited to passive observation and surveillance of quantities in the environment. Very early on in that process, however, man was not content with observation alone; he wanted to influence his environment actively. He observed that physical and chemical influences stimulate certain characteristics, that

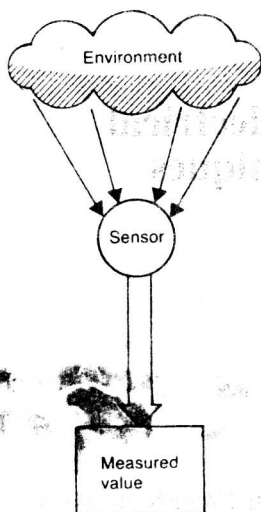


Figure 1.1 Measurement process with one sensor

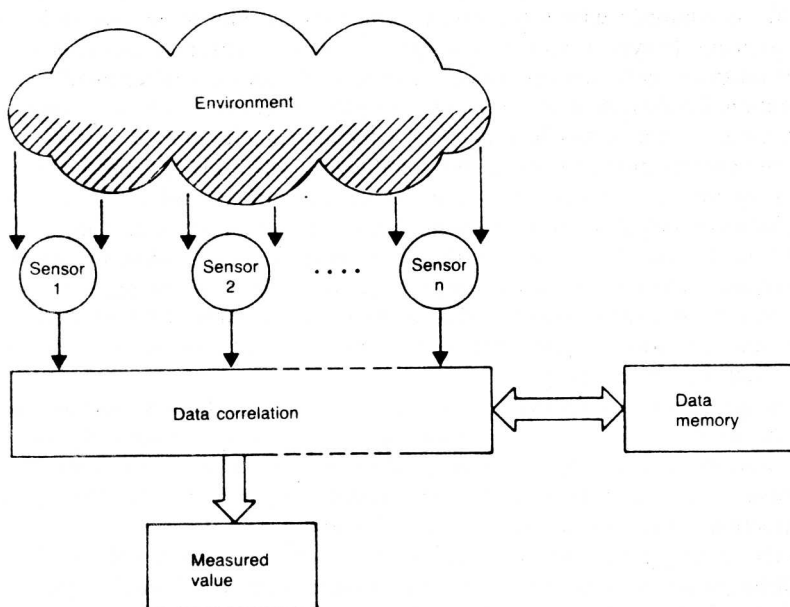


Figure 1.2 Combining measurement values — 'Intelligent Sensor'

these characteristics could be changed reproducibly, and that they allowed man influence over the nature of his environment.

Placed in its historical context, this procedure represented a revolutionary development. It was an achievement of human intelligence because it encompasses such capabilities as awareness of information (sensory perception), storage of information (memory) and drawing of conclusions from this information (inference) (Figure 1.3).

The discussion so far has been restricted to the natural environment of humans. During his development, man began to modify his surroundings imaginatively — he assumed the role of a creator, and was eventually able to transform natural materials by a range of creative abilities available to him and according to his needs and desires. However, it also became necessary to test these transformed materials, and establish their suitability for the task. The knowledge obtained allowed man to influence their characteristics directly for the first time.

To summarize, we can state that man is involved in the testing process:

1. As observer (sensory component).
2. As modifier (stimulus component).
3. As designer (creative component).

Most test procedures involve man in all three activities. Obviously, there is a strong interaction between the effects of all three functions. Such interaction can happen almost

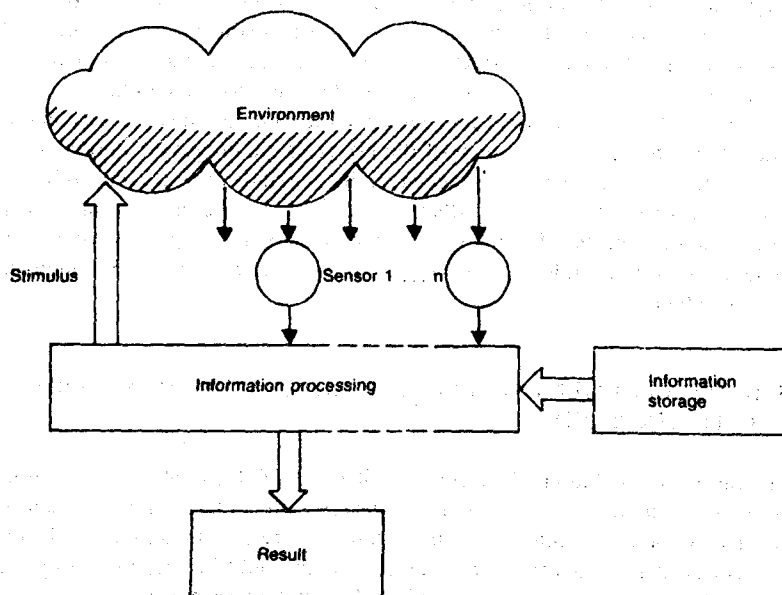


Figure 1.3 Combination of measurement and stimulation signals