

Compound Semiconductor Devices

Structures and Processing

Edited by
Kenneth A. Jackson

 **WILEY-VCH**

Weinheim · New York · Chichester · Brisbane · Singapore · Toronto

Preface

This volume covers the basic processes involved in the manufacture of compound semiconductor devices, starting with materials preparation, purification and crystal growth, includes a description of various device structures, and concludes with a description of the processes involved in device fabrication. The chapters are drawn from the book "Semiconductor Processing" which is Volume 16 of the VCH series on Materials Science and Technology.

It may be surprising to some how little the descriptions of the processing depends on the fundamental physics of semiconductors. The properties of the semiconductor determine what is to be done in the manufacturing process, but not how it is to be done. The processing depends critically on the properties of the wide variety of materials which are used, and the processing of semiconductor devices is a complex multi-stage sequence. There are many aspects of the processing of compound semiconductors which are common to silicon processing, but many of the devices are different, and the basic chemistry of the materials introduces significant differences in processing. In general the processing of compound semiconductors is more complex than silicon processing for a variety of reasons. It is more difficult to purify the starting materials and more difficult to grow single crystals. They are more susceptible to defect formation, and they are softer than silicon, and so must be handled more delicately. Care must be also taken to ensure that the processing preserves the stoichiometry, which is especially a problem when making electrical contacts.

Compound semiconductors have some advantages over silicon, for example, the electron mobility is higher in GaAs than in silicon. This increased mobility is used to make GaAs amplifiers which operate at higher frequencies than is possible with silicon devices. But silicon processing technology is at a more advanced scale of integration than compound semiconductor technology, and so, if a semiconductor device can be made with silicon, it will be. In spite of the many predictions that GaAs will replace silicon for all applications, the more complex processing which GaAs requires make it unlikely that this will happen. As the wag says: GaAs is a material of the future, and always will be. And so silicon is used almost exclusively for logic and memory devices. But because of its intrinsic electronic structure, it cannot be used to make devices which emit light, such as light emitting diodes (LED's) or semiconductor lasers. Semiconductor light source devices are the domain of compound semiconductors. The recent development of blue-emitting devices based on gallium nitride promise to extend the application of semiconductor light sources, and to lead to novel uses.

This volume does not deal with the semiconductor circuit design, although this is clearly the essential first step in the production of a device. Nor does it deal with testing, which is a major aspect of semiconductor manufacture. Simple circuits are sample tested, but complex chips are subject to extensive electrical and performance testing. The test stations are expensive and the tests are time consuming, so that testing is a major cost factor in semiconductor production.

There are two important aspects to the fabrication of semiconductors which are beyond the scope of this volume. Photoresists are used for the patterning of the dopant distributions, as well as the patterning of the dielectrics and metallization. The sophisticated chemistry which is involved in the design of photoresists is beyond the scope of this volume. The packaging technology which is used to protect the chips and to connect them to the outside world is also not discussed in detail.

This volume deals with the basic manufacturing processes for compound semiconductor devices. The fabrication process starts with purification, followed by the growth of single crystals. These processes often have aspects in common for the different compound semiconductors, but in general they are unique for each material. After growth, the crystals are sliced into wafers which are then polished. These processes are discussed in the first chapter by J. Brian Mullins. Compound semiconductor device structures including field-effect transistors, high electron mobility transistors, heterojunction bipolar transistors, and semiconductor lasers are described in the second chapter by William E. Stanchina and Juan F. Lam. In the concluding chapter, John M. Parsey, Jr. discusses compound semiconductor device processing, including doping, isolation methods, diffusion, etching, ohmic contacts and Schottky barriers, dielectrics, metallization, and die separation. The processing of a wafer typically involves hundreds of separate steps, but several hundred chips can be made from a single wafer. There is a continuing trend to use larger wafers and finer features on the wafers in order to get more chips from each wafer, and a continuing effort to improve performance and increase yields.

I would like to thank the authors who have taken time from their very busy schedules to prepare their chapters. They are experts in processing technology because they are involved with it on a daily basis, and it has been difficult for them to find the time to write. But the result is a valuable and timely description of the state-of-the-art of compound semiconductor processing.

Kenneth A. Jackson
Tucson, AZ
August, 1998

List of Contributors

Prof. Kenneth A. Jackson
University of Arizona
Arizona Materials Laboratory
4715 East Lowell Road
Tucson, AZ 85712
U.S.A.

Dr. Juan F. Lam
Hughes Aircraft company
Hughes Research Laboratories
3011 Malibu Canyon Road
Malibu, CA 90265-4799
U.S.A.

Dr. J. Brian Mullin
EMC Malvern
"The Hoo". Brockhill Road
West Malvern, Worcs.
WR14 4DL
U.K.

Dr. John M. Parsey, Jr.
Advanced Materials
Wireless Research and
Development Laboratory
Wireless Subscriber Systems Group
Motorola, Inc.
Tempe, AZ 85284
U.S.A.

Dr. William E. Stanchina
Hughes Aircraft Company
Hughes Research Laboratories
3011 Malibu Canyon Road
Malibu, CA 90265-4799
U.S.A.

Contents

1	Compound Semiconductor Processing	1
	<i>J. B. Mullin</i>	
2	Compound Semiconductor Device Structures	45
	<i>W. E. Stanchina, J. F. Lam</i>	
3	Compound Semiconductor Device Processing	61
	<i>J. M. Parsey, Jr.</i>	
	Index	175

1 Compound Semiconductor Processing

J. Brian Mullin

Electronic Materials Consultancy, Malvern, Worcestershire, U.K.

List of Symbols and Abbreviations	3
1.1 Introduction	4
1.2 Historical Background	4
1.3 Purification	7
1.3.1 General Purification Procedures	7
1.3.2 Zone Refining and Related Techniques	8
1.3.3 Problems with Specific Compounds	8
1.3.3.1 InSb and GaSb	9
1.3.3.2 InAs and GaAs	10
1.3.3.3 InP and GaP	10
1.3.3.4 II-VI Compounds	10
1.4 Technical Constraints to Melt Growth Techniques	11
1.4.1 Chemical Reactivity	12
1.4.2 Melting Point	13
1.4.3 Vapor Pressure	13
1.5 Crystal Growth	13
1.5.1 Horizontal Growth	14
1.5.2 Vertical Growth	16
1.5.3 Crystal Pulling	18
1.5.4 Liquid Encapsulated Czochralski (LEC) Pulling	20
1.5.4.1 The Low Pressure LEC Technique	20
1.5.4.2 The High Pressure LEC Technique	20
1.6 Crystal Growth of Specific Compounds	21
1.6.1 InSb	22
1.6.2 InAs and GaAs	22
1.6.3 InP	24
1.6.4 II-VI Compounds: General	26
1.6.4.1 Bulk $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$	26
1.6.4.2 CdTe and $\text{Cd}_{1-x}\text{Zn}_x\text{Te}$	27
1.6.4.3 ZnSe	28
1.6.4.4 ZnS and CdS	28
1.7 Fundamental Aspects of Crystal Growth	29
1.7.1 Structure	30
1.7.2 Temperature Distribution, Crystal Shape and Diameter Control	30
1.7.3 Solute Distribution	33

1.7.4	Constitutional Supercooling	34
1.7.5	Facet Effect, Anisotropic Segregation and Twinning	36
1.7.6	Dislocations and Grain Boundaries	39
1.8	Wafering and Slice Preparation	40
1.9	References	41

List of Symbols and Abbreviations

C_S, C_L, C_I	solute or dopant concentration (in the solid, in the liquid, at the interface)
d	depth of volume of convecting gas
D	diffusion coefficient
G	temperature gradient
h, k, l	Miller indices
H_f	latent heat of fusion
k	dopant distribution coefficient
k_0	equilibrium dopant distribution coefficient
K_0	thermal diffusivity
m	gradient of liquidus
p	gas pressure
P_G, P_d	pressure of gas, pressure of dissociation vapor of components
R_a	Rayleigh number
T	temperature
v	growth velocity
δ	boundary layer "thickness", parameter of BPS model
θ	angle
ν_0	kinematic viscosity
ρ_s	crystal density
σ	thermal conductivity
ϕ_L, ϕ_s, ϕ_G	interfacial energies
ω	angular rotation rate
ACRT	accelerated crucible rotation technique
BPS	Burton, Prim and Slichter
CRA	cast recrystallize anneal
HG	horizontal growth
LEC	liquid encapsulated Czochralski (techniques)
LPE	liquid phase epitaxy
MBE	molecular beam epitaxy
MCT	mercury cadmium telluride
MOVPE	metal organic vapor phase epitaxy
PBN	pyrolytic boron nitride
ppba	atomic parts per billion
ppm	parts per million
QA	quench anneal
RF	radio frequency
SI	semi-insulating
TGZM	temperature gradient zone melting
THM	traveling heater method
VGf	vertical gradient freeze (technique)
VP	vertical pulling

1.1 Introduction

This chapter reviews the general principles and practice governing the preparation and processing of compound semiconductors and their alloys, how they are purified, how they are prepared as single crystals and how they are converted into wafers suitable for epitaxial growth.

The range of materials which can be classified as compound or alloy semiconductors is vast and covers the whole of the periodic table. It includes IV–IV, II–IV, I–V, II–V, III–V, I–VI, II–VI, III–VI, IV–VI, V–VI, I–III–VI, I–IV–VI, I–V–VI, II–IV and II–III–V compounds. However, because of the enormous cost of developing these materials as high-quality semiconductors most of these compounds are currently in a relatively primitive state of development when compared with Ge or Si. Indeed the only compounds which have been developed to a state of significant commercial application are to be found in the III–V and II–VI semiconductor groups of materials. It is with these classes of materials that this chapter will be mainly concerned.

The efficient processing of semiconductors in a form suitable for device application requires a sound understanding of the practical technologies involved together with a knowledge of the scientific principles underlying these technologies. Both the technology and the science of the processing will be covered in this chapter. However, it is important to appreciate that the technology as opposed to the science of semiconductor processing is undergoing a constant evolution driven by ever more demanding specifications arising from an ever increasing range of devices.

1.2 Historical Background

Probably the most important event which promoted significant scientific and technological research in the processing of semiconduction materials was the discovery of transistor action in germanium by Brattain and Bardeen (1948) which had been stimulated by the predictions of Shockley (1949). As a result serious international interest developed in the search for new semiconductors. II–VI compounds had of course been known since before the beginning of the century, but the early work of Welker (1952, 1953) and his colleagues in Germany on III–V compounds following the discovery of transistor action marked the beginning of the evolution of compound semiconductor processing.

Our knowledge of semiconductor processing (Mullin, 1975 a, b, 1989; Thomas et al., 1993), indeed of all aspects of semiconductors and the solid state, is rooted in research on Ge in the 1950s. Even early work in this period highlighted the two overriding requirements for semiconductors, the need for high purity and the need for single crystals.

The first requirement resulted in the creation of new methods of purification and the evolution of a most significant concept, the concept of semiconductor purity. This specified the need for unprecedentedly low levels of impurities, typically less than 10 parts per billion atomic (ppba) of electrically active impurities. The second requirement resulted in the development of new technologies for producing completely single crystals free from defects including dislocations.

At the forefront of this materials work aimed at fulfilling these demands of purity and crystalline perfection was the development of the science and technology of crys-

tal growth. In less than a decade the intense research and development effort resulted in the melt growth of Ge developing from an art to a science.

In the case of the compound semiconductors, the less difficult materials, like InSb, followed the pattern of evolution of Ge, and single crystals containing less than 10^{13} carriers/cm³ (1 ppba is equivalent to 2.9×10^{13} atoms/cm³) were state of the art well within a decade. However, in the case of the more difficult materials like GaAs, InP and GaP, their evolution has taken over three decades and is still in a development phase. For the very difficult materials like ZnSe no melt growth technology has yet been devised that can achieve reproducibly and readily acceptable quality single-crystal material, although there are promising developments (Rudolph et al., 1994). For ZnSe, vapor growth techniques are pioneering the way to semiconductor quality (Cantell et al., 1992).

The key to the development of Ge was the creation of new melt growth technologies. Very significant contributions to our knowledge resulted from the pioneering work of Pfann (1966) on zone melting and Teal (1958) on the vertical pulling of single crystals.

Pfann (1966) initiated the concept of zone melting. This generic term covers a range of related horizontal crystallization technologies. The simplest technology is the single zone freeze in which a horizontal boat containing a molten charge is progressively frozen from one end. Other procedures were developed involving the translation of a liquid zone through a solid ingot. In particular it created two very powerful processing technologies, zone leveling and zone refining (see Sec. 1.3.2).

Zone leveling was initially applied to Ge and resulted in a very successful crystallization technology for the production of

uniformly doped single-crystal material. This process involves the formation of a liquid zone in a solid ingot and its movement through the ingot in one direction and subsequently, for ideally uniform material, in the reverse direction. The liquid zone acquires a constant dopant concentration $1/k$ times that in the solid, where k , the distribution coefficient, is given by $k = C_s/C_L$ and C_s and C_L are the concentrations of dopant in the solid and liquid respectively. This process levels out the dopant concentration in the solid so that the dopant concentration of the solid being melted is the same as the concentration in the solid being crystallized.

The horizontal technologies were not only used for zone leveling and for purification by zone refining but they were also developed for the growth of single crystals. This was achieved by arranging for a molten zone to melt-back into a single crystal seed positioned at one end of a polycrystalline ingot. The solid which crystallized on the seed as the zone was moved through the ingot took up the orientation of the seed and resulted in the formation of a single crystal.

In addition to HG for the growth of single crystals, the use of VP of crystals from the melts was pioneered by Teal (1958). The technique has its origins in the Czochralski technique. Czochralski (1917) arranged to dip a thin rod which acted like a seed into a molten melt of metal and withdraw it from the melt. As the liquid was pulled away from the melt it crystallized, giving regions of single crystal metal. However, this technology is far removed from modern crystal pulling technology.

The modern pulling technique (Teal, 1958) was developed during the initial phase of semiconductor research at Bell Labs in the 1950s and early 1960s. The most important innovation was the intro-

duction of rotation using a pull rod. A single-crystal seed was mounted in a chuck on the pull rod which could be raised and lowered at a set rate. In the pulling process the crystal nucleated on the seed and its diameter was controlled by adjusting the power to the melt. This concept had profound consequences for the semiconductor processing of single crystals.

Theoretical work on crystal pulling has also had an important influence on the development of the technology. The work of Burton, Prim and Slichter (BPS) (Burton et al., 1953) on solute distribution during crystal growth proved to be most significant. They modeled solute transport in the melt adjacent to the rotating crystallizing surface using concepts developed by von Kármán (1921) and Cochran (1934). BPS established the flow normal to the disc as a function of the crystal growth parameters enabling quantitative estimates to be made of the solute distribution from the interface into the melt. Use of the BPS model has stimulated much research and laid the foundations of a great deal of our understanding of the science of crystal growth from the melt.

It has been used, for example, in the modeling of heavy doping during crystal pulling. This has resulted in a predictive theory of constitutional supercooling (Hurle, 1961; see Sec. 1.7.4). This knowledge is directly relevant to the crystallization of compound semiconductors from nonstoichiometric melts, where constitutional supercooling is a very common occurrence and can be a major problem seriously affecting crystal quality.

The causes of nonuniform dopant or impurity incorporation are a major consideration in understanding the mechanisms of crystal growth. Of particular significance has been the discovery of the facet effect (Hulme and Mullin, 1959) and anisotropic

segregation (Mullin, 1962) of dopants during crystal growth. Also important are impurity striations, which are a common occurrence. Crystal rotation introduces periodic impurity incorporation due to the growth rate variations imposed by the rotating crystal. The incorporation of dopants will be developed in further detail in Sec. 1.7.5.

The science of horizontal growth (HG) has lagged significantly behind that of vertical pulling (VP). In HG there is no effective working theory for convection in the molten zone and transient control of doping as opposed to uniform doping is not possible as it is in VP. The VP technique thus evolved as a favored tool for investigating the science of crystal growth from the melt.

From an historical viewpoint it is instructive to follow the evolution and role of HG and VP techniques in relation to the science and technology of Ge and Si. The horizontal growth of Ge, a technology that pioneered purification by zone refining and the production of doped single crystals by zone melting, gradually emerged as the more cost effective crystal growth process and replaced the VP technique. Ultimately however, the semiconductor applications of Ge were taken over by Si, eliminating the need for Ge altogether with the exception of a few specialist applications such as the growth of very large crystals for detectors. These are fulfilled by pulling.

It is interesting that the VP technique that was developed for Ge created the conditions for the single-crystal growth of Si. Silicon with its superior device properties has emerged as the dominant semiconductor and as such has had and continues to have a profound influence on every aspect of semiconductor processing. The VP technique has been refined and developed for Si and is still the dominant industrial tech-

nology for Si. But, also of major importance for Si is the float zone technique, in which a liquid zone out of contact with the container is moved through a vertical rod of Si. This zone refining action produces the very highest grade of single-crystal Si, a very important industrial requirement. Nevertheless, it is important to recognize that some of the unique properties of the compound semiconductors have also stimulated developments in semiconductor processing.

Undoubtedly the very rapid expansion in our knowledge of semiconductor processing can be attributed to the relative ease of handling Ge and in particular to the ability to hold and crystallize molten Ge with negligible contamination from silica apparatus. The technology of Si is in many ways very different to that of Ge. It reacts with SiO_2 and cannot be crystallized in a silica boat. It also forms a tenacious oxide which requires special techniques to prevent its formation. Hence the importance of the pulling technique and the non-contacting float zone technique in its development.

Technology never stands still. Zone refining has been developed (Hukin, 1989) for Si using a horizontal water-cooled Cu boat. A liquid zone is formed and levitated out of contact with the boat using RF fields. Two-meter, 125 cm^2 section solar cell grade Si can be produced in this way.

The III-V and II-VI compounds present different problems again to those of Si. The antimonides are similar in their attributes to Ge but the arsenides and the phosphides, selenides and tellurides suffer dissociative decomposition near their melting points, resulting in the loss of one of their component elements. As a result, closed-tube techniques needed to be developed in order to prevent vapor loss. This has stimulated new technologies such as

liquid encapsulation and more recently the vertical gradient freeze (VGF) technique to overcome this problem.

The relatively slow development, over three decades, of these compounds is in no small way due to the difficulties associated with dealing with compounds which have a significant vapor pressure at the melting point. In addition the number of point defects at the melting point is high $\sim 10^{19} \text{ cm}^{-3}$. This leads to extended defects and doping nonuniformities and a range of problems not found in Si and Ge. The continuing challenge of processing technology is to understand and control these problems.

1.3 Purification

The cost of developing the knowledge and technology to be able to process raw materials into device quality semiconducting compounds is enormous and inevitably involves a very significant research and development effort involving both purification and crystal growth. As a consequence, there are only a few highly developed compound semiconductors. These include InSb, GaAs, InP, GaP and CdTe and its related alloys with HgTe. Most of the II-VI compounds are still not readily available in wafer form as high-quality single-crystalline material. The basic aspects of the purification technologies required to produce high-purity semiconducting compounds will now be considered.

1.3.1 General Purification Procedures

It is convenient to identify two stages in the purification of semiconductor compounds, firstly the purification of the elements themselves and secondly the purification of the compounds. From an historical perspective the role of the more con-

ventional chemical purification procedures has been more useful than zone refining in purifying the elements. This can be appreciated from the early reviews in Willardson and Goering's book on III-V compounds (1962). It is evident that work on zone refining of group III metals as well as phosphorus and arsenic was clearly not seen to be markedly effective. This coupled with the fact that zone refining represented an additional costly batch process meant that its use has always been problematical, especially for elements like In and Ga which are low melting point readily alloyable metals with a tendency, in the case of Ga, to supercool.

Whilst zone refining has not been particularly useful for the common elements of groups III and V, in the case of groups II and VI zone refining has proved to be a very effective process for the production of ultra-pure Cd and Te. This development was made possible by military funding since these elements are used in the preparation of HgCdTe for infrared detectors. Here very high purity elements, having less than 1 part in 10^9 electrically active impurities are essential.

It is evident that zone refining is most effective for strongly bonded materials which crystallize well and in which impurities have a low solubility. These criteria apply particularly to the compounds themselves. Thus many compounds can be zone refined but most compounds have their own peculiarities, demanding specialized processes. These will be considered for the more important compounds later.

1.3.2 Zone Refining and Related Techniques

Zone refining, which involves the motion of a liquid zone or zones through an ingot, is the most important and effective

purification procedure for Ge. The impurities that are less soluble in the solid, or more soluble in the liquid ($k_0 < 1$), are moved in the direction of crystallization towards the finish (last to freeze) end of the ingot whereas the impurities that are more soluble in the solid ($k_0 > 1$), that is, less soluble in the liquid, are moved to the start end of the ingot. Provided the distribution coefficients¹ k_0 are not close to 1 – a condition satisfied by Ge – this very simple process can after very few zone passes produce semiconductor purity in an ingot. A remarkable result.

One can appreciate the effectiveness of zone refining from the graphs in Fig. 1-1, where the theoretical ultimate distributions for impurities having different distribution coefficients are given. Orders of magnitude improvement in purification are indicated. However, these dramatic results must only be taken as a guide since solid-state diffusion and vapor transport can reduce the effectiveness of impurity removal.

1.3.3 Problems with Specific Compounds

Processing by conventional zone refining or chemical purification methods is often insufficient on its own as a means of achieving semiconductor purity in compounds. Inevitably there is some problem or problems, some difficult-to-remove residual impurity or some quirk of contamination that needs to be dealt with in an unconventional manner if the ultimate goal of semiconductor purity is to be achieved.

¹ The equilibrium distribution coefficient k_0 of a solute (dopant, impurity or excess component) is the ratio of the concentration of the solute in the solid, C_s , to the concentration of the solute in the liquid, C_L , if the phases are kept in contact for a sufficiently long period for them to come to equilibrium.

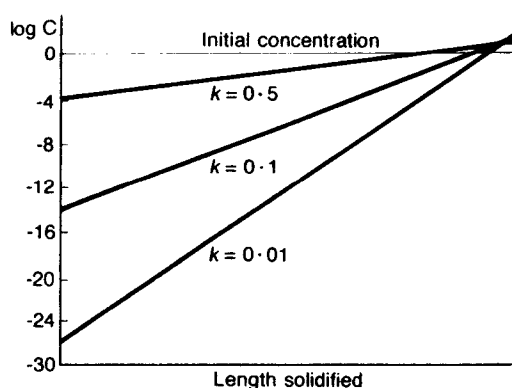


Figure 1-1. Theoretical ultimate distributions for dopants having different distribution coefficients (k) after multiple zone refining passes in an ingot where the zone length is 10% of the ingot length. It is assumed that there is no back reflection of dopant from the freezing of the last zone length. The results highlight the potential of zone refining (see Pfann, 1966).

In this section problems or aspects of purification will be considered which have proved to be important in the achievement of semiconductor purity of the more important compound semiconductors. It should be stressed that achieving semiconductor purity in compounds is a very demanding and generally costly process and one that is frequently underestimated. The processes of purification and the avoidance of contamination represent a continuous battle if the ultimate in semiconductor performance is to be achieved. In the case of many of the II–VI compounds for example the presence of impurities could still be the principal problem preventing their effective development.

1.3.3.1 InSb and GaSb

Indium antimonide (Hulme and Mullin, 1962) has attracted much more research and development (R&D) over the years than GaSb. Major factors in this interest are of course the device applications of the material. InSb, for example, is an impor-

tant infrared detector material suitable for detectors working in the 3–5 μm region of the spectrum.

The low melting point of InSb, 525°C, combined with the negligible vapor pressure of Sb over its melt make InSb an ideal candidate for conventional zone refining procedures. However, the straightforward process is of limited value because of troublesome impurities, particularly Zn and Te. Not only do they exhibit anisotropic segregation (Mullin, 1962), but in the case of Te the value of its effective distribution coefficient, k_{eff} (see Sec. 1.7.5) can range from ~ 0.5 for growth in a non-[111] direction to ~ 4.0 for growth on a (111) facet. Thus Te would be distributed in polycrystalline material as though the effective k were some weighted mean of these values, that is, close to one. Zinc has a value of k_{eff} ranging from ~ 2.3 to ~ 3.0 . But more troublesome is its volatility at the melting point of InSb. Vapor transport of Zn above the ingot can reduce the efficiency of zone refining.

This problem has been overcome by using the volatility of Zn to advantage in a two-stage evaporation and zone-refining procedure (Hulme, 1959). Zone-refined Sb in excess of that required to form stoichiometric InSb is added to high-purity In in a boat in a modified zone-refining apparatus and melted under vacuum. Both Zn and Sb evaporate from the molten charge and condense on the cooled upper surface of the outer containing tube. The excess Sb traps in the very small quantity of the more volatile Zn.

After a timed period when the excess Sb has evaporated the ingot is cooled and frozen. It is then zone refined under an atmosphere of H_2 , a condition where the Sb has negligible volatility. The purification process is highly reproducible, resulting in the production of very high

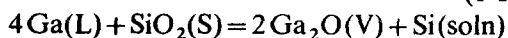
purity InSb with some 60% of the ingot having a carrier concentration less than $1 \times 10^{14} \text{ cm}^{-3}$.

GaSb has not been developed in this way but it can be zone refined. The incentive to purify the material further, however, is limited by the belief that the residual carrier level, $\sim 2 \times 10^{16}$ p-type carriers per cm^3 , is determined by fundamental aspects of the band structure of the compound.

1.3.3.2 InAs and GaAs

InAs and GaAs present additional handling problems because at their melting points the As dissociation pressures are respectively ~ 0.3 and ~ 1.0 atm. Nevertheless, considerable R&D effort has been carried out on GaAs using conventional hot wall technologies. However, a major problem encountered on zone refining GaAs has been the failure to achieve purities with carrier levels below 10^{16} to 10^{17} n-type carriers per cm^3 . This has been shown by Hicks and Greene (1971) to be due to the reaction between Ga in the liquid Ga, As melts and the silica containing vessel, which introduces a fairly constant level of Si into the ingots at about one part per million:

(1-1)



The problem can be overcome by using BN or graphite boats. However, the zone-refining process has generally been superseded and simplified by in situ compounding of very high purity Ga and As which are now available as a result of improvements in chemical purification methods (see Sec. 1.6.2).

1.3.3.3 InP and GaP

The very high vapor pressures generated by these compounds at their melting points, some 27 atm and 32 atm for InP

and GaP respectively, makes zone refining a difficult and potentially hazardous process. The compounds can nevertheless be prepared in horizontal systems by distilling the P_4 into the molten group III element contained in a silica or BN boat. By limiting the amount of group V distilled so that the group III element is in excess of stoichiometry the working vapor pressures are reduced. Crystallization under these conditions has an additional advantage; there is a very much greater purification effect for impurities from group III rich liquids than from stoichiometric melts. The disadvantage of course is that crystallization occurs under conditions of constitutional supercooling, which can result in trapping of the impurity-rich group III element in the solid.

With the availability of purer starting elements, formation of the compounds from stoichiometric melts is now more usual. Nevertheless, further purification is generally required, and is now often achieved by pre-pulling charges using the liquid encapsulation technique. InP having 10^{15} carriers/ cm^3 can be produced in this way. A similar purification procedure for GaP can be used. The current commercial demands on GaP are somewhat less than on InP since it is either used as doped material or as a substrate on which active layers are grown. There is clearly scope for the development of further purification procedures for both these compounds.

1.3.3.4 II-VI Compounds

The state of development of the II-VI compounds is significantly behind that of the III-V compounds even though they have a much longer history. Many of the II-VI compounds, especially the higher energy gap oxides, sulfides and selenides, are not accessible by melt growth tech-

niques and as a consequence there is a much greater emphasis in the use of vapor growth techniques to grow these difficult compounds. Our knowledge of the use of vapor growth as a purification technology is primitive. There is no equivalent to zone refining. Hence there is a more general tendency to rely on the use of elements that have been purified chemically or by zone refining.

The elements Hg, Cd and Te, components of the exceptionally well developed infrared detector material $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$, are now available as very high purity elements as a result of multiple zone refining technologies (Cd and Te) and distillation techniques (Hg). Hence compounds of these elements are prepared in situ by direct reaction. Most of the other elements Zn, Se and S although currently available in conventional high purity form are generally not as pure as the detector materials and do not form very pure semiconducting compounds.

Zone refining of the II–VI compounds is not efficacious because of the volatility of both the group II and group VI elements as well as the compounds themselves. Hence there has been little development of conventional zone-refining technology for the compounds. However, a related zone-refining technology called the traveling heater method (THM) or sometimes the traveling solvent method has attracted much interest and development for the II–VI compounds. In the traveling heater method a molten zone is moved through the ingot as in zone refining, but in THM the zone comprises a solvent of Te or Se. Thus the compound dissolves at the leading edge of the zone and crystallizes out at the trailing edge.

This has two advantages. Firstly, it reduces the temperature of crystallization significantly below the melting point of the

compound, thus markedly reducing the vapor pressure of the components of the compound, effectively eliminating evaporation. Secondly, it provides a group VI rich solution in which impurities are exceptionally soluble, a condition which results in the crystallization of a very pure compound. Because of the reduced growth temperature it is also possible to eliminate sub-grain boundaries. The technique, however, has not yet been developed to grow large completely single crystals. The process has been exploited particularly by Triboulet (1994) and the CRNS Bellevue group for the preparation and purification of $\text{Hg}_{1-x}\text{Cd}_x\text{Te}$, $\text{Hg}_{1-x}\text{Zn}_x\text{Te}$, CdTe, HgTe and ZnTe, as well as CdMnTe. It clearly has scope for the preparation and purification of ZnSe and various alloys of the compounds.

The potential disadvantage of the technique is that the crystallization occurs under conditions of constitutional supercooling and solvent trapping can occur and give rise to group VI rich precipitates together with impurities. Nevertheless it would appear that by optimizing the temperature gradients and the gradient of constitutional supercooling (see Sec. 1.7.4) the worst effects of solvent trapping can be avoided.

1.4 Technical Constraints to Melt Growth Techniques

The processing of compound semiconductors by melt growth techniques both for purification and crystal growth is generally much more difficult than the processing of Ge because of constraints imposed by the properties of the materials. Some of the significant properties which lead to constraints in the use of melt growth and related processing are listed in

Table 1-1. Material properties of main semiconductors.

Compound	Melting point (°C)	Vapor pressure at M.Pt.(atm)	CRSS at M.Pt (MPa)	References
InSb	525	4×10^{-8}		Muller and Jacob (1984)
GaSb	712	1×10^{-6}		Muller and Jacob (1984)
InAs	943	0.33		Van der Boomgaard and Schol (1957)
GaAs	1238	1.0	0.7	Arthur (1967); Thomas et al. (1990)
InP	1062	27.5	0.36	Bachmann and Bühler (1974); Thomas et al. (1990)
GaP	1465	32		Nygren et al. (1971)
HgSe	799			Mayer (1984)
HgTe	670	12.5		Harman (1967); Strauss (1971)
CdSe	1239	0.3		Bassam et al. (1994); Lorenz (1967)
CdTe	1092	0.65	0.2	Isshiki (1992); Strauss (1971); Balasubramanian and Wilcox (1992)
ZnSe	1526	0.5		Isshiki (1992); Lorenz (1967)
ZnTe	1300	0.6		Isshiki (1992); Lorenz (1967)
Ge	960		0.70	Thomas et al. (1990)
Si	1420		1.85	Thomas et al. (1990)

Table 1-1. Consideration of a wider range of properties, chemical reactivity, melting point, vapor pressure, critical resolved shear stress and ionicity are important in understanding the suitability, or more often, the unsuitability of a particular technology.

1.4.1 Chemical Reactivity

Although not specifically listed in Table 1-1, chemical reactivity is an important constraint in all processing. The main problems arise from the reactivity of the molten semiconductor with the container or the gaseous environment. In this respect container materials have proved to be the dominant source of contamination for compound semiconductor melts.

Vitreous silica is widely used as a crucible or boat material and is essentially stable against attack from the lower melting point materials like Ge (937°C), InSb (525°C) and GaSb (712°C). But, for higher melting point materials there is gen-

erally contamination with silicon due to the reduction of the SiO_2 by the melt, in the case of GaAs (1238°C) it is typically above the part per million (ppm) level in the crystallized material. Pyrolytic boron nitride PBN can be used to overcome this problem and is well suited to the growth of III-V compounds since it is a III-V also and does not appear to give rise to electrically contaminating impurities. It is however expensive.

Graphite is also used since it is stable in an inert atmosphere and does not appear to directly cause electrically active doping by contaminating melts. Graphite will react with silica at high temperature, but at lower temperatures (<900°C) it is a very useful material and is used as a slider boat material in liquid phase epitaxy (LPE) and as a boat material for II-VI compounds. But, carbon can be electrically active as an acceptor in GaAs for example. It can be introduced on an As vacancy site via CO under Ga-rich growth conditions, hence the importance of removing O_2 and H_2O .