ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS

SECOND EDITION

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SYMBOL CONVENTION

Unless otherwise stated, the following symbol convention is used in this book. *Bias* or *dc* quantities, such as transistor collector current I_C and collector-emitter voltage V_{CE}, are represented by uppercase symbols with uppercase subscripts. *Small-signal* quantities, such as the incremental change in transistor collector current i_c, are represented by lowercase symbols with lowercase subscripts. Elements such as transconductance g_m in small-signal equivalent circuits are represented in the same way. Finally, quantities such as *total* collector current I_c, which represent the sum of the bias quantity *and* the signal quantity, are represented by an uppercase symbol with a lowercase subscript.

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PREFACE

In the six years since the publication of the first edition of this book, the field of analog integrated circuits has broadened to encompass MOS technology as well as the more traditional bipolar technology. Bipolar technology is still the dominant means of fabricating commercial analog integrated circuits, particularly stand-alone analog circuits of low-to-moderate complexity such as operational amplifiers and voltage regulators. Consequently, bipolar technology is the primary focus of this second edition.

The use of MOS technology to implement analog functions has evolved rapidly in the past five years and continues to grow. The principal motivation for this trend is the need to incorporate analog functions together with complex digital functions on a single integrated circuit in the same technology. The most common function of this analog circuitry is to form the interface between the analog variables produced by sensors and transducers of physical variables, and a digital processor that may implement control, communications, or instrumentation functions. The functions most often required are anti-alias and reconstruction filtering, digital-analog conversion, voltage comparison, sampling, precision amplification, and generation of precision reference potentials. The new material that is incorporated in this second edition is intended to provide the foundation for the device-level analysis and design of these types of circuits in MOS technology. Fortunately, much of the theory that is developed for the analysis and design of bipolar circuits can be used with only minor modification for the analysis of MOS circuits.

To minimize disruption to courses already using the first edition, we have added material on MOS device modeling at the end of Chapter 1, material on MOS technology at the end of Chapter 2, and placed the MOS circuit design and analysis material in a new chapter at the end of the book. The remainder of the book remains essentially unchanged. Thus, the MOS material can be taught together with the bipolar material or relegated to a later course, at the discretion of the instructor.

We would like to acknowledge the contributions to this edition of our colleagues Professors D. A. Hodges and R. W. Broderson of the University of California, Berkeley. They, together with several generations of graduate students at Berkeley, have made major contributions to the material covered in this book.

Paul R. Gray
Robert G. Meyer
Berkeley, California, 1983

PREFACE TO THE FIRST EDITION

This book deals with the analysis and design of analog integrated circuits. Analog circuits are circuits whose inputs and/or outputs are continuously varying analog signals in which the information is conveyed by the instantaneous value of the waveform. We want this book to be useful both as a text for class use and also as a reference book for practicing engineers. For class use, there are numerous worked problems in each chapter; the problem sets at the end of each chapter illustrate the practical applications of the material in the text. Both authors have had extensive industrial experience in integrated circuit (IC) design as well as in the teaching of courses on this subject, and this experience is reflected in the choice of text material and in the problem sets.

Although this book is concerned largely with the design of ICs, a considerable amount of material is also included on applications. In practice these two subjects are very closely linked and a knowledge of both is essential for both designers and users. The latter compose the larger group by far, and it has been our experience that a working knowledge of IC design is a great advantage to an IC user. This is particularly apparent when the user must choose from among a number of competing designs to satisfy a particular need. An understanding of the IC structure is then extremely useful in evaluating the relative desirability of the different designs under extremes of environment or in the presence of variations in supply voltage. In addition, the IC user is in a much better position to interpret a manufacturer's data if he has a working knowledge of the internal operation of the integrated circuit.

The contents of this book originated largely in two courses on analog integrated circuits given at the University of California at Berkeley. The first of these is a senior level elective and the second a graduate course. The book is structured so that such a two-course sequence can be taught using it as the basic text. The more advanced material is found at the end of each chapter or in an appendix, so that a first course in analog integrated circuits can omit this material without loss of continuity. An outline of each chapter is given below together with suggestions for material to be covered in such a first course. It is assumed that the course consists of three hours of lecture per week over a 10-week quarter and that the students have a working knowledge of Laplace transforms and frequency-domain circuit analysis. It is also assumed that the students have had an introductory course in electronics so that they are familiar with the principles of transistor operation and with the functioning of simple analog circuits. Unless otherwise stated, each chapter requires about three lecture hours to cover.

Chapter 1 contains a summary of bipolar transistor and junction field-effect transistor (JFET) device physics. We suggest spending one week on selected

topics from this chapter, the choice of topics depending on the background of the students. The material on JFETs could be omitted from a first course. The material of Chapters 1 and 2 is quite important in IC design because there is significant interaction between circuit and device design, as will be seen in later chapters. A thorough understanding of the influence of device fabrication on device characteristics is essential.

Chapter 2 is concerned with the technology of IC fabrication and is largely descriptive. Two lectures on this material should suffice if the students are assigned to read the chapter.

Chapter 3 deals with the characteristics of elementary transistor connections. The material on one-transistor amplifiers should be review for students at the senior and graduate level, and can be assigned as reading. The section on two-transistor amplifiers can be touched on lightly and assigned as reading. The section on emitter-coupled pairs is most important and should be covered in full in class, requiring two to three hours. If time allows, the material on JFET source-coupled pairs or on offset voltage and current can be covered.

In Chapter 4 the important topics of current sources and active loads are considered. These configurations are basic building blocks in modern analog IC design and this material should be covered in full with the exception of the appendices.

Chapter 5 is concerned with output stages and methods of delivering output power to a load. Integrated-circuit realizations of Class A, Class B, and Class AB output stages are described, as well as methods of output-stage protection. A selection of topics from this chapter should be covered.

Chapter 6 deals with operational-amplifier design. As an illustrative example the dc and ac analysis of the 741 operational amplifier (op amp) is performed in detail and the limitations of this basic op amp are described. The design of op amps with improved characteristics is then considered, leading to a discussion of JFET and super-β input stages. The material in this chapter up to Section 6.4 should be covered.

In Chapter 7 the frequency response of ICs is considered. The zero-value time constant technique is introduced for the calculation of the -3-dB frequency of complex circuits. The material of this chapter should be covered in full.

Chapter 8 describes the analysis of feedback circuits and should be covered in full with the section on voltage regulators assigned as reading.

Chapter 9 deals with the frequency response and stability of feedback circuits and should be covered up to the section on root locus. Time does not permit a detailed discussion of root locus but some introduction to this topic can be given.

In a 10-week quarter, coverage of the above material leaves only one week for Chapters 10 and 11. A selection of topics from these chapters can be chosen as follows. Chapter 10 deals with nonlinear analog circuits and portions of this chapter up to Section 10.3 could be covered in a first course. Chapter 11 is a comprehensive treatment of noise in integrated circuits and material up to and including Section 11.4 is suitable.

The material in this book has been greatly influenced by our association with Professor D. O. Pederson of the University of California, Berkeley, and we acknowledge his contributions. Ms. Bettye Fuller and Mrs. Marie Carey typed the manuscript and we appreciate their outstanding work.

Berkeley, California, 1977

Paul R. Gray
Robert G. Meyer

CONTENTS

CHAPTER 1

MODELS FOR INTEGRATED-CIRCUIT ACTIVE DEVICES

1.1 INTRODUCTION

The analysis and design of integrated circuits depend heavily on the utilization of suitable models for integrated-circuit components. This is true in hand analysis, where fairly simple models are generally used, and in computer analysis, where more complex models are encountered. Since any analysis is only as accurate as the model used, it is essential that the circuit designer have a thorough understanding of the origin of the models commonly utilized and the degree of approximation involved in each.

This chapter deals with the derivation of large-signal and small-signal models for integrated-circuit devices. The treatment begins with a consideration of the properties of *pn* junctions, which are basic parts of most integrated-circuit elements. Since this book is primarily concerned with circuit analysis and design, no attempt has been made to produce a comprehensive treatment of semiconductor physics. The emphasis is on summarizing the basic aspects of semiconductor-device behavior and indicating how these can be modeled by equivalent circuits.

1.2 DEPLETION REGION OF A *pn* JUNCTION

The properties of reverse-biased *pn* junctions have an important influence on the characteristics of many integrated-circuit components. For example, in conventional integrated-circuit technology all elements are isolated by reverse-biased *pn* junctions, and these junctions contribute a voltage-dependent parasitic capacitance to each element. In addition a number of important characteristics of bipolar transistors, such as breakdown voltage and output resistance, depend directly on the properties of the depletion region of a reverse-biased *pn* junction. Finally, the basic operation of the junction field-effect transistor is controlled by the width of the depletion region of a *pn* junction. Because of its importance and application to many different problems, an analysis of the depletion region of a reverse-biased *pn* junction is considered below. The properties of forward-biased *pn* junctions are treated in Section 1.3 when bipolar-transistor operation is described.

Consider a *pn* junction under reverse bias as shown in Fig. 1.1. Assume *constant doping densities* of N_D atoms/cm^3 in the *n*-type material and N_A atoms/cm^3 in the

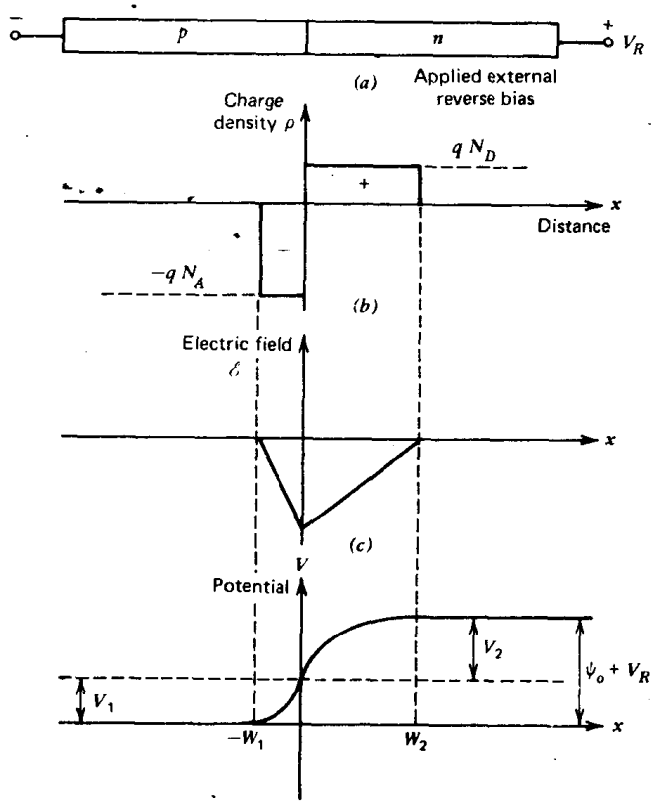

Figure 1.1 The abrupt junction under reverse bias V_R. (*a*) Schematic. (*b*) Charge density. (*c*) Electric field. (*d*) Electrostatic potential.

p-type material. (The characteristics of junctions with nonconstant doping densities will be described later.) Due to the difference in carrier concentrations in the *p*-type and *n*-type regions, there exists a region at the junction where the mobile holes and electrons have been removed, leaving the fixed acceptor and donor ions. Each acceptor atom carries a negative charge and each donor atom carries a positive charge so that the region near the junction is one of significant space charge and resulting high electric field. This is called the *depletion* region or *space-charge* region. It is assumed that the edges of the depletion region are sharply defined as shown in Fig. 1.1, and this is a good approximation in most cases.

For zero applied bias, there exists a voltage ψ_0 across the junction called the *built-in potential*. This potential opposes the diffusion of mobile holes and electrons across the junction in equilibrium and has a value[1]

$$\psi_0 = V_T \ln \frac{N_A N_D}{n_i^2} \tag{1.1}$$

where $$V_T = \frac{kT}{q} \simeq 26 \text{ mV at } 300°\text{K}$$

The quantity n_i is the intrinsic carrier concentration in a pure sample of the semiconductor and $n_i \simeq 1.5 \times 10^{10}$ cm^{-3} at 300°K for silicon.

In Fig. 1.1 the built-in potential is augmented by the applied reverse bias, V_R, and the total voltage across the junction is $(\psi_0 + V_R)$. If the depletion region penetrates a distance W_1 into the p-type region and W_2 into the n-type region then we require

$$W_1 N_A = W_2 N_D \tag{1.2}$$

because the total charge per unit area on either side of the junction must be equal in magnitude but opposite in sign.

Poisson's equation in one dimension requires that

$$\frac{d^2V}{dx^2} = -\frac{\rho}{\epsilon} = \frac{qN_A}{\epsilon} \quad \text{for} \quad -W_1 < x < 0 \tag{1.3}$$

where ρ is the charge density, q is the electron charge (1.6×10^{-19} coulomb), and ϵ is the permittivity of the silicon (1.04×10^{-12} farad/cm). The permittivity is often expressed as

$$\epsilon = K_S \epsilon_0 \tag{1.4}$$

where K_S is the dielectric constant of silicon and ϵ_0 is the permittivity of free space (8.86×10^{-14} farad/cm). Integration of (1.3) gives

$$\frac{dV}{dx} = \frac{qN_A}{\epsilon} x + C_1 \tag{1.5}$$

where C_1 is a constant. However the electric field $\mathscr{E}$ is given by

$$\mathscr{E} = -\frac{dV}{dx} = -\left(\frac{qN_A}{\epsilon} x + C_1\right) \tag{1.6}$$

Since there is zero electric field outside the depletion region, a boundary condition is

$$\mathscr{E} = 0 \quad \text{for} \quad x = -W_1$$

and use of this condition in (1.6) gives

$$\mathscr{E} = -\frac{qN_A}{\epsilon}(x + W_1) = -\frac{dV}{dx} \quad \text{for} \quad -W_1 < x < 0 \tag{1.7}$$

Thus the dipole of charge existing at the junction gives rise to an electric field that varies linearly with distance.

Integration of (1.7) gives

$$V = \frac{qN_A}{\epsilon}\left(\frac{x^2}{2} + W_1 x\right) + C_2 \tag{1.8}$$

If the zero for potential is arbitrarily taken to be the potential of the neutral p-type region, then a second boundary condition is

$$V = 0 \quad \text{for} \quad x = -W_1$$

and use of this in (1.8) gives

$$V = \frac{qN_A}{\epsilon}\left(\frac{x^2}{2} + W_1 x + \frac{W_1^2}{2}\right) \quad \text{for} \quad -W_1 < x < 0 \tag{1.9}$$

At $x = 0$, we define $V = V_1$ and then (1.9) gives

$$V_1 = \frac{qN_A}{\epsilon}\frac{W_1^2}{2} \tag{1.10}$$

If the potential difference from $x = 0$ to $x = W_2$ is V_2, then it follows that

$$V_2 = \frac{qN_D}{\epsilon}\frac{W_2^2}{2} \tag{1.11}$$

and thus the total voltage across the junction is

$$\psi_0 + V_R = V_1 + V_2 = \frac{q}{2\epsilon}\left(N_A W_1^2 + N_D W_2^2\right) \tag{1.12}$$

Substitution of (1.2) in (1.12) gives

$$\psi_0 + V_R = \frac{qW_1^2 N_A}{2\epsilon}\left(1 + \frac{N_A}{N_D}\right) \tag{1.13}$$

From (1.13), the penetration of the depletion layer into the p-type region is

$$W_1 = \left[\frac{2\epsilon(\psi_0 + V_R)}{qN_A\left(1 + \frac{N_A}{N_D}\right)}\right]^{1/2} \tag{1.14}$$

Similarly

$$W_2 = \left[\frac{2\epsilon(\psi_0 + V_R)}{qN_D\left(1 + \frac{N_D}{N_A}\right)}\right]^{1/2} \tag{1.15}$$

Equations 1.14 and 1.15 show that the depletion regions extend into the p-type and n-type regions in *inverse* relation to the impurity concentrations and in proportion to $\sqrt{\psi_0 + V_R}$. If either N_D or N_A is much larger than the other, the depletion region exists almost entirely in the *lightly doped* region.

EXAMPLE

An abrupt *pn* junction in silicon has doping densities $N_A = 10^{15}$ atoms/cm^3 and $N_D = 10^{16}$ atoms/cm^3. Calculate the junction built-in potential, the depletion-layer depths and the maximum field with 10 V reverse bias.

From (1.1)

$$\psi_0 = 26 \ln \frac{10^{15} \times 10^{16}}{2.25 \times 10^{20}} \text{mV} = 638 \text{ mV at } 300°\text{K}$$

From (1.4) the depletion-layer depth in the p-type region is

$$W_1 = \left(\frac{2 \times 1.04 \times 10^{-12} \times 10.64}{1.6 \times 10^{-19} \times 10^{15} \times 1.1} \right)^{1/2} = 3.5 \times 10^{-4} \text{ cm}$$

$$= 3.5\ \mu \text{ (where } 1\ \mu = 1 \text{ micron} = 10^{-6} \text{ m)}$$

The depletion-layer depth in the more heavily doped n-type region is

$$W_2 = \left(\frac{2 \times 1.04 \times 10^{-12} \times 10.64}{1.6 \times 10^{-19} \times 10^{16} \times 11} \right)^{1/2} = 0.35 \times 10^{-4} \text{ cm} = 0.35\ \mu$$

Finally, from (1.7) the maximum field that occurs for $x = 0$ is

$$\mathscr{E}_{\max} = -\frac{qN_A}{\epsilon} W_1 = -1.6 \times 10^{-19} \times \frac{10^{15} \times 3.5 \times 10^{-4}}{1.04 \times 10^{-12}}$$

$$= -5.4 \times 10^4 \text{ V/cm}$$

Note the large magnitude of this electric field.

1.2.1 Depletion-Region Capacitance

Since there is a *voltage-dependent charge* Q associated with the depletion region we can calculate a small-signal capacitance, C_j, as follows

$$C_j = \frac{dQ}{dV_R} = \frac{dQ}{dW_1} \frac{dW_1}{dV_R} \tag{1.16}$$

Now
$$dQ = AqN_A\,dW_1 \tag{1.17}$$

where A is the cross-sectional area of the junction. Differentiation of (1.14) gives

$$\frac{dW_1}{dV_R} = \left[\frac{\epsilon}{2qN_A\left(1 + \dfrac{N_A}{N_D}\right)(\psi_0 + V_R)}\right]^{1/2} \tag{1.18}$$

Use of (1.17) and (1.18) in (1.16) gives

$$C_j = A\left[\frac{q\epsilon N_A N_D}{2(N_A + N_D)}\right]^{1/2} \frac{1}{\sqrt{\psi_0 + V_R}} \tag{1.19}$$

The above equation was derived for the case of reverse bias V_R applied to the diode. However it is valid for positive bias voltages as long as the forward current flow is small. Thus, if V_D represents the bias on the junction (positive for forward bias, negative for reverse bias), then (1.19) can be written as

$$C_j = A\left[\frac{q\epsilon N_A N_D}{2(N_A + N_D)}\right]^{1/2} \frac{1}{\sqrt{\psi_0 - V_D}} \tag{1.20}$$

$$= \frac{C_{j0}}{\sqrt{1 - \dfrac{V_D}{\psi_0}}} \tag{1.21}$$

where C_{j0} is the value of C_j for $V_D = 0$.

Equations 1.20 and 1.21 were derived using the assumption of constant doping in the p-type and n-type regions. However many practical diffused junctions more closely approach a *graded* doping profile as shown in Fig. 1.2. In this case a similar calculation yields

$$C_j = \frac{C_{j0}}{\sqrt[3]{1 - \dfrac{V_D}{\psi_0}}} \tag{1.22}$$

Note that both (1.21) and (1.22) predict values of C_j approaching infinity as V_D approaches ψ_0. However the current flow in the diode is then appreciable and the equations no longer valid. A more exact analysis[2,3] of the behavior of C_j as a function of V_D gives the result shown in Fig. 1.3. For forward bias voltages up to

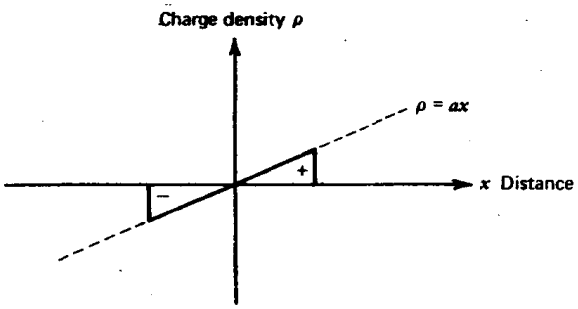

Figure 1.2 Charge density versus distance in a graded junction.

about $\psi_0/2$ the values of C_j predicted by (1.21) are very close to the more accurate value. As an approximation, some computer programs approximate C_j for $V_D > \psi_0/2$ by a linear extrapolation of (1.21) or (1.22).

EXAMPLE

If the zero-bias capacitance of a diffused junction is 3 pF and $\psi_0 = 0.5$ V, calculate the capacitance with 10 V reverse bias. Assume the doping profile can be approximated by an abrupt junction.

From (1.21)

$$C_j = \frac{3}{\sqrt{1 + \dfrac{10}{0.5}}}\text{pF} = 0.65\text{ pF}$$

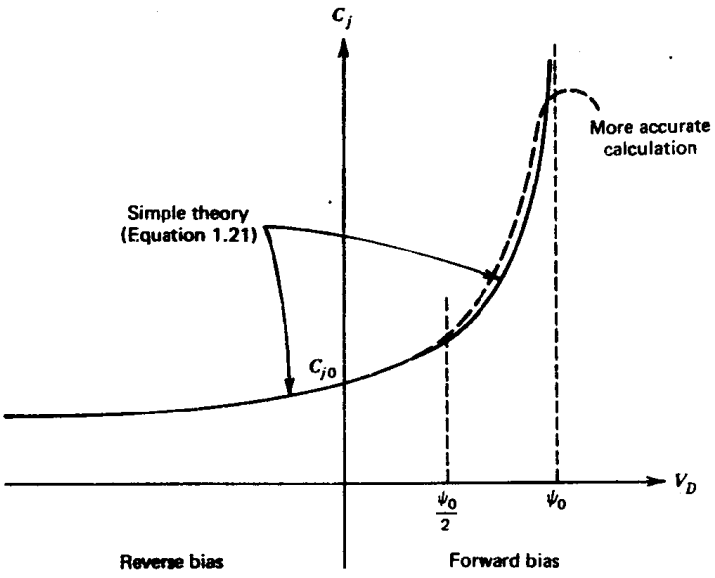

Figure 1.3 Behavior of *pn* junction depletion-layer capacitance C_j as a function of bias voltage V_D.