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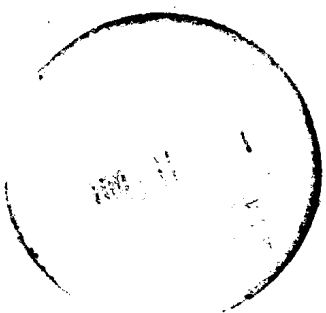
D. ROY CHOUDHURY
SHAIL JAIN



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PREFACE

The term *Integrated Circuit* (IC) reflects the capabilities of semiconductor industry to fabricate complex electronic circuit consisting of a large number of components on a single substrate. The operational amplifier or op-amp is the most versatile active element amongst linear ICs. The present text covers the design and application of op-amp and other linear ICs. The emphasis is on the fundamental design concepts. The book is intended for undergraduate students of Electronics, Electrical, Computer, Control and Instrumentation engineering. The text has evolved from the lecture notes prepared by the authors for linear integrated circuit course over the years.

This book presents the widely used op-amp IC741 and other linear ICs such as 555 (timer), 565 (phase locked loop), regulated power supply IC chips, the switched mode power supply, active filters, switched capacitor filters, D/A and A/D converters. Besides this, IC fabrication technology has been discussed to give better insight of the linear ICs commonly used. It gives better understanding of the functions of operations and limitations of different ICs and their remedies. Each chapter contains examples to support the main topic in the text. The laboratory experiments at the end of each chapter demonstrate the use and operation of the ICs described. IC number, pin configuration, data sheet for important ICs have been given.

Chapter 1 introduces the fundamentals of IC fabrication technology. Various processes used in silicon planar technology are discussed in detail. Brief aspects of thick and thin film technology are given. MOSFET fabrication technique is also discussed. Chapter 2 introduces the basic principles of an op-amp: packages, pin configuration, power supply connections etc. The various configurations, such as inverting, non-inverting and differential mode of operation are described. Great emphasis has been made on the internal circuitry of commonly used op-amp ICs. Various blocks such as difference amplifier, current mirror, active load, level shifter and output stage are described. The dc and ac characteristics of an op-amp are described in Chapter 3. The dc characteristics such as input offset current, input offset voltage, bias current are explained. The ac characteristics, that is, frequency response and the effect of slew rate on the performance of op-amp has been explained. Various compensating techniques have also been discussed. Interpretation of important parameters in the data sheet is also featured in this Chapter.

A number of linear and nonlinear applications of operational amplifier such as adder, subtractor, integrator, differentiator, instrumentation amplifier, log/antilog amplifiers, multiplier, divider, analog computation techniques, clipper/clamper, sample and hold circuit are presented in Chapter 4. The various comparators—square, triangular and sine wave generators are discussed in Chapter 5. Chapter 6 deals with voltage regulator chips—fixed regulator, variable voltage regulator and switched mode power supply.

Active filters—low pass, high pass, band pass, band reject and state variable filters are discussed in Chapter 7. Switched capacitor filter and its realization are also described. Chapter 8 is devoted to 555-timer and its various applications. The phase locked loop-565, an important linear IC which is very useful in communications has been discussed in Chapter 9 with its detailed applications. In Chapter 10, the various analog to digital (A/D) and digital to analog (D/A) techniques are presented.

We wish to acknowledge a large number of students and colleagues who have contributed to this book. Thanks to Mr. Manav Sen of Solid State Physics Laboratory and Dr. B. Kumar of Delhi Institute of Technology for their valuable suggestions.

Our family members deserve very special thanks for their continued support, encouragement and patience throughout this project.

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CONTENTS

CHAPTER 1

INTEGRATED CIRCUIT FABRICATION

1.1. Introduction

We are going through a period of micro-electronic revolution. For a common person, the role of electronics is limited to audio-visual gadgets like radio and television, but the truth is, today the growth of any industry like communication, control, instrumentation or computer, is dependent upon electronics to a great extent. And integrated circuits are electronics.

The integrated circuit or IC is a miniature, low cost electronic circuit consisting of active and passive components that are irreparably joined together on a single crystal chip of silicon. Most of the components used in ICs are not similar to conventional components in appearance although they perform similar electrical functions. In this chapter, we describe the basic processes used in the fabrication of integrated circuits. Both bipolar and MOS fabrication are treated. These circuits naturally offer a number of distinct advantages over those made by interconnecting discrete components. These may be listed as follows:

1. Miniaturization and hence increased equipment density
2. Cost reduction due to batch processing
3. Increased system reliability due to elimination of soldered joints
4. Improved functional performance (as it is possible to fabricate even complex circuits for better characteristics)
5. Matched devices
6. Increased operating speeds (due to the absence of parasitic capacitance effect)
7. Reduction in power consumption.

1.2. Classification

Integrated circuits offer a wide range of applications and could be broadly classified as:

Digital ICs

Linear ICs

Based upon the above requirements, two distinctly different IC technologies

namely, Monolithic technology and Hybrid technology have been developed.

In monolithic integrated circuits, all circuit components, both active and passive elements and their interconnections are manufactured into or on top of a single chip of silicon. The monolithic circuit is ideal for applications where identical circuits are required in very large quantities and hence provides lowest per-unit cost and highest order of reliability. In hybrid circuits, separate component parts are attached to a ceramic substrate and interconnected by means of either metallization pattern or wire bonds. This technology is more adaptable to small quantity custom circuits. Based upon the active devices used, ICs can be classified as bipolar (using BJT) and unipolar (using FET). Bipolar and unipolar ICs may further be classified depending upon the isolation technique or type of FET used as in Fig. 1.1.

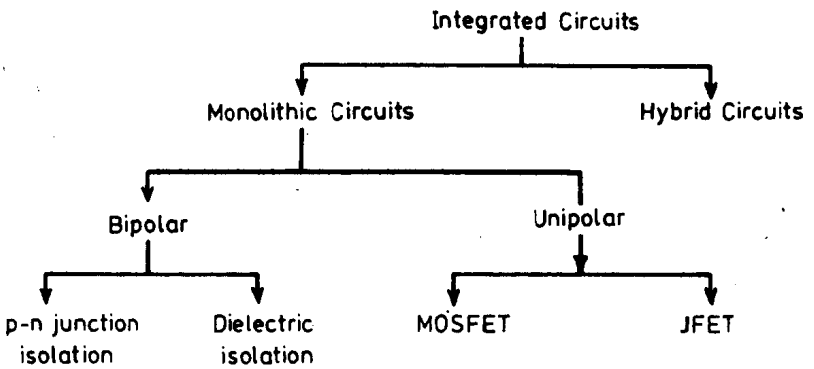

Fig. 1.1. Classification of ICs

1.3. IC Chip Size and Circuit Complexity

The first transistor was a Germanium alloy junction transistor, developed in the year 1948. Silicon devices came up in the mid-to-late 1950s and the concept of integrated circuit was introduced in early 1960s by both Texas Instruments and Fairchild Semiconductors. Since that time, the size and complexity of ICs have increased rapidly as shown by the following brief chronology.

Invention of transistor (Ge)	1948
Development of Silicon transistor	1955–1959
Silicon Planar technology	1959
First ICs, Small Scale Integration (SSI), 3 to 30 gates/chip	1960
Medium Scale Integration (MSI) 30 to 300 gates/chip	1965–1970

Large Scale Integration (LSI) 300 to 3000 gates/chip	1970–1975
Very Large Scale Integration (VLSI) more than 3000 gates/chip	1975
First Commercial VLSI chip: 64k RAM	late 1970s
256k RAM	early 1980s
512k RAM, 1M ROM, very high speed GaAs ICs, "Three dimensional" (Multilayer) ICs, Silicon-on-insulator technology	Middle 1980s

Over the years, the device density has increased together with some increase in the chip area. Figure 1.2 (a, b, c) show small (SSI), medium (MSI) and large (LSI or VLSI) IC chip size. The chip areas range from 1 mm^2 (1600 mil^2)* for the SSI chip to 1 cm^2 (160,000 mil^2) for the LSI chip.

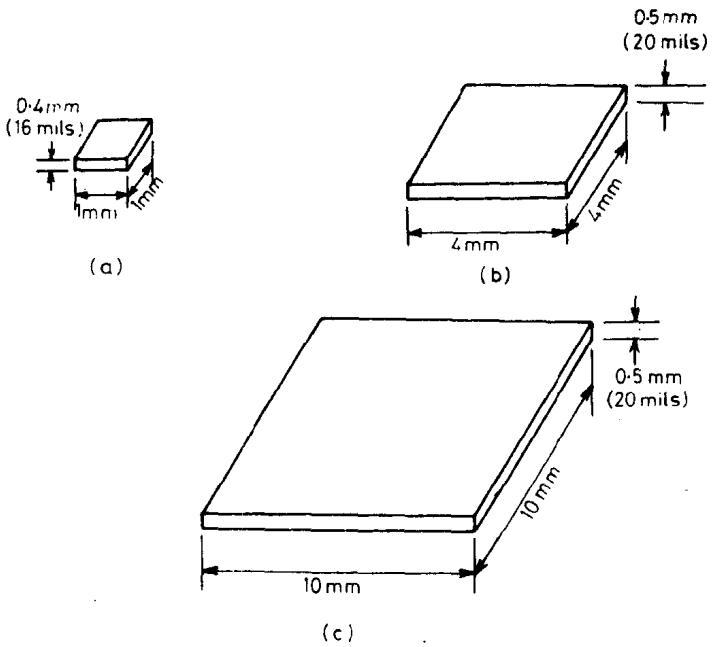

Fig. 1.2. Integrated circuit chips (a) SSI chip (b) MSI chip (c) LSI or VLSI chip

1.4. Fundamentals of Monolithic IC Technology

A monolithic circuit, literally speaking, means a circuit fabricated from a single stone or a single crystal. The origin of the word 'monolithic' is from the Greek

*1 mil = 0.001 in = 25.4 μm = 0.0254 mm

word *monos* meaning 'single' and *lithos* meaning 'stone'. So monolithic integrated circuits are, in fact, made in a single piece of single crystal silicon.

The most significant advantage of integrated circuit of reducing the cost of production of electronic circuits due to batch production can be easily visualized by a simple example. A standard 10 cm diameter wafer can be divided into approximately 8000 rectangular chips of sides 1 mm. Each IC chip may contain as few as tens of components to several thousand components. And if 10 such wafers are processed in one batch, we can make 80,000 ICs simultaneously. Many chips so produced will be faulty due to imperfection in the manufacturing process. Even if the yield (percentage of fault free chips/wafer) is only 20 percent, it can be seen that 16,000 good chips are produced in a single batch.

The fabrication of discrete devices such as transistor, diode or an integrated circuit in general can be done by the same technology. The various processes usually take place through a single plane and therefore, the technology is referred to as planar technology. A simple circuit of Fig. 1.3 when fabricated by silicon planar technology will have the cross-sectional view shown in Fig. 1.4.

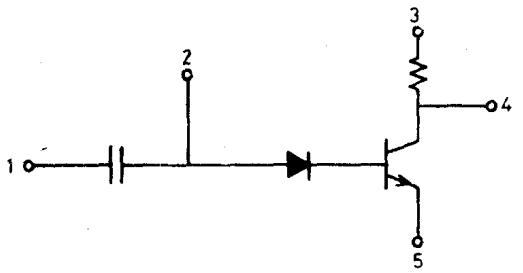

Fig. 1.3. A typical circuit

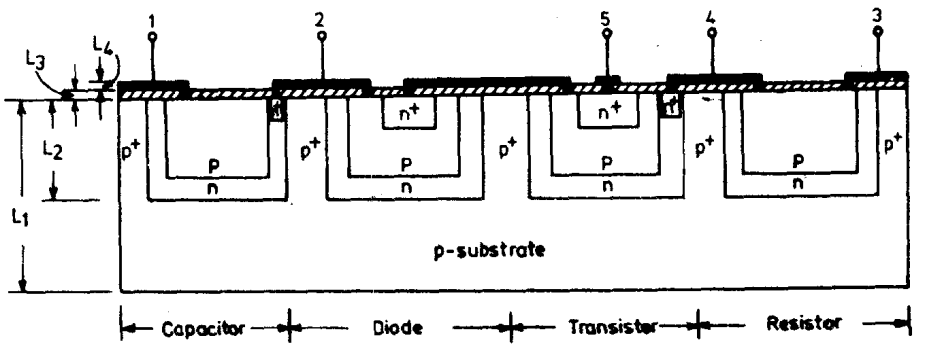

Fig. 1.4. Complete cross-sectional view of the circuit in Fig. 1.3 when transformed into monolithic form

An IC in general, consists of four distinct layers, as follows:

Layer No.1 (~ 400 μm)	is a p-type silicon substrate upon which the integrated circuit is fabricated.
Layer No.2 (~ 5–25μm)	is a thin n-type material grown as a single crystal extension of the substrate using epitaxial deposition technique. All active and passive components are fabricated within this layer using selective diffusion of impurities.
Layer No. 3 (0.02–2μm)	is a very thin SiO_2 layer for preventing diffusion of impurities wherever not required using photolithographic technique.
Layer No. 4 (~ 1μm)	is an aluminium layer used for obtaining interconnection between components.

It may be pointed out that the drawings showing the cross-sectional view in this chapter are never scale drawings, but are distorted for the particular emphasis required.

1.5. Basic Planar Processes

The basic processes used to fabricate ICs using silicon planar technology can be categorised as follows:

1. Silicon wafer (substrate) preparation
2. Epitaxial growth
3. Oxidation
4. Photolithography
5. Diffusion
6. Ion implantation
7. Isolation technique
8. Metallization
9. Assembly processing and packaging

We shall now describe these processes in detail.

1.5.1. Silicon Wafer Preparation

The following steps are used in the preparation of Si-wafers.

1. Crystal growth and doping
2. Ingot trimming and grinding
3. Ingot slicing
4. Wafer polishing and etching
5. Wafer cleaning

The starting material for crystal growth is highly purified (99.99999) polycrystalline silicon. The Czochralski crystal growth process is the most often

used for producing single crystal silicon ingots. The polycrystalline silicon together with an appropriate amount of dopant is put in a quartz crucible and is then placed in a furnace. The material is then heated to a temperature in excess of the silicon melting point of 1420°C. A small single crystal rod of silicon called a seed crystal is then dipped into the silicon-melt and slowly pulled out as shown in Fig. 1.5. As the seed crystal is pulled out of the melt, it brings with it a solidified mass of silicon with the same crystalline structure as that of seed crystal. During the crystal pulling process, the seed crystal and the crucible are rotated in opposite directions in order to produce ingots of circular cross-section. The diameter of the ingot is controlled by the pulling rate and the melt temperature. Ingot diameter of about 10 to 15 cm is common and ingot length is generally of the order of 100 cm.

Next the top and bottom portions of the ingot are cut off and the ingot surface is ground to produce an exact diameter (D = 10, 12.5, 15 cm). The ingot is also ground flat slightly along the length to get a reference plane. The ingot is then

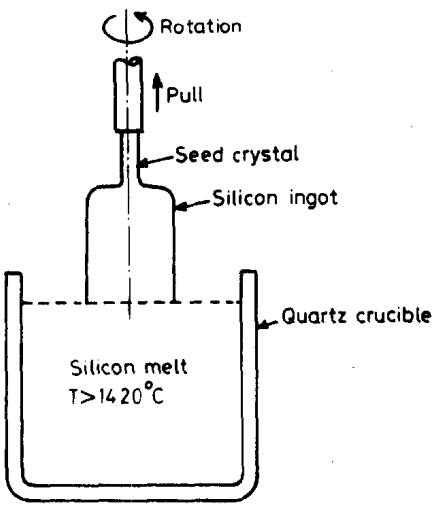

Fig. 1.5. Czochralski crystal growth

sliced using a stainless steel saw blade with industrial diamonds embedded into the inner diameter cutting edge. This produces circular wafers or slices as shown in Fig. 1.6. The orientation flat portion serves as a useful reference plane for the various processes described later. The silicon wafers so obtained have very rough surface due to slicing operation. These wafers undergo a number of polishing steps to produce a flat surface. Then one side of the wafer is given a final mirror-smooth highly polished finish, whereas the other side is simply lapped on an abrasive lapping machine to obtain an acceptable degree of flatness. Finally, the wafers are thoroughly rinsed and dried. A raw cut slice of thickness 23-40 mils

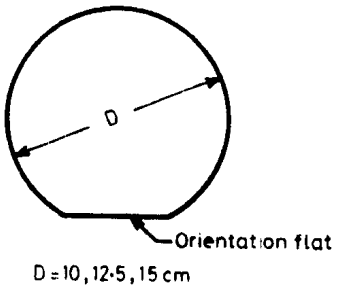

Fig. 1.6. Silicon wafer, D = 10, 12.5, 15 cm showing flat orientation

produces wafers of 16-32 mils thickness after all the polishing steps.

These silicon wafers will contain several hundred rectangular chips, each one containing a complete integrated circuit. After all the IC fabrication processes are complete, these wafers are sawed into 100 to 8000 rectangular chips having side of 10 to 1 mm. Each chip is a single IC and may contain hundreds of components. The wafer thickness therefore is so chosen that it is possible to separate chips without breaking and at the same time, it gives sufficient mechanical strength to the IC chip.

1.5.2. Epitaxial Growth

The word epitaxy is derived from Greek word *epi* meaning 'upon' and the past tense of the word *teinon* meaning 'arranged'. So, one could describe epitaxy as, arranging atoms in single crystal fashion upon a single crystal substrate, so that the resulting layer is an extension of the substrate crystal structure.

The basic chemical reaction used for the epitaxial growth of pure silicon is the hydrogen reduction of silicon tetrachloride.

$$SiCl_4 + 2H_2 \overset{1200°C}{\rightleftharpoons} Si + 4HCl$$

Mostly, epitaxial films with specific impurity concentration are required. This is accomplished by introducing phosphine (PH_3) for the n-type and bi-borane (B_2H_6) for p-type doping into the silicon-tetrachloride hydrogen gas stream.

The process is carried out in a reaction chamber consisting of a long cylindrical quartz tube encircled by an RF induction coil. Figure 1.7 shows the diagrammatic representation of the system used. The silicon wafers are placed on a rectangular graphite rod called a boat. This boat is then placed in the reaction chamber where the graphite is heated inductively to a temperature 1200°C. The various gases required for the growth of desired epitaxial layers are introduced into the system through a control console.

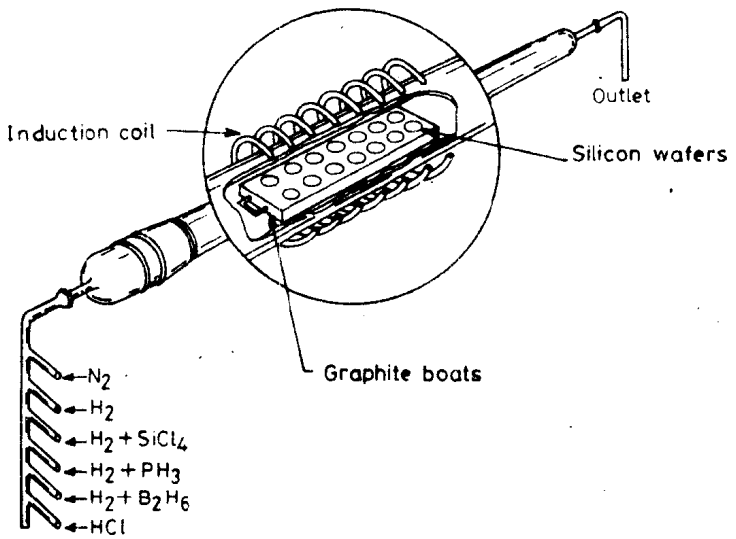

Fig. 1.7. A diagrammatic representation of a system for growing silicon epitaxial films

1.5.3. OXIDATION

SiO_2 has the property of preventing the diffusion of almost all impurities through it. It serves two very important purposes.

1. SiO_2 is an extremely hard protective coating and is unaffected by almost all reagents except hydrofluoric acid. Thus it stands against any contamination.

2. By selective etching of SiO_2, diffusion of impurities through carefully defined windows in the SiO_2 can be accomplished to fabricate various components.

The silicon wafers are stacked up in a quartz boat and then inserted into quartz furnace tube. The Si-wafers are raised to a high temperature in the range of 950 to 1150°C and at the same time, exposed to a gas containing O_2 or H_2O or both. The chemical reaction is

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2$$

This oxidation process is called thermal oxidation because high temperature is used to grow the oxide layer. The thickness of the film is governed by time, temperature and the moisture content. The thickness of oxide layer is usually in the order of 0.02 to 2 μm.