Choosing and Using CMOS

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Preface

Welcome to *Choosing and Using CMOS*. Obviously you have some requirement to learn more about Complementary Metal Oxide Silicon technology. Whether you are taking your first steps into this subject or simply wish to expand your knowledge, this book should be of great relevance.

Unlike conventional technical books, the data covered here does not originate from just one or two authors; rather, contributions have been solicited from many of the major semiconductor manufacturers and users of CMOS. Thus the subject matter represents a variety of views and many different presentation styles. Every effort has been made, however, to incorporate each contribution within a clearly defined overall structure so that data is neither duplicated nor contradicted and flows from chapter to chapter. Although occasions do arise where similar technical areas are covered in two different chapters, the treatment and presentation will be sufficiently different that one writer's approach complements another's.

Topics covered represent current information on the wide variety of devices and techniques where CMOS may be utilised. The contents should be pertinent to student, engineer and engineering manager alike. Of particular importance, I believe, is the study of semicustom and custom techniques, since increasingly the trend is towards complete system integration wherever achievable. The approach required when designing with this eventual target in mind differs from conventional techniques in many ways and to this end a section of the book not only contains items which detail these differences but also investigates some actual casebook examples, indicating the type of difficulties which may be encountered.

Although the nature of the book is essentially technical, some

information has been included on the financial and timespan implications of the different technological approaches. This data will be particularly important to those about to embark upon a design exercise with a technique that may be unfamiliar. It should of course be noted that this information is current only at the time of going to press and only represents an order of magnitude since inevitably every design is different in terms of complexity, quantities required, etc. and every manufacturer will have different cost and timescales.

Why another book about CMOS? Most of the data that exists on this subject is contained within data sheets and manuals provided by manufacturers engaged in some aspect of the fabrication or use of CMOS devices of one form or another. This being the case, it would require a great deal of effort to collect information pertaining to the entire field and extract the relevant portions. Much of that work has been performed by the individual authors who have contributed to this volume.

Mike Walsh

Contents

CHAPTER 1

An introduction to choosing and using CMOS

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Where did it all start? Although one can trace the birth of electronics back as far as the discovery of an 'unusual electrical effect' within the first carbon filament lamps developed by Thomas Edison and later (1903) explained as the theory of thermionic emission by Richardson, the inception of solid state electronics and devices is a far more recent event.

The discovery and use of the crystal set where the point contact between certain crystalline materials and a fine wire provided a rectifying action could be considered the landmark that pointed the way towards modern electronics. Although the action of these devices was not understood at the time, they were in fact constructed from materials which we know today as semiconductors.

Until 1948 these devices were used to provide a solid state means of rectification but there had been no success in building a structure which could provide amplification. In that year, however, two engineers working at Bell Laboratories in the United States, Jon Bardeen and Walter Brattain, invented the point contact transistor. This device utilised a small wafer of cystalline germanium on to the surface of which two wire contacts were positioned close together. One contact was referred to as the 'emitter' and the other as the 'collector'. A third contact made with a much larger area on the opposite side of the wafer was referred to as the 'base'. Variation of the base potential could be used to influence current flow from emitter to collector and thus provide an amplifying action. The junction transistor suffered the disadvantage that the currents that it could handle were extremely small, but although it was never developed beyond the laboratory it was of great importance in providing the experimental basis upon which William Shockley, a co-worker at

Bell Laboratories, developed the theory of junction transistors – a theory which proved to be extraordinarily accurate when practical devices were fabricated some two years later.

The electrical characteristics of semiconductors depend upon the regular crystal structures of certain materials. The most common such material used today is silicon. A member of the same chemical group as carbon, pure silicon crystals have a tightly bound molecular structure with no free electrons. However, if a small amount of impurity (often called 'dopant') is added the regular structure is upset and there is an excess of electrons available for conduction under the correct conditions. A material doped in this way is referred to as 'n-type', indicating that current is carried by the flow of electrons. If, however, the dopant material has an electronic structure that is short of electrons then the resultant material will have a deficit of electrons, each deficit being referred to as a 'hole'. Material of this sort is called 'p-type'.

Fuelled by the needs of defence programs, the acceleration in the growth of the electronics industry between 1950 and 1960 was dramatic. Continual innovation enhanced the quality of transistors and reduced their size while at the same time manufacturing techniques were rapidly being refined. During this period many new types of semiconductor device were developed, but the introduction of the integrated circuit must be acknowledged as the next major landmark in the electronics industry.

The first such integrated devices were of the bipolar type, leading very rapidly to the introduction of the 7400 family of components. Much research into the integration of field effect devices resulted in the construction of customised monolithic devices based around p-channel technology from the early 1960s. This research culminated in the introduction of a family of standard integrated circuit devices based on complementary MOS technology by several companies in the late 1960s.

CMOS is an important part of today's electronics technology and its many advantages and relatively few disadvantages mean that it has found application over a very wide area. Probably of prime importance is its extremely low power requirements in most operating conditions. Figure 1.1 shows the basic CMOS gate construction, the invertor. The p- and n-channel transistors can be considered in the ideal situation to act as perfect switches. When the control pin (gate) on the n-channel device is made

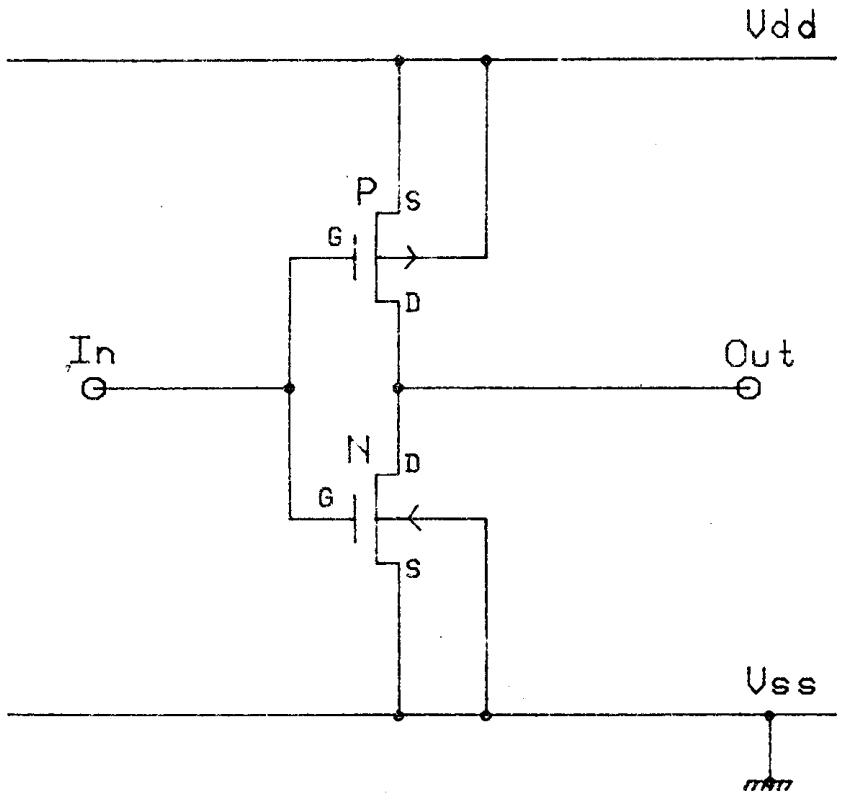

Fig. 1.1 The simple CMOS invertor.

positive with respect to its source it turns on, presenting a current path from source to drain. A similar action occurs when the gate of the p-device is made negative with respect to its source. Now, since both gates are connected together a positive voltage will turn on the n-device and turn off the p-device connecting the output terminal to 0 volts; when the input is held at 0 volts the p-channel transistor turns on and the n-device is held off, connecting the output termal to the positive voltage rail.

Two important features of this action should be noted. Firstly, the composite connection of the two transistors is acting like an invertor; when the input is a low voltage the output is a high voltage, and vice versa. Secondly, no current actually appears to flow to maintain this condition; when one transistor is 'on' the complementary transistor is 'off'. Although in a DC condition this is true (ignoring second order effects), current is required during the transition in order to charge and discharge the capacitances of other circuit connections.

Low power implies several things; not just that a circuit will consume little current but that the equipment supplying the power can be reduced, to such an extent in many cases that circuits may be powered for very long periods from very small batteries, e.g. wristwatches and calculators. But a reduction of current also relates to many other aspects that interest the engineer. Reliability increases as not so much stress is applied to the printed circuit board or to other components and heating effects are reduced, minimising the requirement to add cooling devices.

Low current capability is not the only thing that makes the use of CMOS attractive. Wide operating voltage contributes to both flexibility and reliability, with the stability requirements for power supplies being relaxed. The high noise immunity (that is, the ability to reject signals on inputs that are less than a certain threshold) of CMOS compared to other technologies makes it ideal for use in adverse electrical environments. Due to the insulated gate structure of the inputs to CMOS logic an extremely high input impedance is always associated with these devices. This aspect simplifies the tasks of interfacing other logic families and non-CMOS signals into the CMOS devices.

Of course, while every aspect of a particular technology may have its advantages nothing is perfect; there will always be associated disadvantages. Many of the early failings of CMOS technology have been addressed by the process of continual improvement. The first standard CMOS parts suffered from poor speed performances in comparison to TTL and the construction of the input circuitry provided little protection against damage from injected static charge, thus damage resulting from adverse handling was always possible. The mechanism known as 'latchup' was also not well understood. This effect, in which parasitic transistors making up the MOS structure could be induced to take up a stable state, effectively shorting the power rails until power was removed, at best caused functional failure of the circuit and at worst catastrophic failure of the device. In the main these problem areas have all now been addressed with a large degree of success. Processes have improved to the extent that modern CMOS circuits approach TTL in their operating speed capability. Protection networks are utilised to guard against spurious failure from electrostatic damage, and various approaches to the topological design of the MOS layout have been used to successfully solve latchup problems.

Outstanding problems for the CMOS technologist are to increase speed of operation even further, the main effort being directed towards techniques such as reduction of gate dimensions and thus the capacitance that limits performance; the use of more than one layer of metal interconnect to minimise the delays associated with time constants of interconnect; and also the development of new materials for fabrication rather than just silicon, for example 'silicon on sapphire' technology.

CMOS technology may be divided into three distinct areas when considering application and marketing. Of primary importance are the SSI/MSI families available from a wide variety of manufacturers. These devices form the 'building blocks' for a wide range of discrete design possibilities with newer, more complex devices constantly being added to the families.

A second series of CMOS devices are the LSI standard products. Predominant in this area are the requirements of the telecommunications industry where low power operation is often a prerequisite. Other devices in this group include large display drivers and DVM ICs.

The technology also plays an important role in the world of analogue conditioning and processing. The high input impedances and low power consumptions make CMOS ideal for the implementation of op amps, analogue-to-digital convertors and complex signal processing devices such as switched capacitor filters.

Lastly, probably one of the fastest growing technology areas is custom and semicustom integrated circuits. As indicated above, this technology is well suited to a number of engineering requirements and thus is widely used to implement the applications specific ICs required in so many areas of today's electronics industry. The complementary transistor structure is well suited to integration, with the characteristics of low power aiding the designer; thus a very large number of custom designs are performed in CMOS.

Another increasing trend is to implement microprocessor technology in CMOS. Significant advantages are once again offered by low power, including the important requirement of maintaining some or all random access memory in a low power condition while the main power supply is off. CMOS static memory techniques facilitate this.

With the movement towards implementation of customers' specific circuit requirements on to a single IC, an appreciation

and understanding of the techniques involved is becoming increasingly important. Although later chapters provide detailed introductions to these areas, it is useful to have an overview of the benefits and constraints of each of three approaches: gate arrays, standard cells and full-custom.

Gate array methodology allows circuits to be developed into integrated form most quickly and for least development cost since only one or two layers of metallisation are affected by the specific design. Thus prefinished wafers can be held in inventory and then very rapidly processed to the customer's requirements. The major disadvantage here is that, almost inevitably, the die size is larger than actually required, implying a higher production price as some silicon area cannot be utilised.

The standard cell approach has slightly more complexity attached to its design and a higher initial tooling cost, thus the initial expense of development is larger than for the method previously described. Production pricing is, however, lower since the die can be used more efficiently.

Lastly, full-custom design usually requires long development spans by highly experienced engineers and layout designers, and hence has high costs. However wasted silicon is minimised, reducing production price to a minimum.

Although many different factors will influence the decision on which technique is appropriate to a particular design, one major factor is always the trade-off between production volume and effective unit cost. Figure 1.2 shows a graph used universally to indicate these relationships. Although the scales and absolute values may differ, a graph of this kind can give a first order approximation to the best technique to be adopted.

Developmental work now going on in both existing manufacturers' R & D departments and in research institutions and universities gives some insight into the future evolution of CMOS technology. The prime push is towards smaller feature sizes which will allow more circuitry to be packed into the same area of silicon; halving the feature size more or less doubles the amount of circuit functions for a given area of silicon. Smaller geometries also provide enhanced performance, mainly in operating speed. Multiple metallisation levels also improve circuitry packing immensely since interconnect may be placed directly over active circuitry. Double metal technology of this type is now quite commonplace but theoretically it is possible to achieve three or four levels of interconnect. Of course, reducing

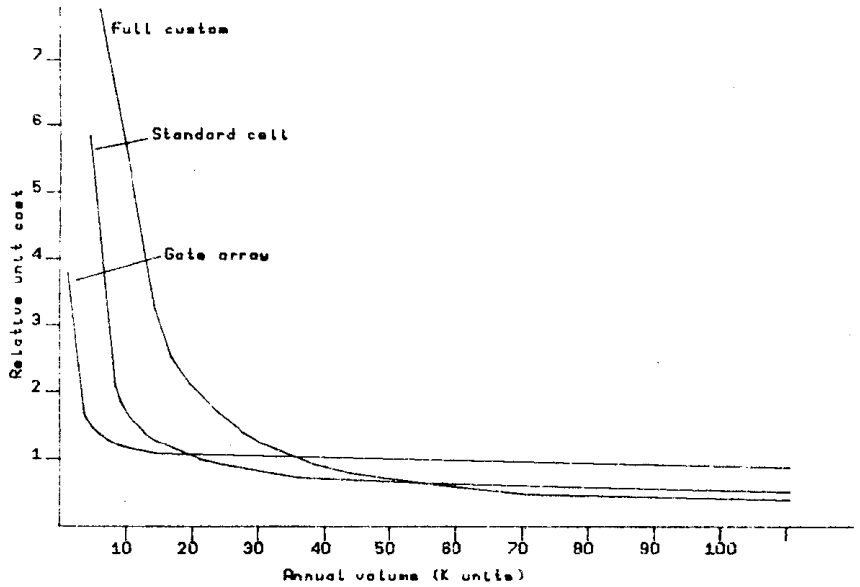

Fig. 1.2 Cost vs. volume for major custom design approaches.

physical geometries has more than just a mechanical effect on the semiconductor devices being fabricated. As channel lengths decrease, second order effects begin to influence the operation of the devices to the extent that their widely accepted and understood mechanisms of operation no longer hold true. Much research is currently proceeding to predict, measure and understand these behaviour modes.

Since it is not possible to reduce design rules continually, other approaches to improving design density are also being investigated. New circuit techniques such as the dynamic logic approach indicate the potential for integrating logic functions with all the advantages of CMOS but with a smaller investment in transistors. Of course nothing is ever 'for free' and these new circuit techniques do hold some traps for the unwary, primarily in the nature of higher design complexity. This comment leads nicely into another developmental area, that of computer aided design tools.

As the complexity of circuitry increases it is impractical, and is indeed becoming impossible, for engineers alone to control the number of variables involved in designing integrated systems; thus the ubiquitous computer has been a major tool in this industry. Software presently exists that can contribute

significantly to all aspects of the design of discrete and integrated circuits, but always the human eye and brain can outmatch the computer in certain areas. Much effort is thus being directed to methods of simulation (the emulation of the functional and timing operation of the circuit being designed, using a form of software modelling), automatic layout (the design of the physical layout, performed by a software package), and silicon compilers (automated layout from functional description of the circuit). Although the engineer's creative abilities are unlikely ever to be surpassed by the computer, increasing reliance is being placed in this area to optimise all design related aspects.

Of course CMOS may not be (and is certainly not at the moment) the 'be all and end all' of semiconductor technology. Development work continues into other areas, with bipolar technology still leading when very high speed operation is desired. N-channel technology is still able to match CMOS in many applications; power consumption is certainly not low but very efficient use can usually be made of silicon. Other approaches such as silicon on insulator (SOI) and gallium arsenide technologies have also been subject to evaluation and each has its own strong and weak characteristics.

CMOS has a vast and rapidly growing user base and a thorough grounding in this technology is therefore vital for today's designers and engineers. The following chapters will provide a valuable introduction and source of reference for such people.

CHAPTER 2

CMOS technology

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INTRODUCTION

The earliest CMOS processes, developed in the 1960s, employed aluminium as the gate conductor and were based on p-channel MOS technologies. Their complexity was such that circuits of only a few logic functions could be designed and fabricated. Process developments subsequently led to aluminium gates being replaced by polysilicon, with the benefit that sources and drains could be self-aligned to the gate electrode by dopant implantation. In recent years, fabrication technology has permitted entire electronic systems to be integrated within a single CMOS chip. Unlike some other process technologies, an additional degree of freedom exists for CMOS in the selection of substrate silicon; not only can n-type and p-type resistivities be used but there is also a choice of silicon on insulator substrate.

Advances in processing techniques have taken place so that wafer steppers, plasma etchers, low temperature deposition systems, the use of silicides and multi-metallisation have permitted minimum feature sizes to fall to around 1.5 microns and have increased both packing densities and circuit performance. The evolution of CMOS has by no means ended; new fabrication techniques and design methodologies are being developed to further increase circuit speed and complexity. The outcome will be that feature sizes will fall to sub-micron values, circuit packing densities will rise and CMOS circuit functional complexity will increase.

DESIGN RULES, CIRCUIT LAYOUT AND TRANSISTOR SYMBOLS

CMOS circuits are created from the design innovation which uses both n-channel and p-channel enhancement transistors to perform logic inversion. Such an invertor exploits the low off-state power dissipation from both transistor types since power is consumed only during a transition from one logic state to another.

A circuit is initially designed in terms of circuit symbols which represent electronic components such as transistors, resistors, capacitors and so on. This stage of the design defines the circuit function be it a logic, memory or analogue device. The next stage of the design is to convert all the individual circuit symbols into rectangular patterns which will become electronic components on the silicon chip. This conversion is made by reference to a set of design rules which determine the order for layers of insulators and conductors to be formed and patterned on wafers, their minimum sizes and the minimum distances allowable between them. The coordinates of these patterns are fed into a computer and stored on magnetic tape.

The use of computer aided design techniques has considerably speeded up the creation of circuit layouts by permitting blocks of circuitry to be permanently stored as cells and re-used in subsequent designs. On completion of the circuit design, the data tape is used in maskmaking to regenerate the same patterns on photographic masks. There are about eight to twelve such masking layers in a CMOS process, depending on its complexity. In addition to component sizes, the design rules define their electrical parameters. After completion of the design, masks are made for the circuit to be fabricated in silicon.

A simple design exercise is illustrated in fig. 2.1 which shows how transistors are arranged in a simple CMOS invertor. Figure 2.1(a) shows the conventional transistor symbols but for simplicity they are abbreviated to those in fig. 2.1(b) where the substrate and p-well connections are assumed to be present though not actually shown. Figure 2.1(c) shows a simplified silicon gate layout of the invertor and fig. 2.1(d) a cross-sectional diagram; the power supply connections are also shown. In CMOS circuits the bias on the V_{DD} rail is usually +5 V and 0 V on the V_{SS} rail although other voltages may sometimes be used. A similar cross-sectional diagram to the one in fig. 2.1(d) could be

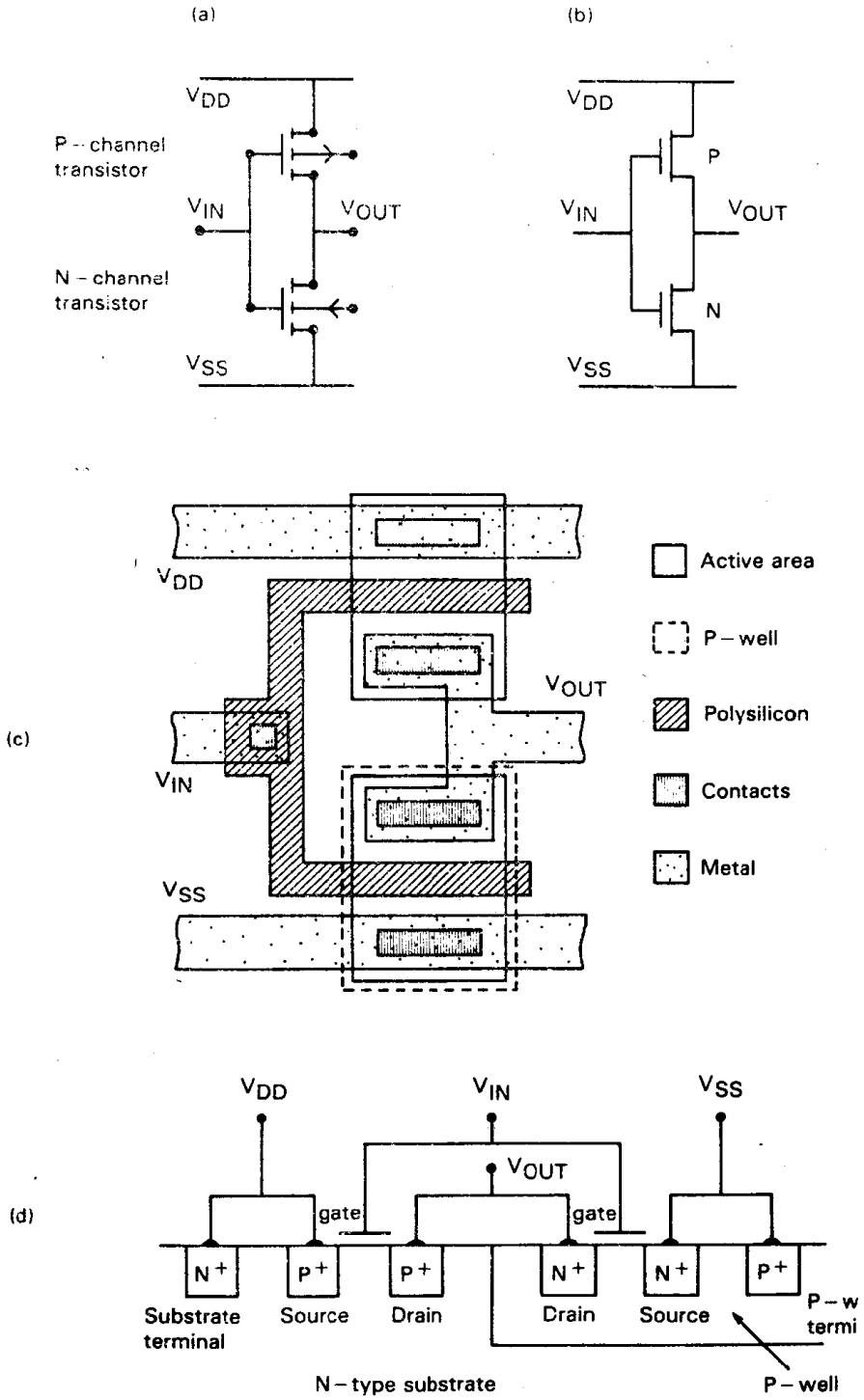

Fig. 2.1 Transistor symbols, silicon-gate layout and a cross-sectional diagram of a CMOS invertor.