MOS Device and Circuit Design

Oliver J. McCarthy

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*Senior Lecturer, Electronic Engineering,
National Institute for Higher Education,
Limerick, Republic of Ireland.*

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Preface

This book is emerging at a time when MOS/LSI has already brought about a revolution in the field of computing. It provides a comprehensive treatment of MOS at device level ranging from the underlying physical principles through device characterization to static and dynamic logic configurations and analog circuit roles. It continues with some discussion of integrated circuit layout and provides some insights to the design of integrated systems, mainly digital, where the topics of circuit configuration and layout can no longer be separated.

A good understanding of semi-conductor conduction mechanisms and p–n junction behaviour is important in MOS design. For this reason, the basic physical theory of Chapter 1 is from first principles and could serve as a brief but adequate treatment for students with no previous knowledge of semi-conductor physics. This discussion moves quickly to introduce a number of important relationships. These are accepted as plausible and well-tested engineering results, while the burden of rigorous developments is omitted as being more appropriate to a detailed physics course.

Throughout the book an effort is made to impart a sound intuitive grasp of each topic before undertaking a quantitative assessment. Chapter 2 describes the action of the MOS transistor in very simple terms and then proceeds to describe the action of a variety of digital circuit configurations; the objective is to provide a broad qualitative appreciation of MOS circuitry before any detailed modelling is undertaken.

The planar fabrication process is described in Chapter 3. Chapter 4 continues that work on a quantitative level and is principally concerned with the specification of diffusion and oxidation cycles and with the electrical properties of diffused layers.

Chapters 5 through 8 are concerned with MOSFET device characterization, starting with a detailed discussion of threshold voltages in Chapter 5 and of current control in Chapter 6. In these chapters again the approach has been to generate reasonably accurate models through arguments which are plausible rather than rigorous while maintaining a 'feel' for the subject at all times. Design methods are based on process and device parameters which are easily measured. Actual measurement data for p- and n-channel devices are included in the appendices as well as derived parameter values. This data is used in some of the worked examples to predict the performance of certain circuit configurations. Though the current-control model is somewhat simplified, comparison with a more precise model is used to illustrate how accurate results can be obtained.

Chapters 7 and 8 provide a comprehensive analysis of the fundamental digital building block, the inverter. Important properties such as trigger level, rise time, and fall time are readily determined for different load types and varying supply conditions. The work is easily extended to arbitrary logic configurations and to buffer and interface designs.

Chapter 9 looks at some of the different technologies in the light of actual performance requirements and provides clarification of the relative merits and trade-offs, and the narrow ranges of parameters essential to satisfactory operation, particularly with CMOS. It also gives brief treatment of some special topics which include V-MOS power transistors and SOS technology.

Chapters 10 to 12 can be viewed as the 'applied' section of the book. They are concerned with analog and digital circuitry utilizing MOS devices and systems. However, they are not intended to provide instruction in analog design techniques or digital system design in a broad sense; their purpose is to show how the particular properties of MOS are best exploited. Of special importance is the topic of multi-phase dynamic logic and memory design. The computational methods of earlier chapters are fully applicable here, too, in dealing with topics such as charge sharing, refresh time, and such like. Chapter 12 is concerned mainly with digital systems design and the question of circuit layout from which it is inseparable. The treatment is no more than an introduction to a very large subject and is intended mainly to illustrate the interaction between electrical and topographical features and to demonstrate some very general approaches to the design of digital circuitry.

This book is intended primarily as an undergraduate text for Degree-level studies in Electronic Engineering. The material can be satisfactorily covered in courses ranging from 20 to 40 lecture hours over a three-month term or longer. It is also appropriate for use in intensive short courses spanning only a few weeks and was first used, in note form, for this purpose as a familiarization program for engineering staff at Analog Devices BV, Limerick. Accordingly, it is also recommended for use by practicing engineers whether they are engaged in actual integrated circuit design and fabrication or in a related peripheral activity. Its suitability as a design reference manual for engineers is supported by the inclusion of extensive graphical data in the appendices.

As a teaching instrument, the book can be used in a few ways. The detailed quantitative work is contained in Chapters 4 to 8 and in Chapter 10. While these represent the core material for design studies, it is possible also to teach a simplified and reasonably self-contained course which takes Chapters 1, 2, 3, 9, 11, and 12 only, in that order. Alternatively, this body of material might be taken first, and followed at a later time by Chapters 4 to 8 and 10. The main part of this work has been taught, for a few years now, as part of their final year Degree-level programme, to students of Electronic Engineering at the National Institute for Higher Education in Limerick.

It was felt that the purpose of the book would best be served by brevity in discussion and by offering a large number of numeric examples which serve to consolidate new ideas and to introduce reasonable values of the various process parameters. In addition, a number of problems appear in the form of a set of Case Studies which are used to tie together the various elements of the design activity. Answers to case study problems are also provided.

The writing of this book is in a large measure a consequence of my association with Analog Devices over a number of years as a design and training consultant. I am indebted to their Vice-President, Heinrich Krabbe, who provided both opportunity and encouragement and to Dr Philip Burton, Development Manager at ADI, for his every assistance. My thanks also to John C. Irvin of Bell Laboratories for his very helpful cooperation in furnishing graphical data on diffused layers.

The preparation of the manuscript has been greatly assisted by the cooperation of my colleagues in the Department of Electronic Engineering at NIHE, Limerick. In particular, I wish to thank Mr Gerard Stockil who provided programming support for inverter characterization, Ms Aine O'Brien who typed the manuscript, and Dr Grant Anderson, Head of Electronic Engineering, who provided full support and facilities.

May 1981 OLIVER J. MCCARTHY

List of Symbols

A	Cross-section area
BV	Breakdown voltage
β	Transistor 'gain', A/V^2
β'	Transistor 'gain', A/V^2, for square geometry
β_D	Driver gain
β_L	Load device gain
β_R	Ratio of (β_D/β_L)
C	Capacitance per unit area
C_L	Load capacitance
D	Diffusion coefficient
d_I	Depletion layer width above the junction
E	Electric field strength
E_c	Conduction band energy level
E_v	Valance band energy level
E_F	Fermi level
E_i	Intrinsic level
E_{go}	Gap energy
e_0	Permittivity of free space
F	Particle flux
GND	Symbol for 'ground' or reference potential
g_m	Device transconductance
I_s	Saturation current for diode or bipolar transistor
I_{DS}	Drain to source current
i_L	Instantaneous load current
i_D	Instantaneous driver current
I_o	Transistor current at entry to saturation
J	Current density
K_D	Depletion factor, V_I/V_{DD}, for depletion load
k	Boltzmann's constant
k_{si}	Relative permittivity of silicon
k_{ox}	Relative permittivity of silicon dioxide
L	Device length (from source to drain diffusion)
L'	Distance from end of channel to drain
ΔL	Horizontal penetration distance of diffusion
M	Body-effect factor
m	Relative drive factor for a non-saturated load
μ	Mobility
$\bar{\mu}$	Average mobility
n	Electron concentration
n_p	Electron concentration in p-type material

N	Impurity ion concentration
N_A	Acceptor concentration
N_D	Donor concentration
N_B	Ion concentration from doping sources in bulk
n^+	Heavily doped n-type region
n^-	Lightly doped n-type region
n_i	Intrinsic electron or hole concentration
p	Hole concentration per unit volume
p_n	Hole concentration in n-type material
p^+	Heavily doped p-type region
p^-	Lightly doped p-type region
Q	Electric charge or charge per unit area
Q_B	Depletion layer charge per unit area under gate with zero bulk bias
Q_{SS}	Oxide trapped charge per unit area for gate regions
Q_{Na^+}	Charge per unit area for mobile sodium ions in gate dielectric
q	Charge on an electron
R	Resistance
R_{on}	The ON-resistance of a driver or switch
R_s	Sheet resistance, ohms 'per square'
r_o	Small-signal output resistance
r_L	Small-signal load resistance
ρ	Resistivity
S	Strobe symbol
σ	Conductivity
T	Temperature
t_{ox}	Thickness of SiO_2 in gate region
T_D	Time constant, $C_L/\beta V_t$ for depletion loads.
T_f	Time constant (fall-time) for driver discharge
T_r	Time constant (rise-time) for MOS loads
T_{sc}	Unified time constant for enhancement loads and resistors
V_d	Drift velocity
V_{DS}	Drain-to-source potential difference
V_{GS}	Gate-to-source potential difference
V_{SB}	Source-to-bulk potential difference
V_{DB}	Drain-to-bulk potential difference
V_{CHS}	Channel-to-source potential difference
V_{CS}	Channel support voltage
V_{CB}	Channel-to-bulk potential difference
V_{GB}	Gate-to-bulk potential difference
V_{DD}	Drain supply level
V_{CC}	Supply level (CMOS circuits)
V_{GG}	Gate supply level
V_T	Threshold voltage in gate regions
V_{TF}	Field threshold voltage

V_{TO}	Threshold at source with $V_{BS}=0$
V_{TS}	Threshold voltage at source
V_{TD}	Threshold voltage at drain
V_{TCE}	Threshold voltage at channel end
V_{TL}	Load device threshold voltage
V_{TCEL}	Channel-end threshold for load device
V_{TP}	Threshold voltage for p-channel transistor
V_{TM}	Threshold voltage, mean of source and channel-end values
V_{TN}	Threshold voltage for n-channel transistor
V_{tr}	Trigger level
V_I	Inversion voltage, negative of V_T for a depletion-load device
V_{CHE}	Channel-end voltage using source reference
V_{OL}	Logic output low level
V_{OH}	Logic output high level
v_i	Instantaneous input voltage
v_o	Instantaneous output voltage
V_x	Transition voltage for a CMOS inverter
v_{ox}	Output voltage at transition between saturated and non-saturated conditions
v_{o1}, v_{o2}	Initial and final values of output voltage
v_s	Instantaneous signal voltage at input
W	Device width
ΔW	Lateral penetration distance of diffused layer under window
x_j	Junction depth
X_{mL}	Depletion layer width
ψ_0	Contact potential
$(2\phi_F)$	Contact potential based on N_B
$\phi_1, \phi_2, \ldots$	Clock phase labels

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CHAPTER 1

Conduction in Semi-conductors: An Overview

This introductory chapter does not deal directly with MOS devices or circuits. It is concerned with the basic 'raw materials' of integrated circuit fabrication—the semi-conductors. An understanding of the electrical properties of semi-conductors is a prerequisite to a study of electronic devices, both bipolar and MOS. The treatment here is brief and is principally directed towards providing insights into the electrical behaviour of a semi-conductor p–n junction. Those properties, which will be important in later work, are emphasized. Theoretical derivations are usually avoided; they are to be found in the appropriate physics texts. The objective here is rather to present results which have wide acceptance as useful engineering approximations and to impart an ability to use these results intelligently.

Silicon (Si) and, to lesser extent, germanium (Ge) are semi-conductors of interest. Both materials furnish four valence electrons per atom and all four are required in forming stable bonds with neighbouring atoms (Fig. 1.1).

This highly ordered arrangement is valid at absolute zero temperature (0 K or −273 °C). Increase in temperature introduces a random 'vibratory' motion to the crystal, increasing the possibility that an electron may break loose from its bond—in doing so, it becomes a 'free' electron and can participate in conduction. It leaves behind a *hole*, i.e. a location of nett positive charge. An electron in a neighbouring bond may 'jump' to fill this hole and so create another so that the hole appears to move in the opposite direction. (The electron in question is *not* a free electron but it has no statistical preference for one location rather than the other.) As this process repeats (with different electrons) *the hole displays true mobility*. The key point is that the hole is as acceptable at one location as any other and, given a highly dynamic system, will shift location on a purely random basis. The electron (negative charge $-q$) and hole (positive charge $+q$) can both participate in conduction. The value of electron charge is $q = 1.6 \times 10^{-19}$ Coulombs.

The thermal 'birth' of electron-hole pairs is balanced by a 'death' mechanism. An electron, on 'meeting' a hole, fills it; they *recombine* and disappear. Defining:

n = mobile electrons per cubic centimetre

p = (mobile) holes per cubic centimetre

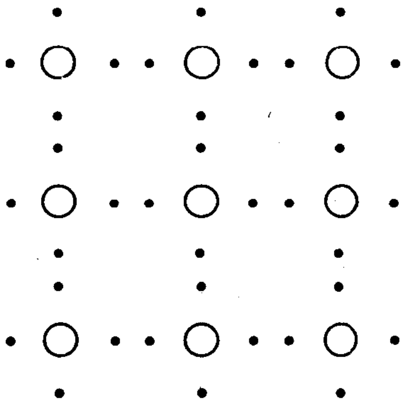

Fig. 1.1. Valence electrons in silicon and germanium.

a sample of pure (intrinsic) silicon or germanium has, by dynamic equilibrium, an intrinsic concentration $n_i = n = p$ which increases rapidly with temperature. A widely accepted expression for $n_i(T)$ is:

$$n_i(T) = 3.87 \times 10^{16} T^{3/2} e^{-E_{go}/(2kT/q)} \qquad \text{per cm}^3 \tag{1.1}$$

with T in °kelvin, $k = 1.38 \times 10^{-23}$ Joules/°K is Boltzmann's constant, and E_{go} is a physical constant with a value of 1.21 for silicon. For example:
At 300 K (27 °C):

$$n_i = 1.41 \times 10^{10} \qquad \text{per cm}^3$$

At 398 K (125 °C):

$$n_i = 6.80 \times 10^{12} \qquad \text{per cm}^3$$

Conduction in silicon is, of course, in direct proportion to n_i and the figures represent poor conduction at room temperature—hence the term *semiconductor.*

DONOR DOPING

Silicon or germanium may be doped with five-valence atoms (the most common is phosphorus). Doping is a process by which very low concentrations of a foreign material are added to the semi-conductor. It is usually achieved by diffusion of dopant atoms at very high temperatures and is described in detail later. A typical dose would be one phosphorus atom to 10^7 silicon atoms! Each phosphorus atom forms a bond with four silicon atoms in the usual way—which leaves a loosely held fifth electron, so loose that it is essentially a *conduction* electron. On entering conduction it leaves behind *an immobile positive ion.* The immobility stems from the fact that this atom is unlike any of its neighbours; it has little affinity for an electron in a neighbouring bond since it already has four bonding electrons.

A typical dose of phosphorus might be $N_D = 10^{16}$ atoms/cm^3 while silicon has about 10^{23} atoms/cm^3. Thus N_D augments n by 10^{16} atoms/cm^3 but since n_i is only 10^{10} approximately, this is a million-to-one increase! The new n value describes excellent conducting properties. The phosphorus atoms are referred to as 'donors' since each one 'donates' an electron to the conduction band. The large increase in n gives a boost to recombination so that p falls to quite a low level. Eventually, equilibrium is reached in a manner such that:

$$n_i^2(T) = np$$

is true for doped as well as intrinsic semi-conductors! (This is called the law of mass action). In this situation, electrons are *majority carriers* and holes are *minority carriers*, the latter contributing very little to current flow. To excellent approximation, $n = N_D$ and $p = n_i^2/N_D$. Since the majority carriers carry negative charge, the conduction mechanism, and the material so treated, are said to be 'n-type'.

ACCEPTOR DOPING

Doping with three-valence electron atoms (such as boron), in similar quantities to N_D, produces a crystal with occasional boron atoms bonding to silicon neighbours. In such a situation, one bond is incomplete (although neutral). It will readily take an electron from a normal bond nearby and thus become a stable immobile negative ion. Such three-valence atoms are called 'acceptors' since they accept an electron in order to form a stable bond. The electron capture leaves a hole which is essentially mobile. The concentration N_A of boron acceptor atoms contributes directly to p which increases vastly. The large hole population leads to a short-lived increase in recombination so that electron population falls and equilibrium is reestablished when $p = N_A$ (neglecting the small thermal contribution) and $n = n_i^2/N_A$.

If an n-type sample (i.e. one doped with donor atoms) is subsequently doped with an equal concentration of acceptor atoms, e.g. $N_A = N_D = 10^{16}$ atoms/cm^3, their effects cancel and the sample becomes intrinsic again. More generally, the effective doping level is $N_D - N_A$. Since electrical neutrality must be preserved, equating positive and negative total charge yields:

$$p + N_D = n + N_A \tag{1.2}$$

true for any doping conditions. Note that N_D, the concentration of donor atoms, is also the concentration of immobile positive ions and is approximately equal to the free electron concentration. Similar comments are valid for N_A.

The results, thus far, can be summarized as follows. Intrinsic semiconductors offer poor conduction with equal concentrations of holes and electrons which are thermally generated. Donor doping produces n-type material with large conductivity via electron flow. Acceptor doping produces p-type material with large conductivity via hole movement.

Our next task is to examine the two mechanisms which result in mass movement of conducting particles, positive or negative, and are thereby responsible for all external current flow.

CURRENT FLOW BY DRIFT

Drift is the familiar process whereby carriers (electrons or holes), in addition to their random thermal motion, show a nett movement in response to an applied electric field E volts per centemetre. Holes drift in the E direction, electrons in the opposite way (see Fig. 1.2). While E accelerates carriers between collisions, the velocity component acquired is lost with each collision and carriers show an average *drift velocity* V_d due to E. To take hole conduction as an example, the resulting current density is:

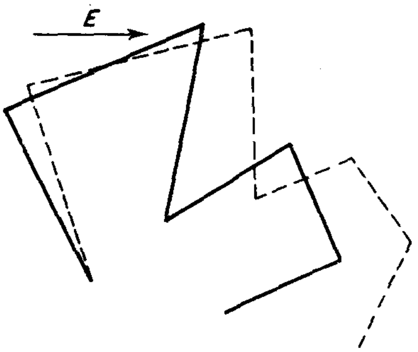

Fig. 1.2. Hole drift.
——— Random ($E=0$)
------ Forced ($E \neq 0$)

$$J_p = qpV_d \qquad \text{amperes (A)/cm}^2 \tag{1.3}$$

This is better appreciated in dimensional form as:

$$\frac{\text{Charge}}{\text{Particle}} \times \frac{\text{particles}}{\text{cm}^3} \times \frac{\text{cm}}{\text{sec}} = \frac{\text{charge/sec}}{\text{cm}^2} = \frac{\text{A}}{\text{cm}^2}$$

The drift velocity V_d is proportional to E and to a *mobility* term:

$$V_d = \mu E \qquad \text{cm/sec} \tag{1.4}$$

The mobility (μ_p for holes, μ_n for electrons) depends on crystal structure, temperature, level of doping, and other factors. Roughly speaking, electrons are about twice as mobile as holes.

We also define *conductivity* (σ) by the simple statement $J = \sigma E$. Since $J = qp\mu E$, we then have:

$$\sigma = qp\mu \qquad \text{(for holes)} \tag{1.5}$$

or, more generally:

$$\sigma = q(p\mu_p + n\mu_n) \tag{1.6}$$

for conduction involving both holes and electrons. It is intuitively correct that conductivity, the ability to transport electric current, should be in proportion to carrier concentrations and to their freedom of movement, their mobility.

The reciprocal of conductivity is *resistivity* (ρ):

$$\rho = \frac{1}{\sigma} = \frac{1}{q(p\mu_p + n\mu_n)} \quad \text{ohm } (\Omega) \cdot \text{cm} \tag{1.7}$$

In turn, resistivity and physical dimensions give the resistance of a sample (Fig. 1.3):

$$R = \frac{\rho l}{A} \tag{1.8}$$

or

$$\rho = \frac{RA}{l} \tag{1.9}$$

A most important set of curves give the resistivity of silicon at 300 K as a function of impurity concentration, and doping type. These appear in Appendix D. They refer to uniformly doped semi-conductors and demonstrate the higher mobility of electrons for all but very high doping levels. (The appendix also gives similar data for germanium and for gallium arsenide).

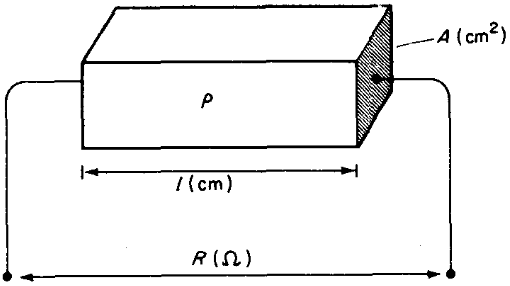

Fig. 1.3. Resistance of a rectangular section.

CURRENT FLOW BY DIFFUSION

In certain circumstances, concentration of a carrier type is non-uniform. Consider a case where hole density diminishes in the positive x direction (Fig. 1.4). Since these carriers are in random thermal motion, then, in a given time interval, more carriers will cross AA from left to right than in the other direction ***simply because carriers are more numerous on the left.*** This

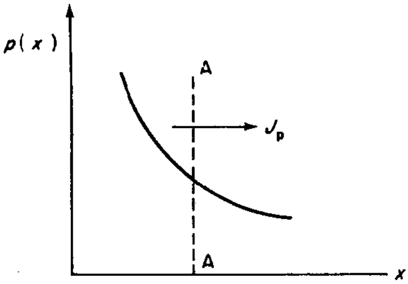

Fig. 1.4. Diffusion.

indicates a nett hole current density J_p amperes per square centimetre, as shown, which is quite plausibly proportional to the concentration gradient dp/dx (which determines particle flow rate) and the charge q per particle (since J is *charge* per square centimetre per second) with a proportionality factor known as the *diffusion coefficient* (D_p for holes, D_n for electrons). Thus, for hole diffusion:

$$J_p = -qD_p \frac{dp}{dx} \tag{1.10}$$

and, for electrons:

$$J_n = qD_n \frac{dn}{dx} \tag{1.11}$$

In checking the direction of J_n, remember that it represents *conventional* current flow. A positive electron gradient (dn/dx) causes electron diffusion from right to left and, hence, conventional current flow from left to right.

An important physical parameter $V_T = kT/q$ arises frequently in semiconductor theory. It has the dimensions of voltage and is referred to as the 'volt-equivalent of temperature'. Evaluated at 27 °C (i.e. 300 K), it has a value;

$$\frac{kT}{q} = \frac{1.38 \times 10^{-23} \times 300}{1.6 \times 10^{-19}} = 0.0259 = 25.9\,\text{mV}$$

It is of fundamental importance to the behaviour of a p–n junction. It also arises as the factor which links the two conduction mechanisms:

$$D_n = \frac{kT}{q} \mu_n \tag{1.12}$$

$$D_p = \frac{kT}{q} \mu_p \tag{1.13}$$

It indicates a direct proportionality between drift-induced flow and that resulting from diffusion. The diffusion effect is further promoted by higher temperature due to increased thermal motion.