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IEEE Computer Society
13, avenue de l'Aquilon
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IEEE Computer Society
Ooshima Building
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Foreword

On behalf of the ICCAD-91 Executive and Technical Program Committees, it is our great pleasure to welcome the participants to the 9th International Conference on Computer-Aided Design, and to present you this Digest of Technical Papers.

This year, the number of papers submitted to ICCAD was 448. The papers came from 24 countries, with 25% from industry and 41% from Non-USA countries. The Technical Program Committee of 61 world-renowned experts selected 126 exceptional papers for this year's conference.

The Technical Committee was subdivided into nine subcommittees, each of which included at least one member from Asia and one from Europe. After a careful two-day selection process, using a blind review, the Committee selected papers for presentation at the conference. We sincerely believe that the very high attendance at the paper selection meeting (94% of the members attended the meeting in Longmont, Colorado) and the blind review significantly contributed to the fairness and accuracy of the review process.

To complement the technical sessions, we are including in the program one excellent panel discussion on Monday night and eight half-day tutorials on Thursday. The panel, "The Cutting Edge in CAD: Who Will Get the Axe" will be done in a debate format, and we are sure that all attendants will enjoy it. The tutorials cover high-interest topics with four tracks. Attendants can select and register freely on the half-day base, although each track is set up for a specific subject. We hope that many of you will take the opportunity of participating in one or more of the tutorials.

As in the past years, daily breakfasts and lunches are provided to all conference attendees to encourage and promote professional interaction in a less formal setting. A cocktail party and a banquet are also provided in the conference registration fee. This year, the banquet will feature a Japanese music group, Taiko (Drum) and Koto (Harp), and we hope you enjoy the Japanese atmosphere.

ICCAD is the best place to learn about today's state-of-the-art in CAD for Electronic Circuit Design. Thank you for participating in ICCAD-91.

Satoshi Goto
Conference Chair

Louise Trevillyan
Technical Program Chair

CONFERENCE COMMITTEE

CONFERENCE CHAIR
Satoshi Goto
NEC Corporation
Daito Bldg. 7F
14-22, Shibaura, 4-chome
Minato-ku, Tokyo 108 Japan
+81-3-3456-6348

PROGRAM CHAIR
Louise Trevillyan
IBM Corp.
P.O. Box 218, MS 33-145
Yorktown Heights, NY 10598
(914) 945-1507

FINANCE CHAIR
Ed Cheng
Mentor Graphics Corp.
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Univ. of Colorado
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Knowledge Systems Lab.
NTT. Comm & Info. Proc. Lab.
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+31-40-743353

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Dept. of ECE
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(408) 285-5771

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(415) 962-5000

CONFERENCE MANAGERS
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(303) 530-4562

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In addition to the Technical Program Committee, the following people participated in the paper review process. The Technical Program Committee is grateful for their expertise and dedication to ICCAD.

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Tutorial: Multi-Level Logic Synthesis

Sharad Malik, Princeton Univ., Princeton, NJ
Sharad Malik is an Assistant Professor at Princeton University. His research interests are in the areas of logic synthesis and timing issues in VLSI design.

Richard Rudell, Synopsys, Inc., Mountain View, CA
Richard Rudell currently manages a research group at Synopsys, Inc. where he has worked since its inception. At UC Berkeley, Richard developed the Espresso and MIS logic synthesis programs.

Background: The attendee should understand the motivation behind logic synthesis and its critical role in automatic ASIC design. Familiarity with Boolean algebra and classical switching theory, static timing analysis, and testing techniques will be useful.

Description: This tutorial provides an overview of techniques for automatic logic design of sequential and combinational circuits, with particular emphasis on techniques that have proven practical for the design of large, multiple-level circuits.

The sequential techniques we will cover include the modern solutions to problems such as state minimization, state machine decomposition, and state assignment. We will cover many new problems in sequential optimization such as optimal clocking, retiming, and mixed combinational logic synthesis with retiming. We will also show very briefly how sequential ATPG plays a role in sequential optimization.

Multiple-level combinational logic synthesis includes technology-independent optimization and technology mapping. We will cover the best known techniques for each of these steps.

Finally, we will show how all of these pieces come together to form a complete logic synthesis system for sequential and combinational circuits.

Tutorial: Advanced Sequential Circuit Testing Techniques

Kwang-Ting Cheng, AT&T Bell Labs., Murray Hill, NJ
Dr. Cheng is a member of the Technical Staff at AT&T Bell Labs., where he is leading exploration of new methodologies and techniques for sequential circuit testing. He has over 40 publications and is the co-author of the book "Unified Method for VLSI Simulation and Test Generation".

Irith Pomeranz, Univ. of Iowa, Iowa City, IA
Irith Pomeranz is an Assistant Professor at the University of Iowa; she has worked extensively on techniques for assuring 100% fault coverage for sequential ATPG.

Background: Knowledge of switching and automata theory and the basics of logic design is suggested. Familiarity with basic testing concepts is recommended.

Description: The tutorial covers the theory and application of sequential circuit testing at the chip level. Due to recent advances in automatic sequential circuit test generation, the need for high-overhead design for testability techniques, such as full scan design, is reduced. Current methods for test generation and low-cost design for testability for sequential circuits will be presented.

Test generation approaches can be classified according to the level of abstraction at which the circuit is described or according to the fault model employed. We will illustrate that no single approach out-performs the others for all applications, resulting in a need for a comprehensive set of test generation procedures.

Existing circuit synthesis methods may produce circuits containing redundant logic. The relationships between the existence of redundant logic and untestable faults in sequential circuits will be presented. Methods for the identification of such faults based on test generation techniques will be described.

Design for testability is still required for extermely large circuits. However, as test generation advances, the amount of hardware added for testing purposes reduces. Partial Scan allows the tradeoff between test generation effort and hardware overhead to be automatically explored. Different approaches to partial scan will be presented.

Tutorial: Software Engineering and Object-Oriented Programming for CAD

Howard Mozeico, Mentor Graphics Corp., Wilsonville, OR
Howard Mozeico is director of special engineering projects in the Framework Products Division at Mentor Graphics Corporation.

Wayne Wolf, Princeton Univ., Princeton, NJ
Wayne Wolf has designed experimental and production CAD systems at both Princeton University and AT&T Bell Laboratories; he has published widely on programming technology for CAD.

Background: Programming experience with C is recommended. The tutorial is aimed at both programmers and programming project managers.

Description: Modern CAD systems are huge software projects---typical commercial systems include several million lines of code. An understanding of the latest and best software engineering techniques is critical to the design, development, and support of CAD systems. This tutorial surveys software engineering methods important to CAD system design, and concentrates on object-oriented programming as a key software design technology.

Object-oriented programming (OOP) languages help programmers build more modular extensible, and maintainable programs. OOP is useful in both small programming projects and company-wide, multi-year programming efforts. The tutorial introduces the basics of object-oriented programming and illustrates how typical CAD programs can be improved when recast in an object-oriented language. It then goes on to a case study: how the C++ object-oriented language was used to design a multimillion-line CAD framework. Examples from CAD systems are used throughout to illustrate important concepts.

Tutorial: Framework Technology: Current Status and Future Directions

Bob Carver, Cadence Design Systems, Inc., Santa Clara, CA
Bob Carver is the Cadence-MCC program director. Mr. Carver was a founding member of the CAD Framework Initiative and has served as the Vice-president for two years.

Ed Guy, Digital Equipment Corp., Marlboro, MA
Ed Guy is a Digital Equipment Corporation Visiting Researcher at MCC CAD Framework Lab; he chairs the CFI InterTool Communication Technical Subcommittee and is involved with several commercial framework projects.

Nick Naclerio, United States Air Force, Arlington, VA
Nick Naclerio is a Program Manager at the Defense Advanced Research Projects Agency (DARPA). He has been involved in Framework technology for CAD, CIM and CALS at both DARPA and the Air Force. He is a charter member of the CFI Technical Advisory Board.

Background: This tutorial assumes that the participant is familiar with CAD tools and, at least in a general sense, the fact that frameworks glue these tools together to support the product-development process. Familiarity with CAD framework technology is helpful, but not required.

Description: The emergence of integrated design environments--frameworks--and standards that will allow tools from multiple sources to share information will greatly change the product-development environment of the mid- to late- 1990's. This tutorial will begin with an overview of current framework technology: what the components are, what role they play in the design process, how they interact, and the role of standards in framework evolution. We will then use this overview as the base from which to discuss future directions and the evolution of framework technology. The tutorial will examine (1) what the design environment of the mid- to late- 1990's will look like, and (2) how it will evolve from today's technology. In particular, we will try to point out the "holes" along the path from the frameworks we have today to the design environments we will need in the coming decade.

Tutorial: CAD And Architecture Issues in FPGAs

Abbas El Gamal, Stanford Univ., Palo Alto, CA
Abbas El Gamal is a Professor of Electrical Engineering at Stanford; he was a founder of Actel Corp.

Dwight Hill, AT&T Bell Labs., Murray Hill, NJ
Dwight Hill received his Ph.D. degree at Stanford University. He is currently a distinguished member of the Technical Staff at Bell Labs. He has worked extensively in machine architecture, physical design systems, and FPGAs.

Stephen Trimberger, XILINX, San Jose, CA
Stephen Trimberger received his Ph.D. degree from Caltech; he is Manager of Advanced Development for Xilinx.

Background: Some experience with ASIC design such as the use of gate arrays, or PALs, and some familiarity with general CAD tools such as schematic capture and logic synthesis, will be useful for this tutorial. Knowledge of IC circuit and layout issues may be helpful, but is not required.

Description: Field Programmed Gate Arrays (FPGAs) provide a unique and challenging target technology for CAD Tools. Whereas some aspects of FPGA architectures resemble traditional design architectures such as gate arrays or standard cells, the application of traditional CAD tools has met with mixed results.

We will present an overview of several categories of FPGAs, including SRAM- and antifuse based parts, and will discuss some of the strengths and weaknesses of each. The discussion will cover these architectures from both a user's perspective as well as from a CAD tool developer's perspective. Finally we will summarize some of the current CAD tool work used to support the use of FPGAs, including logic synthesis and mapping, placement, routing, editing and configuration.

Tutorial: Design, Modeling and Simulation of Multi-Chip Modules

John L. Prince, Univ. of Arizona, Tucson, AZ
John Prince is Director (Acting), Packaging Sciences and Distinguished Visiting Scientist at Semiconductor Research Corporation and Professor of Electrical and Computer Engineering at the Univeristy of Arizona, where he leads a research team in packaging CAD tool development.

Leonard W. Schaper, Alcoa Electronic Packaging, San Diego, CA
Leonard Schaper is Director of Thin Film Product Programs for Alcoa Electronic Packaging.

Background: The tutorial is aimed at an audience familiar with chip design, but not familiar with Multi-Chip Modules (MCMs) or general packaging trends and design/ modeling/simulation techniques.

Description: Trends in system hardware indicate the importance of multi-chip packaging (e.g., Multi-Chip Modules) in the near future. Although performance advantage is the most often cited reason for this trend, significant advantages in density are also obtained, and cost and reliability benefits may also accrue. Design and analysis methods (electrical and thermal) necessary for these systems (or subsystems) do not have exact analogs in the chip design area. Considerations must be given to broad-band electromagnetic signal propagation characteristics of interconnects, for example, and the factors involved may be quite complex for digital systems operating at clock frequencies well above 100MHz.

This tutorial will introduce MCM packaging technology and will discuss status and trends in this technology. With this as a background, design methodologies will be discussed, modeling and simulation techniques will be examined, and the appropriate and necessary tools for high-performance MCMs will be identified. Examples of performance characteristics from modeling of advanced MCM-type structures will be given. Consequences of technology limitations (e.g., use of perforated ground planes) will be pointed out, for high-performance systems.

Tutorial: CAD Challenges for Consumer Parts and Related Designs

Moderator: D.M. Henry Walker - Carnegie Mellon Univ., Pittsburgh, PA
Hank Walker is Assistant Director and Research Engineer in the SRC-CMU Research Center for CAD at Carnegie Mellon University.

Description: As the worldwide market for semiconductors and electronics continues to expand, the quality and availability of critical CAD tools must improve to match this growth. Despite the commonality of many CAD tools across application sectors--for example, circuit simulation is essentially universal--many emerging applications have their own unique CAD requirements. In this tutorial track, attendees will hear a sequence of experts from several strategically important application areas. Each speaker will define the design problems in their area, the state of current CAD tools for their area, and the CAD challenges that must be overcome as their area evolves in the decade of the 1990's.

Topic: Integrated Telecommunications ICs
Speaker: Dirk H. Rabaey, Alcatel Bell Telephone, Antwerp, Belgium
Dirk Rabaey is Manager of Microelectronics and Hardware Technology in the Switching Systems Division of Alcatel.

Topic: Analog and Mixed-Signal ASICs
Speaker: Michael A. Winchell, NCR Corp., Fort Collins, CO
Mike Winchell is the project leader for the Analog CAD Group at NCR Microelectronics Products Division.

Topic: Automotive Electronics
Speaker: Frank Szorc, Delco Electronics/General Motors Corp., Kokomo, IN
Frank Szorc is a Group Leader responsible for Automated Layout and Design Synthesis Tools at the IC Design Center of Delco Electronics.

Topic: MEMS: MicroElectroMechanical Systems
Speaker: Kensall D. Wise, Univ. of Michigan, Ann Arbor, MI
Ken Wise is Professor of Electrical Engineering Computer Science and Director of the Center for Intergrated Sensors at the University of Michigan. He has worked extensively in the field of integrated sensors and their applications.

Tutorial: CAD Challenges for Computers and Systems

Moderator: D.M. Henry Walker, Carnegie Mellon Univ., Pittsburgh, PA

Topic: High-End Consumer Systems
Speaker: Leo Nederlof, Philips Research Labs., Eindhoven, The Netherlands
Leo Nederlof is Manager of the MICROTEL IC Design group of Philips Research Lab; with his group, he is heavily involved in the realisation of consumer systems on silicon.

Topic: Memories
Speaker: Tsuguo Shimizu, Hitachi, Ltd., Tokyo, Japan
T. Shimizu researches design automation systems at Hitachi, Ltd., and now leads the development of their high-level synthesis system.

Topic: Microprocessors
Speaker: Robert Colwell, Intel Corp., Hillsboro, OR
Robert Colwell is a Staff VLSI Architect at Intel, working on future implementations of the i386™ instruction set architecture.

Topic: High-End Computer Systems
Speaker: John Darringer, IBM Corp., Somers, NY
John Darringer is Director of Electronic Design Automation for IBM.

Panel: The Cutting Edge in CAD: Who Will get the Axe?

Panel Chair: *Kurt Keutzer* - Synopsys, Inc., Mountain View, CA

In the world of CAD research, as in the entire IC industry, it is true that "To the victor belongs the spoils." We can identify three major players in the CAD research competition: Universities, Corporate CAD Centers and CAD Vendors. All three have a vested interest in establishing a leading edge in CAD research, and each group is uniquely positioned to do so. However, the current economic environment is one in which corporate CAD research and development budgets are diminishing, university research is becoming more focussed and CAD vendors are being pressed to exceed the state-of-the-art in order to survive. As a result each of these groups is forced to compete for the same shrinking supply of R&D dollars and ultimately only one is likely to emerge pre-eminent in a research area.

Given the need to establish acknowledged pre-eminence to survive and grow, which one of these groups is likely to lead in CAD research? It is common to look to universities as the leading research centers, but the lack of exposure to real design problems hampers most university research. The advantage that corporate CAD researchers enjoy due to their close interaction with on-site circuit designers is reflected in their long history of innovation in CAD area; however, the trend in large corporations is that more and more dollars for CAD are being diverted to external tools. With this influx of capital, CAD vendors have an opportunity to increase their research spending, but most often, business concerns dictate that improving market share is a higher priority than establishing a research lead.

So who will determine the cutting edge of CAD and who will get the axe? You're invited to join in this timely debate in which each of our panelists will represent one of these groups and argue that their group is most likely to become the pre-eminent arena for CAD research.

- **Corporate CAD:** *William Joyner,* IBM Corp., Yorktown Heights, NY
- **CAD Vendors:** *Min-Yu Hsueh,* Cadence Design Systems, Inc., San Jose, CA
- **Universities:** *Hugo de Man,* Katholieke Univ., Leuven, Belgium