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SEMICONDUCTOR HETEROSTRUCTURE DEVICES

by Masayuki Abe
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Semiconductor Heterostructure Devices

Part I: High Electron Mobility Transistors

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Part II: Resonant Tunneling Devices

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Preface to the Series

Modern technology has a great impact on both industry and society. New technology is first created by pioneering work in science. Eventually, a major industry is born, and it grows to have an impact on society in general. International cooperation in science and technology is necessary and desirable as a matter of public policy. As development progresses, international cooperation changes to international competition, and competition further accelerates technological progress.

Japan is in a very competitive position relative to other developed countries in many high technology fields. In some fields, Japan is in a leading position; for example, manufacturing technology and microelectronics, especially semiconductor LSIs and optoelectronic devices. Japanese industries lead in the application of new materials such as composites and fine ceramics, although many of these new materials were first developed in the United States and Europe. The United States, Europe, and Japan are working intensively, both competitively and cooperatively, on the research and development of high-critical-temperature superconductors. Computers and communications are now a combined field that plays a key role in the present and future of human society. In the next century, biotechnology will grow, and it may become a major segment of industry. While Japan does not play a major role in all areas of biotechnology, in some areas such as fermentation (the traditional technology for making "sake"), Japanese research is of primary importance.

Today, tracking Japanese progress in high-technology areas is both a necessary and rewarding process. Japanese academic institutions are very active; consequently, their results are published in scientific and technical journals and are presented at numerous meetings where more than 20,000 technical papers are presented

orally every year. However, due principally to the language barrier, the results of academic research in Japan are not well known overseas. Many in the United States and in Europe are thus surprised by the sudden appearance of Japanese high-technology products. The products are admired and enjoyed, but some are astonished at how suddenly these products appear.

With the series *Japanese Technology Reviews*, we present state-of-the-art Japanese technology in five fields:

Electronics,
Computers and Communications,
Manufacturing Engineering,
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Each tract deals with one topic within each of these five fields and reviews both the present status and future prospects of the technology, mainly as seen from the Japanese perspective. Each author is an outstanding scientist or engineer actively engaged in relevant research and development.

We are confident that this series will not only give a bright and deep insight into Japanese technology but will also be useful for developing new technology of our readers' own concern.

As editor in chief, I would like to acknowledge with sincere thanks the members of the editorial board and the authors for their contributions to this series.

TOSHIAKI IKOMA

Preface

The semiconductor-superlattice concept was first presented by Esaki and Tsu in 1970. Dingle et al. successfully applied the concept in modulation-doped GaAs-AlGaAs superlattices in 1978. In 1980, Mimura et al. succeeded in developing a high electron mobility transistor (HEMT), using a two-dimensional electron gas channel confined in a high quality modulation-doped single heterostructure. Since this invention, the research and development of HEMTs, MODFETs and other devices has been vigorously promoted, resulting in the development of commercially available microwave HEMTs. In the 1990s, the HEMT will also be used in digital applications, such as supercomputer systems.

The research and development of HEMTs has made major contributions to epitaxial growth techniques, such as MBE and MOCVD. These techniques enabled the fabrication of semiconductor heterostructures with precisely controlled heterointerfaces. This, in turn, triggered the research and development of any other devices that use quantum mechanical effects, such as resonant tunneling devices.

This book is concerned with the fundamentals and applications of these heterostructure devices. Part 1 describes physical principles and operational characteristics of HEMTs, and covers analog and digital applications. Part 2 discusses the physical principles and operating characteristics of a resonant tunneling hot electron transistor (RHET), a resonant tunneling bipolar transistor (RBT), and recent advances in this device technology using InGaAs-based materials. The microwave characteristics of these resonant tunneling transistors is also described.

The author of Part 1 thanks Takashi Mimura, Yasutake Hirachi, Kohichiro Odani, Kazuo Kondo and Junji Komeno, and his colleagues, whose many contributions have made possible the results

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The author of Part 2 thanks Kenichi Imamura, Hiroaki Ohnishi, Toshihiko Mori, and Toshiro Futatsugi for their contributions to the development of resonant tunneling transistors, and Shunichi Muto, Tsuguo Inata, and Toshio Fujii for their support in the fields of epitaxial growth and evaluation. He also expresses his gratitude to Akihiro Shibatomi, Masaaki Kobayashi, and Takahiko Misugi for their continuing encouragement. This work was performed under the management of the R&D Association for Future Electron Devices as a part of the R&D Project of Basic Technology for Future Industries sponsored by the Agency of Industrial Science and Technology, Ministry of International Trade and Industry, Japan.

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and
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PART 1

High Electron Mobility Transistors

1.1. Introduction

Since the 1980 announcement of the high electron mobility transistor (HEMT),¹ HEMT technology has progressed rapidly in digital and analog application fields, offering new possibilities for ultrahigh-speed large-scale integration (LSI)/very large scale integration (VLSI) applications² and high frequency microwave devices applications. The evolution of high-speed low-power HEMT devices is the result of continuous technological progress utilizing the superior electronic properties due to the supermobility of GaAs/AlGaAs heterojunction structure. Electron mobility in the conventional GaAs metal semiconductor field-effect transistor (MESFET) channel with typical donor concentrations of around 10^{17} cm^{-3} ranges from 4000 to 5000 $\text{cm}^2/\text{V}\cdot\text{s}$ at room temperature. The mobility in the channel at 77 K is not too much higher than at room temperature due to ionized impurity scattering. In undoped GaAs, however, electron mobility of 2 to $3 \times 10^5 \text{ cm}^2/\text{V}\cdot\text{s}$ has been obtained at 77 K. The mobility of GaAs with feasibly high electron concentrations for facilitating the fabrication of devices was found to increase through modulation-doping techniques demonstrated in GaAs/AlGaAs superlattices.³ As the first application of this electron mobility-enhanced phenomena to the new transistor approach, a high electron mobility transistor (HEMT), based on modulation-doped GaAs/AlGaAs single heterojunction structures, was invented¹ and was demonstrated to greatly improve the 77 K channel mobility.

HEMTs are being used in satellite communications and are being effectively applied in radio astronomy observation applications to discover new interstellar materials in the universe.

HEMT technology has been demonstrated to be promising for ultra-high-speed LSI/VLSI applications.^{1,4-6} Due to the supermobility of GaAs/AlGaAs heterojunction structure, the HEMT is

especially attractive for low-temperature operations at liquid nitrogen temperature. In 1981 a HEMT ring oscillator with a gate length of $1.7\ \mu\text{m}$ demonstrated a $17.1\ \text{ps}$ switching delay with $0.96\ \text{mW}$ power dissipation per gate at $77\ \text{K}$, indicating that switching delays below $10\ \text{ps}$ will be achievable with $1\ \mu\text{m}$ gate devices.⁴ A switching delay of $8.5\ \text{ps}$ with $2.59\ \text{mW}$ power dissipation per gate has already been obtained with a $0.5\ \mu\text{m}$ gate device at $77\ \text{K}$.⁷ And also, $5.8\ \text{ps}$ with $1.76\ \text{mW}$ power dissipation per gate at $77\ \text{K}$ and $10.2\ \text{ps}$ with $1.03\ \text{mW}$ power dissipation per gate at $300\ \text{K}$ have been achieved for a $0.35\ \mu\text{m}$ gate device.⁸ Even at room temperature, $9.2\ \text{ps}$ with $4.2\ \text{mW}$ per gate has been obtained with a $0.28\ \mu\text{m}$ gate device.⁹

More complex circuits were achieved by divide-by-two operations of HEMT frequency dividers with direct coupled FET logic (DCFL) circuits, demonstrating maximum clock frequencies of $8.9\ \text{GHz}$ ^{10,11} and $13\ \text{GHz}$ ¹² at $77\ \text{K}$. The maximum clock frequency achieved with HEMT technology is roughly two times higher than that of its GaAs MESFET counterpart with comparable geometry.

For LSI level complexity, HEMT technology has made it possible to develop a $4\ \text{kbit}$ static RAM,^{13,14} $16\ \text{kbit}$ static RAM¹⁵ as memory circuits, and a $4.1\ \text{kgate}$ gate array with 16×16 -bit parallel multiplier¹⁶ as a logic circuit. The $4\ \text{kbit}$ static RAM has an address access time of $500\ \text{ps}$ with a power dissipation of $5.7\ \text{W}$ per chip, designed ECL compatible level.¹⁴ The 16×16 -bit parallel multiplier designed on $4.1\ \text{kgate}$ gate array has a multiply time of $4.1\ \text{ns}$ with a power dissipation of $6.2\ \text{W}$. HEMT has already jumped into the LSI/VLSI application field.

This part first presents the principle and performance advantages of HEMT approaches, with the focus on scaled-down device structure in the submicron dimensional range. Next, microwave HEMT with low noise/high power performances for analog applications are described. Then we will describe a HEMT LSI technology, including material, self-alignment device fabrication technology. Finally, the current status and recent advances in HEMT logic and memory LSI circuit implementation are discussed and the future of HEMT VLSI prospects for ultrahigh-speed computer applications is projected.

1.2. HEMT Principle and Performance Advantages

HEMT technology has new possibilities for LSI/VLSI with high speed and low power dissipation. This section describes the principles of the HEMT, its technological advantages compared with other technologies for high-speed devices, and HEMT performances scaled down in the submicron dimensional range.

1.2.1. Principle and Technology: Comparison with other High-Speed Device Approaches

A cross-sectional view of the basic structure of a HEMT, with a selectively doped GaAs/AlGaAs heterojunction structure, is shown in Fig. 1. An undoped GaAs layer and Si-doped n-type AlGaAs layer are successively grown on a semi-insulating GaAs substrate by molecular beam epitaxy (MBE). Because of the higher electron affinity of GaAs, free electrons in the AlGaAs layer are transferred to the undoped GaAs layer, where they form a two-dimensional high-mobility electron gas within 10 nm of the interface. The n-type AlGaAs layer of the HEMT is completely depleted in two depletion mechanisms: (1) the surface depletion results from the trapping of free electrons by surface states; and (2) the interface depletion results from the transfer of electrons into the undoped GaAs. The Fermi level of the gate metal is matched to the pinning point, which is 1.2 eV below the conduction band. With the reduced AlGaAs

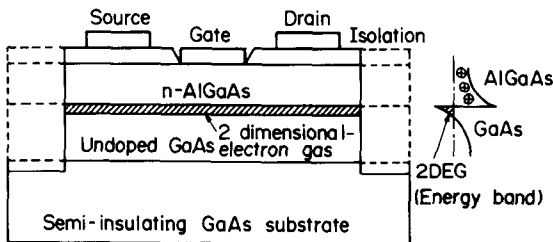


Figure 1. Cross-sectional view of the basic structure of a HEMT, with a selectively doped GaAs/AlGaAs heterostructure.

layer thickness, the electrons supplied by donors in the AlGaAs layer are insufficient to pin the surface Fermi level. Therefore, the space-charge region extends into the undoped GaAs layer and, as a result, band bending results in the upward direction, and the two-dimensional electron gas does not appear. When a positive voltage higher than the threshold voltage is applied to the gate, electrons accumulate at the interface and form a two-dimensional electron gas (2DEG).

Thus, we can control the electron concentration to achieve depletion (D)-mode and enhancement (E)-mode HEMT operation.^{1,17} Electron mobility and sheet electron concentration (N_s) in the heterostructure are shown as a function of temperature in Fig. 2.¹⁸ As temperature decreases, the electron mobility, which was about $8 \times 10^3 \text{ cm}^2/\text{V}\cdot\text{s}$ at 300 K, increases dramatically and reaches $2 \times 10^5 \text{ cm}^2/\text{V}\cdot\text{s}$ at 77 K due to reduced phonon scattering. A further increase with a considerable gradient occurred even below 50 K, and a maximum value of $1.5 \times 10^6 \text{ cm}^2/\text{V}\cdot\text{s}$ in the dark and $2.5 \times 10^6 \text{ cm}^2/\text{V}\cdot\text{s}$ under light illumination was attained at 4.2 K. Sheet electron concentration decreases with decreasing temperature until it becomes constant below 150 K. The almost constant value of about $3.5 \times 10^{11} \text{ cm}^{-2}$ below 150 K corresponds to that of 2DEG at the interface, since this value agrees well with the value of N_s

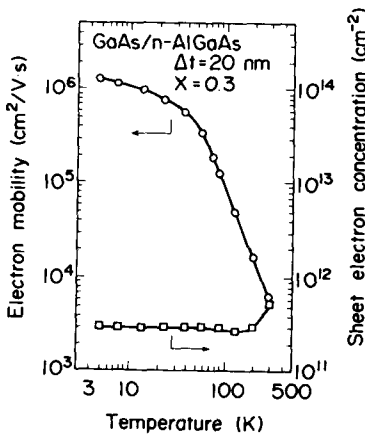


Figure 2. Electron mobility and sheet electron concentration in GaAs/n-AlGaAs with a 20 nm thick undoped AlGaAs spacer layer, as a function of a temperature.

determined by Shubnikov-de Haas measurement at 4.2 K. Apparent excess carriers above 150 K are attributed to free electrons which are thermally excited from relatively deep donors in n-type $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$.

In HEMT structures the AlGaAs layer heavily doped with donors like Si contains DX centers¹⁹ which behave as electron traps at low temperatures. Some anomalous behaviors at low temperatures are believed to be related to these traps. These include distortion of drain I-V characteristics, an unexpected threshold voltage shift at low temperatures and highly sensitive persistent photoconduction. We have found that the distortion of drain I-V characteristics is related to the type of device structure. In a conventional partial gate HEMT structure which has relatively long ($> 100 \mu\text{m}$) exposed surfaces of AlGaAs at both sides of the gate, electrons heated by the drain field have sufficient energy to transfer from a GaAs channel to the AlGaAs region with exposed surface of the drain side of the gate where they are trapped at DX centers. As a result, space charges build up at the drain side of the gate. This eventually increases the drain output resistance in the linear region of operation, leading to drain current collapse. To eliminate drain current collapse at low temperature, we adopt a self-aligned gate structure as shown in Fig. 1. The n-AlGaAs layer is completely covered by the n-GaAs top layer. There are no exposed surfaces at the drain end of the gate. In the structure, high energy electrons can easily pass through the thin n-AlGaAs layer (30 nm) without being trapped and can reach the n-GaAs top layer, eliminating the anomalous drain I-V characteristics at low temperature. Concerning the threshold voltage shift with temperature, 0.2 V to 0.3 V shift for the temperature range from 300 K to 77 K has been reported in a HEMT. We have succeeded in eliminating the threshold voltage shift and sensitive persistent photoconduction effect by optimizing device parameters with reduced AlAs mole fraction of 0.2.

The technological advantages of HEMTs are compared to various competing approaches to high-speed devices design in Table 1. It is difficult to compare their optimized performances fairly. Here we have the criteria based on 0.5-1 μm device technology. The switching delay of GaAs MESFETs is two or three times longer

Table 1. Technological advantages of HEMTs compared with various competing high-speed device approaches.

Device approach	Performances			Uniformity & Control-ability ($\sigma V_T/\text{swing ratio}$)	Fabricability	Material problems	Total advantages
	Speed	Power					
HEMT $L_G = 0.5\text{--}1 \mu\text{m}$	Exc. 10 ps Highly geometry controllable	Very good 0.1 mW		Exc. 10–20 mV (1%)	Exc. Simple MBE & OMVPE Dry etching	Good Defect & trap free epi High throughput Good Defect free ingot	Exc. Good
GaAs MESFET $L_G = 0.5\text{--}1 \mu\text{m}$	Good 20–30 ps Poor geometry controllable	Good 1 mW		Good 60 mV (10%)	Exc. Simple		Good
GaAs/AlGaAs HBT	Exc. 10–30 ps	Good 1 mW		Exc. ($< 1\%$)	Complex New process required	Good Defect & trap free epi High throughput Exc.	Unknown
SiMOSFET	Very poor 80 ps	Very good 0.1 mW		Exc. (1%)	Complex	High throughput Exc.	Difficult to high speed
Si bipolar	Good 30–60 ps	Poor 1–10 mW		Exc. ($< 1\%$)	Complex	Exc.	Difficult to large scale

than that of HEMTs. GaAs/AlGaAs heterojunction bipolar transistors (HBT) should achieve the same high-speed performance as the HEMT. The ultimate speed capability, limited by cutoff frequency f_T , is over 100 GHz, and the HBT also has the merit of flexible fan-out loading capability. The silicon MOSFET and bipolar transistor are excellent for both designing due to threshold voltage uniformity and controllability with no material problems, and for ease of fabrication in spite of complex processing steps. Configuration for both high-speed and large-scale integration with low-power performance, however, may be difficult for Si-based technology. HEMTs are very promising devices for high-speed VLSI, but require new technological breakthroughs to achieve the LSI quality of GaAs/AlGaAs material, using MBE and/or organic metal vapor phase epitaxy (OMVPE) and the self-alignment device fabrication technologies as described in the following sections.

To evaluate the high-speed capability of HEMTs in complex logic circuits, a single-clocked divide-by-two circuit based on the master-slave flip-flop consisting of eight direct-coupled FET logic (DCFL) NOR gates, one inverter, and four output buffers was fabricated. The circuit has a fan-out of up to 3 and employs 0.5 mm long interconnects, giving a more meaningful indication of the overall performance of HEMT integrated circuits (IC's) than that obtained with a simple ring oscillator. The basic gate consists of $0.5 \times 20 \mu\text{m}$ gate E-HEMT and saturated resistors as loads. Direct writing electron-beam lithography and lift-off techniques were used throughout the fabrication process. Divide-by-two operation is demonstrated at up to 8.9 GHz at 77 K and up to 5.5 GHz at 300 K.¹¹ The values of 8.9 and 5.5 GHz, respectively, correspond to internal logic delays of 22 ps/gate with power dissipation of 2.8 mW/gate at 77 K and 36 ps/gate with power dissipation of 2.9 mW/gate at 300 K, with an average fan-out of about 2. A frequency divider circuit composed of dual-gate, selectively doped heterojunction transistors (SDHT) with $0.7 \mu\text{m}$ gate lengths was also fabricated, showing a maximum clock frequency of 13 GHz at 77 K.¹² Figure 3 compares switching delay and power dissipation for a variety of frequency dividers.^{11,12,20} The switching speed of HEMT is roughly three times as fast as that of a GaAs MESFET.

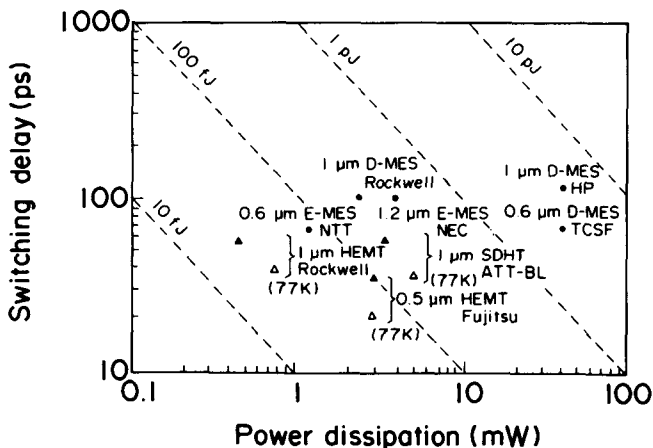


Figure 3. Switching delay and power dissipation of a variety of frequency dividers. The symbol ● denotes GaAs MESFET at 300 K, ▲ and △ HEMTs at 300 K and 77 K, respectively.

1.2.2. HEMT Performances in the Submicron Dimensional Range

HEMT has a performance advantage over conventional devices, because of superior electron dynamics of HEMT channels and the unique electrical properties of HEMT structure. During switching, the speed of the device is limited by both low-field mobility and saturated drift velocity. Low-field mobility routinely obtained is $8000 \text{ cm}^2/\text{V}\cdot\text{s}$ at 300 K and $40,000 \text{ cm}^2/\text{V}\cdot\text{s}$ at 77 K. Saturated drift velocity measured with HEMT structures at room temperature has been reported to be 1.5 to $1.9 \times 10^7 \text{ cm/s}$. These superior transport properties in HEMT channels would result in a high average current-gain-cutoff frequency f_T value.

Going to LSI circuits with low power dissipation per gate, logic voltage swing should be minimized. A high transconductance g_m value with a small logic voltage swing is achieved. The transconductance g_m in gradual channel approximation is given by $g_m = K(V_{GS} - V_T)$, where notations have their usual meanings. K is given by $K = (\epsilon\mu_n W_G / 2dL_G)$, where ϵ is the dielectric constant, μ_n the