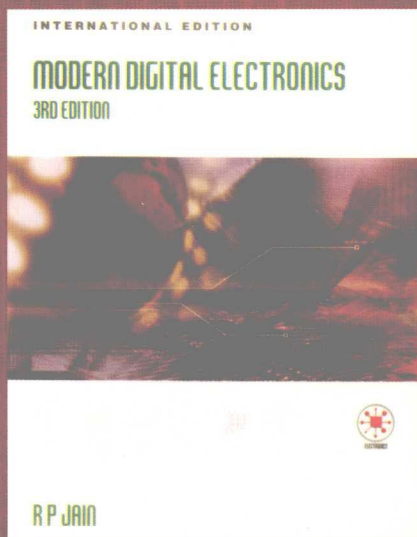


Mc
Graw
Hill Education

清华版双语教学用书



现代数字电子学 (第3版)

Modern Digital Electronics
(Third Edition)

R. P. Jain

清华大学出版社

Mc
Graw
Hill

清华版双语教学用书

现代数字电子学 (第3版)

Modern Digital
Electronics

(Third Edition)

R. P. Jain

江苏工业学院图书馆
藏书章

清华大学出版社
北京

Modern Digital Electronics(Third Edition)

R. P. JAIN

EISBN: 007-123670-8

Copyright © 2003 by The McGraw-Hill Companies, Inc.

Original language published by The McGraw-Hill Companies, Inc. All Rights reserved. No part of this publication may be reproduced or distributed by any means, or stored in a database or retrieval system, without the prior written permission of the publisher.

Authorized English language edition jointly published by McGraw-Hill Education (Asia) Co. and Tsinghua University Press. This edition is authorized for sale only to the educational and training institutions, and within the territory of the People's Republic of China (excluding Hong Kong, Macao SAR and Taiwan). Unauthorized export of this edition is a violation of the Copyright Act. Violation of this Law is subject to Civil and Criminal Penalties. 本书英文影印版由清华大学出版社和美国麦格劳-希尔教育出版(亚洲)公司合作出版。此版本仅限在中华人民共和国境内(不包括中国香港、澳门特别行政区及中国台湾地区)针对教育及培训机构之销售。未经许可之出口,视为违反著作权法,将受法律之制裁。

未经出版者预先书面许可,不得以任何方式复制或抄袭本书的任何部分。

北京市版权局著作权合同登记号 图字:01-2007-4047

本书封面贴有 McGraw-Hill 公司防伪标签,无标签者不得销售。

版权所有,侵权必究。侵权举报电话:010-62782989 13701121933

图书在版编目(CIP)数据

现代数字电子学:第3版=Modern Digital Electronics, 3e: 英文/()杰恩(JAIN, R. P.)著.
—北京:清华大学出版社,2008.4

(清华版双语教学用书)

ISBN 978-7-302-17068-6

I. 现… II. 杰… III. 数字电路—电子技术—高等学样—教材—英文 IV. TN79

中国版本图书馆 CIP 数据核字(2008)第 022196 号

责任编辑:王一玲

责任印制:杨 艳

出版发行:清华大学出版社

地 址:北京清华大学学研大厦 A 座

<http://www.tup.com.cn>

邮 编:100084

社 总 机:010-62770175

邮 购:010-62786544

投稿与读者服务:010-62776969, c-service@tup.tsinghua.edu.cn

质 量 反 馈:010-62772015, zhiliang@tup.tsinghua.edu.cn

印 装 者:北京嘉实印刷有限公司

经 销:全国新华书店

开 本:200×260 印 张:35.75

版 次:2008 年 4 月第 1 版 印 次:2008 年 4 月第 1 次印刷

印 数:1~3000

定 价:49.80 元

本书如存在文字不清、漏印、缺页、倒页、脱页等印装质量问题,请与清华大学出版社出版部联系调换。联系电话:(010)62770177 转 3103 产品编号:026163-01

Modern Digital Electronics, Third Edition

影印版序

在教育部的倡导和推动下,许多高等学校都在电子技术课程的教学开展了不同形式的双语教学试点工作。实践表明,采用双语教学是提高学生专业外语水平的一种有效途径。而能否找到一本合适的外语教材,将直接影响到教学效果,有时甚至会成为双语教学成败的关键。

就数字电子技术基础课程而言,这几年国内各家出版社引进的英语原版教材不下几十种,其中尤以美国的教材为多。由于国外电子技术课程的设置和内容的划分与我国的不完全相同,所以多数引进的英语教材在内容上与教育部主持制定的《数字电子技术课程教学基本要求》不完全吻合。主要表现在有些英语教材中缺少 A/D、D/A 转换和脉冲波形的产生和变换这两部分内容;有些教材只讲逻辑设计而对于电路的基础知识讲得过于简单,甚至根本不讲。此外这些英语教材的篇幅往往很大,容易使学生望而生畏。因此,用它们作数字电子技术基础课程的主教材都不够理想。

在这本由 R P Jain 编著的《Modern Digital Electronics》一书中则不存在上面所说的各种问题。将原书的第 13 章 Fundamentals of Microprocessors 略去以后,其内容完全符合《基本要求》所规定的内容,而且正文部分只有五百多页。该书内容精练,概念表述清晰,系统性强。无论是作为作数字电子技术课程双语教学的主教材,还是作为一般数字电子技术基础课程的外文参考书,该书的出版都为我们提供了一个更为理想的选择。

阎 石

清华大学自动化系

2007 年 5 月

PREFACE TO THE THIRD EDITION

The tremendous power and usefulness of digital techniques and systems can be seen from the wide variety of industrial machinery, computers, microprocessors, household appliances (washing machines, refrigerators, digital TVs, etc.), medical equipment, internet, e-banking, e-business, e-governance, etc. which are based on the principles of digital electronics. The areas of applications of digital electronics have been increasing day by day, resulting in an unprecedented interest in the subject. In fact, digital systems have invaded all walks of life that has created digital revolution.

One of the most important reason for the unprecedented growth of digital electronics is the advent of integrated circuits (ICs). Developments in the IC technology have made it possible to fabricate complex digital circuits, such as microprocessors, memories, complex programmable logic devices (CPLDs) and field programmable gate arrays (FPGAs), etc.

The wonderchip **microprocessor** has been the most fantastic development of the recent years. No other single development has affected our lives as much as the microprocessor in such a short time. Its ever-increasing applications have resulted in developments which were simply unheard of till a few years ago. The emergence of various programmable logic devices have resulted in significant changes in the design methodologies of digital systems. The designers of modern digital systems in industry rarely use conventional manual techniques. Instead, computer aided design (CAD) tools are used. But this has not made the basic concepts and the manual techniques of digital theory and practice obsolete. Rather, the manual techniques are the foundation of CAD tools and they provide a clear insight into the CAD tools. Therefore, it is very essential to have a strong foundation of the basic digital techniques for making effective use of automation in design.

This has made it imperative for all those who aspire to design, develop, test, and maintain various electronic systems to learn the principles of modern digital devices and systems.

The third edition of the book deals with the subject of digital techniques and systems from the basic circuits (gates) to small scale integrated circuits (SSI), medium scale integrated circuits (MSI), large scale integrated circuits (LSI), and very large scale integrated circuits (VLSI). Computer aided design concepts, CAD tools and hardware description language VHDL have been introduced to familiarize the readers with the CAD techniques.

This book is self contained and is suitable for a course in digital electronics and logic design for electrical, electronics, computer and other engineering disciplines and computer science programmes. Students of physics specializing in electronics will also find the book useful. For experimental work using SSI and MSI devices, the reader is advised to refer to Jain and Anand, *Digital Electronics Practice Using Integrated Circuits*, Tata McGraw-Hill, New Delhi, 1983.

The book has been systematically organized and the presentation has been kept at a level suitable for a student with the basic knowledge of circuit theory and electronics.

Chapter 1 introduces the fundamental concepts of digital electronics, advantages of digital systems, and the basic digital circuits. Various number systems and commonly used codes in digital systems and microprocessors have been discussed in Chapter 2. Error-detecting and error-correcting codes have also been included in this edition. Chapter 3 reviews semiconductor devices from the point of view of their applications in digital circuits. Based on these devices, various digital circuits, referred to as logic families, have been discussed in Chapter 4. Availability of various digital functions in ICs have changed the teaching of digital electronics from the good old style using discrete devices to a new style using modern digital ICs. For example, now it is no more important to minimize the number of gates for the design of a digital circuit, since a number of similar gates are available in a single IC chip; rather it has become necessary to minimize the number of IC packages. Thus the designers of digital systems have to be thoroughly familiar with the principles of operation and flexibilities available in various ICs in order to optimize the design of digital systems from the point of view of cost, space, power requirement, speed of operation, etc. This chapter also deals with the interfacing problems between ICs of the same logic families and between those of different logic families to obtain maximum benefits.

Chapter 5 deals with the conventional methods of combinational circuit design. Quine-Mccluskey method has also been included in this edition.

Combinational logic design using MSI circuits is covered in Chapter 6, which is important for the design of digital systems considering the simplicity in design, cost, space, power requirement, speed and other factors.

Chapter 7 introduces the basic building block of a sequential circuit—the FLIP-FLOP. All types of FLIP-FLOPs with their excitation tables and triggering methods have been discussed in detail. Sequential logic design has been discussed in Chapter 8. Here again, both the approaches, namely conventional design using FLIP-FLOPs and the modern approach using available MSI circuits, have been discussed. Design of synchronous sequential as well as asynchronous sequential circuits have been discussed.

Chapter 9 deals with timing circuits and their applications which are essential to a digital system.

The analog-to-digital (A/D) and digital-to-analog (D/A) converters form an important part of many digital systems and the commonly used techniques for such conversions have been discussed in Chapter 10.

Chapter 11 deals with semiconductor memories which have assumed an important role in present-day digital systems. Various semiconductor memories, such as static and dynamic shift registers, static and dynamic RAMs, ROM, PROM, EPROM, EAROM, CAM, CCD, have been discussed in detail. Programming techniques used for programmable ROMs and erasing techniques used for erasable programmable ROMs have also been discussed.

Chapter 12 presents various programmable logic devices (PLDs), such as programmable logic arrays (PLA), programmable array logic (PAL), Complex Programmable logic devices (CPLDs) and field programmable gate array (FPGA) devices. These devices are extremely useful for the design of complex digital circuits.

Chapter 13 introduces computer aided design (CAD) approach to digital system design. CAD tools needed for this purpose have been discussed. The VHDL, a hardware description language has been introduced, which is the basic requirement of designing using CAD tools.

Glossary of the important terms used in the book and Review Questions with answers for each chapter have been included to enhance the understanding of the users.

The solution manual for the third edition is also available with the publishers, for the teachers who adopt this book.

R P JAIN

CONTENTS

1. FUNDAMENTAL CONCEPTS

I

- 1.1 Introduction 1
- 1.2 Digital Signals 3
- 1.3 Basic Digital Circuits 4
 - 1.3.1 The AND Operation 4
 - 1.3.2 The OR Operation 5
 - 1.3.3 The NOT Operation 5
- 1.4 NAND and NOR Operations 6
 - 1.4.1 The NAND Operation 6
 - 1.4.2 The NOR Operation 7
- 1.5 Exclusive-OR Operation 9
- 1.6 Boolean Algebra 9
- 1.7 Examples of IC Gates 12
- 1.8 Summary 13
 - Glossary 14
 - Review Questions 16
 - Problems 17

2. NUMBER SYSTEMS AND CODES

21

- 2.1 Introduction 21
- 2.2 Number Systems 22

2.3	Binary Number System	22
2.3.1	Binary-to-Decimal Conversion	23
2.3.2	Decimal-to-Binary Conversion	24
2.4	Signed Binary Numbers	26
2.4.1	Sign-Magnitude Representation	26
2.4.2	One's Complement Representation	27
2.4.3	Two's Complement Representation	28
2.5	Binary Arithmetic	30
2.5.1	Binary Addition	30
2.5.2	Binary Subtraction	31
2.5.3	Binary Multiplication	32
2.5.4	Binary Division	32
2.6	2's Complement Arithmetic	32
2.6.1	Subtraction Using 2's Complement	33
2.6.2	Addition/Subtraction in 2's Complement Representation	33
2.7	Octal Number System	34
2.7.1	Octal-to-Decimal Conversion	34
2.7.2	Decimal-to-Octal Conversion	35
2.7.3	Octal-to-Binary Conversion	36
2.7.4	Binary-to-Octal Conversion	36
2.7.5	Octal Arithmetic	37
2.7.6	Applications of Octal Number System	38
2.8	Hexadecimal Number System	38
2.8.1	Hexadecimal-to-Decimal Conversion	39
2.8.2	Decimal-to-Hexadecimal Conversion	39
2.8.3	Hexadecimal-to-Binary Conversion	40
2.8.4	Binary-to-Hexadecimal Conversion	40
2.8.5	Conversion from Hex-to-Octal and Vice-Versa	41
2.8.6	Hexadecimal Arithmetic	42
2.9	Codes	42
2.9.1	Straight Binary Code	43
2.9.2	Natural BCD Code	43
2.9.3	Excess-3 Code	43
2.9.4	Gray Code	44
2.9.5	Octal Code	45
2.9.6	Hexadecimal Code	45
2.9.7	Alphanumeric Codes	46
2.10	Error Detecting and Correcting Codes	49
2.10.1	Error-detecting Codes	49
2.10.2	Error-correcting Codes	51
2.11	Summary	54
	Glossary	54
	Review Questions	56
	Problems	57

3. SEMICONDUCTOR DEVICES—SWITCHING MODE OPERATION**58**

- 3.1 Introduction 59
- 3.2 Semiconductors 60
- 3.3 *p-n* Junction Diode 61
 - 3.3.1 Forward Bias 62
 - 3.3.2 Reverse Bias 63
 - 3.3.3 The Volt-Ampere Characteristic 64
 - 3.3.4 Zener Diode 64
 - 3.3.5 Transition Capacitance of a *p-n* Junction Diode 65
 - 3.3.6 Switching Characteristics of a Semiconductor Diode 65
- 3.4 Schottky Diode 67
- 3.5 Bipolar Junction Transistor 67
 - 3.5.1 Transistor Configurations 69
 - 3.5.2 Transistor as a Switch 70
 - 3.5.3 CE Transistor Switch 71
 - 3.5.4 Switching Speed of BJT 72
- 3.6 Schottky Transistor 75
- 3.7 Field-Effect Transistor 75
 - 3.7.1 Junction Field-Effect Transistor 75
 - 3.7.2 Metal-Oxide-Semiconductor Field-Effect Transistor 77
 - 3.7.3 FET Switches 79
 - 3.7.4 Complementary MOSFET (CMOS) 82
- 3.8 Summary 83
 - Glossary 83
 - Review Questions 83
 - Problems 84

4. DIGITAL LOGIC FAMILIES**89**

- 4.1 Introduction 89
 - 4.1.1 Bipolar Logic Families 89
 - 4.1.2 Unipolar Logic Families 90
- 4.2 Characteristics of Digital ICs 90
 - 4.2.1 Speed of Operation 91
 - 4.2.2 Power Dissipation 91
 - 4.2.3 Figure of Merit 91
 - 4.2.4 Fan-Out 91
 - 4.2.5 Current and Voltage Parameters 91
 - 4.2.6 Noise Immunity 92
 - 4.2.7 Operating Temperature 92
 - 4.2.8 Power Supply Requirements 93
 - 4.2.9 Flexibilities Available 93

- 4.3 Resistor-Transistor Logic (RTL) 93
 - 4.3.1 Logic Operation 93
 - 4.3.2 Loading Considerations 93
 - 4.3.3 Noise Margins 95
 - 4.3.4 Propagation Delay Time 95
 - 4.3.5 Current Source Logic 95
 - 4.3.6 Wired-Logic 95
- 4.4 Direct-Coupled Transistor Logic (DCTL) 96
- 4.5 Integrated-Injection Logic (I²L) 96
 - 4.5.1 I²L Inverter 97
 - 4.5.2 I²L Configuration 97
 - 4.5.3 Fabrication of I²L 99
- 4.6 Diode-Transistor Logic (DTL) 100
 - 4.6.1 Operation of DTL NAND Gate 101
 - 4.6.2 Propagation Delays 102
 - 4.6.3 Current Sink Logic 102
 - 4.6.4 Wired-Logic 103
 - 4.6.5 Modified Integrated DTL NAND Gate 103
- 4.7 High-Threshold Logic (HTL) 103
- 4.8 Transistor-transistor Logic (TTL) 105
 - 4.8.1 Operation of TTL NAND Gate 105
 - 4.8.2 Active Pull-up 106
 - 4.8.3 Wired-AND 108
 - 4.8.4 Open-Collector Output 108
 - 4.8.5 Unconnected Inputs 108
 - 4.8.6 Clamping Diodes 108
- 4.9 Schottky TTL 108
- 4.10 5400/7400 TTL Series 108
- 4.11 Emitter-Coupled Logic (ECL) 110
 - 4.11.1 Fan-Out 113
 - 4.11.2 Wired-OR Logic 113
 - 4.11.3 Open-Emitter Outputs 114
 - 4.11.4 Unconnected Inputs 114
 - 4.11.5 ECL Families 114
- 4.12 Interfacing ECL and TTL 114
 - 4.12.1 TTL-to-ECL Translator 114
 - 4.12.2 ECL-to-TTL Translator 115
- 4.13 MOS Logic 115
 - 4.13.1 MOSFET NAND and NOR Gates 117
 - 4.13.2 Fan-Out 118
 - 4.13.3 Propagation Delay Time 118
 - 4.13.4 Power Dissipation 119
 - 4.13.5 Unconnected Inputs 119

- 4.14 CMOS Logic 119
 - 4.14.1 CMOS Inverter 119
 - 4.14.2 CMOS NAND and NOR Gates 119
 - 4.14.3 CMOS Transmission Gate 120
 - 4.14.4 Noise Margin 120
 - 4.14.5 Unconnected Inputs 121
 - 4.14.6 Wired-Logic 121
 - 4.14.7 Open-Drain Outputs 122
 - 4.14.8 54C00/74C00 CMOS Series 122
- 4.15 Interfacing CMOS and TTL 123
 - 4.15.1 CMOS Driving TTL 123
 - 4.15.2 TTL Driving CMOS 124
- 4.16 Interfacing CMOS and ECL 125
- 4.17 Tri-State Logic 126
 - 4.17.1 TSL Inverter 126
- 4.18 Summary 128
 - Glossary 129
 - Review Questions 133
 - Problems 134

5. COMBINATIONAL LOGIC DESIGN

138

- 5.1 Introduction 138
- 5.2 Standard Representations for Logical Functions 139
- 5.3 Karnaugh Map Representation of Logical Functions 146
 - 5.3.1 Representation of Truth Table on K-Map 148
 - 5.3.2 Representation of Standard SOP Form on K-Map 149
 - 5.3.3 Representation of Standard POS Form on K-Map 150
- 5.4 Simplification of Logical Functions Using K-Map 150
 - 5.4.1 Grouping Two Adjacent Ones 151
 - 5.4.2 Grouping Four Adjacent Ones 152
 - 5.4.3 Grouping Eight Adjacent Ones 154
 - 5.4.4 Grouping 2, 4, and 8 Adjacent Zeros 155
- 5.5 Minimization of Logical Functions Specified in Minterms/Maxterms or Truth Table 155
 - 5.5.1 Minimization of SOP Form 155
 - 5.5.2 Minimization of POS Form 158
- 5.6 Minimization of Logical Functions not Specified in Minterms/Maxterms 159
- 5.7 Don't-Care Conditions 161
- 5.8 Design Examples 163
 - 5.8.1 Arithmetic Circuits 163
 - 5.8.2 BCD-to-7-Segment Decoder 166

5.9	EX-OR AND EX-NOR Simplification of K-Maps	168
5.9.1	Diagonal and Offset Adjacencies of Groups of Ones	171
5.10	Five- and Six-Variable K-maps	175
5.11	Quine-McCluskey Minimization Technique	178
5.12	Summary	185
	Glossary	186
	Review Questions	187
	Problems	187

6. COMBINATIONAL LOGIC DESIGN USING MSI CIRCUITS

191

6.1	Introduction	191
6.2	Multiplexers and Their Use in Combinational Logic Design	191
6.2.1	Multiplexer	191
6.2.2	Combinational Logic Design Using Multiplexers	192
6.2.3	Multiplexer Tree	196
6.3	Demultiplexers/Decoders and Their Use in Combinational Logic Design	196
6.3.1	Demultiplexer	196
6.3.2	Demultiplexer Tree	199
6.4	Adders and Their Use as Subtractors	201
6.4.1	Adder with Look-Ahead Carry	202
6.4.2	Cascading of Adders	203
6.4.3	Subtraction Using Adder	205
6.5	BCD Arithmetic	205
6.5.1	BCD Adder	206
6.5.2	BCD Subtractor	206
6.6	Arithmetic Logic Unit (ALU)	209
6.7	Digital Comparators	212
6.8	Parity Generators/Checkers	215
6.9	Code Converters	217
6.9.1	BCD-to-Binary Converter	218
6.9.2	Binary-to-BCD Converter	222
6.10	Priority Encoders	226
6.10.1	Decimal-to-BCD Encoder	226
6.10.2	Octal-to-Binary Encoder	227
6.11	Decoder/Drivers for Display Devices	228
6.11.1	BCD-to Decimal Decoder/Driver	228
6.11.2	BCD-to-7-Segment Decoder/Driver	229
6.12	Summary	233
	Glossary	233
	Review Questions	234
	Problems	234

7. FLIP-FLOPS**237**

- 7.1 Introduction 237
- 7.2 A 1-Bit Memory Cell 239
- 7.3 Clocked *S-R* FLIP-FLOP 240
 - 7.3.1 Preset and Clear 241
- 7.4 *J-K* FLIP-FLOP 243
 - 7.4.1 The Race-Around Condition 244
 - 7.4.2 The Master-Slave *J-K* FLIP-FLOP 245
- 7.5 *D*-Type FLIP-FLOP 246
- 7.6 *T*-Type FLIP-FLOP 247
- 7.7 Excitation Table of FLIP-FLOP 248
- 7.8 Clocked FLIP-FLOP Design 249
 - 7.8.1 Conversion From One Type of FLIP-FLOP to Another Type 250
- 7.9 Edge-Triggered FLIP-FLOPS 252
- 7.10 Applications of FLIP-FLOPS 255
 - 7.10.1 Bounce-Elimination Switch 255
 - 7.10.2 Registers 256
 - 7.10.3 Counters 257
 - 7.10.4 Random-Access Memory 258
- 7.11 Summary 259
 - Glossary 260
 - Review Questions 262
 - Problems 262

8. SEQUENTIAL LOGIC DESIGN**267**

- 8.1 Introduction 267
- 8.2 Registers 268
 - 8.2.1 Shift Register 269
- 8.3 Applications of Shift Registers 272
 - 8.3.1 Delay Line 272
 - 8.3.2 Serial-to-Parallel Converter 272
 - 8.3.3 Parallel-to-Serial Converter 272
 - 8.3.4 Ring Counter 273
 - 8.3.5 Twisted-Ring Counter 273
 - 8.3.6 Sequence Generator 274
- 8.4 Ripple or Asynchronous Counters 276
 - 8.4.1 UP/DOWN Counters 279
 - 8.4.2 Modulus of the Counter 280
 - 8.4.3 54/74 Series Asynchronous Counter ICs 281
- 8.5 Synchronous Counters 287
 - 8.5.1 Synchronous Counter Design 288

- 8.5.2 Lock Out 292
- 8.5.3 54/74 Series Synchronous Counter ICs 292
- 8.6 Clocked Sequential Circuit Design 302
- 8.7 Asynchronous Sequential Circuits 306
 - 8.7.1 Asynchronous versus Synchronous Sequential Circuits 306
 - 8.7.2 Applications of Asynchronous Sequential Circuits 306
 - 8.7.3 Asynchronous Sequential Machine Modes 308
 - 8.7.4 Analysis of Asynchronous Sequential Machines 309
 - 8.7.5 Asynchronous Sequential Circuit Design 321
- 8.8 Summary 327
 - Glossary 328
 - Review Questions 330
 - Problems 330

9. TIMING CIRCUITS

335

- 9.1 Introduction 335
- 9.2 Applications of Logic Gates in Timing Circuits 336
 - 9.2.1 Free-Running Multivibrator 336
 - 9.2.2 Monostable Multivibrator 337
- 9.3 OP AMP and its Applications in Timing Circuits 338
 - 9.3.1 OP AMP Comparator 339
 - 9.3.2 Regenerative Comparator (Schmitt Trigger) 342
 - 9.3.3 Astable (or Free-Running) Multivibrator 345
 - 9.3.4 Monostable Multivibrator 347
- 9.4 Schmitt Trigger ICs 349
 - 9.4.1 Schmitt Trigger Square-Wave Generator 349
- 9.5 Monostable Multivibrator ICs 350
 - 9.5.1 74121 Monostable Multivibrator 350
 - 9.5.2 Retriggerable Monostable Multivibrators (74122 and 74123) 352
 - 9.5.3 Non-retriggerable Monostable Multivibrator with Clear (74221) 354
 - 9.5.4 Astable Multivibrator Using One-Shots 357
- 9.6 555 Timer 358
 - 9.6.1 Monostable Multivibrator 359
 - 9.6.2 Astable Multivibrator 360
- 9.7 Summary 362
 - Glossary 362
 - Review Questions 363
 - Problems 364

10. A/D AND D/A CONVERTERS

366

- 10.1 Introduction 366
- 10.2 Digital-to-Analog Converters 367

- 10.2.1 Weighted-Resistor D/A Converter 368
- 10.2.2 R - $2R$ Ladder D/A Converter 372
- 10.2.3 Specifications for D/A Converters 376
- 10.3 An Example of D/A Converter IC 378
 - 10.3.1 Digital Input Codes 379
 - 10.3.2 Analog Output 380
 - 10.3.3 Calibration 380
- 10.4 Sample-And-Hold 382
 - 10.4.1 Sample-and-Hold Circuit 382
- 10.5 Analog-to-Digital Converters 383
 - 10.5.1 Quantization and Encoding 383
 - 10.5.2 Parallel-Comparator A/D Converter 385
 - 10.5.3 Successive-Approximation A/D Converter 385
 - 10.5.4 Counting A/D Converter 389
 - 10.5.5 Dual-Slope A/D Converter 390
 - 10.5.6 A/D Converter Using Voltage-to-Frequency Conversion 392
 - 10.5.7 A/D Converter Using Voltage-to-Time Conversion 393
 - 10.5.8 Specifications of A/D Converters 395
- 10.6 An Example of A/D Converter IC 395
 - 10.6.1 Operation 395
 - 10.6.2 Digital Output 395
 - 10.6.3 Analog Input 396
 - 10.6.4 Calibration 396
- 10.7 Summary 397
 - Glossary 398
 - Review Questions 399
 - Problems 399

11. SEMICONDUCTOR MEMORIES

401

- 11.1 Introduction 401
- 11.2 Memory Organization and Operation 401
 - 11.2.1 Write Operation 403
 - 11.2.2 Read Operation 405
- 11.3 Expanding Memory Size 408
 - 11.3.1 Expanding Word Size 408
 - 11.3.2 Expanding Word Capacity 408
- 11.4 Classification and Characteristics of Memories 410
 - 11.4.1 Principle of Operation 410
 - 11.4.2 Physical Characteristics 412
 - 11.4.3 Mode of Access 413
 - 11.4.4 Fabrication Technology 413

- 11.5 Sequential Memory 413
 - 11.5.1 Static Shift Register 414
 - 11.5.2 Dynamic Shift Register 414
- 11.6 Read-Only Memory 419
 - 11.6.1 ROM Organization 421
 - 11.6.2 Programming Mechanisms 423
 - 11.6.3 ROM ICs 426
- 11.7 Read and Write Memory 426
 - 11.7.1 Bipolar RAM Cell 428
 - 11.7.2 MOS RAMs 430
 - 11.7.3 RAM ICs 433
- 11.8 Content Addressable Memory 433
 - 11.8.1 Operation of CAM 435
- 11.9 Charge Coupled Device Memory 440
 - 11.9.1 Basic Concept of CCD 440
 - 11.9.2 Operation of CCD 441
 - 11.9.3 A Practical CCD Memory Device 442
- 11.10 Summary 443
 - Glossary 444
 - Review Questions 445
 - Problems 446

12. PROGRAMMABLE LOGIC DEVICES

449

- 12.1 Introduction 449
- 12.2 ROM as a PLD 451
- 12.3 Programmable Logic Array 451
 - 12.3.1 Input Buffer 452
 - 12.3.2 AND Matrix 453
 - 12.3.3 OR Matrix 454
 - 12.3.4 Invert/Non-Invert Matrix 456
 - 12.3.5 Output Buffer 456
 - 12.3.6 Output through FLIP-FLOPs and Buffers 457
 - 12.3.7 Programming the PLA 457
 - 12.3.8 Expanding PLA Capacity 457
 - 12.3.9 Applications of PLAs 458
 - 12.3.10 Available PLAs 465
- 12.4 Programmable Array Logic 465
 - 12.4.1 Registered PALs 469
 - 12.4.2 Configurable PALs 469
 - 12.4.3 Generic Array Logic Devices 472
 - 12.4.4 EX-OR PALs 473
 - 12.4.5 Available PALs 475
 - 12.4.6 Simple PLDs (SPLDs) 478