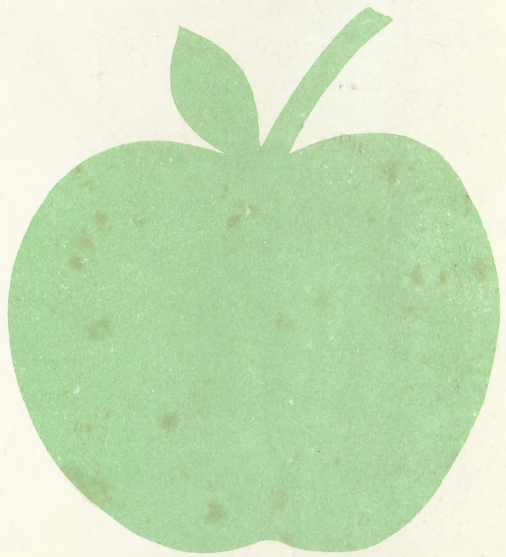
538

# 微型计算机Apple Ⅱ的电路分析（附图）

# THE APPLE II CIRCUIT DESCRIPTION



四川科学技术出版社

026652

TP36
8044

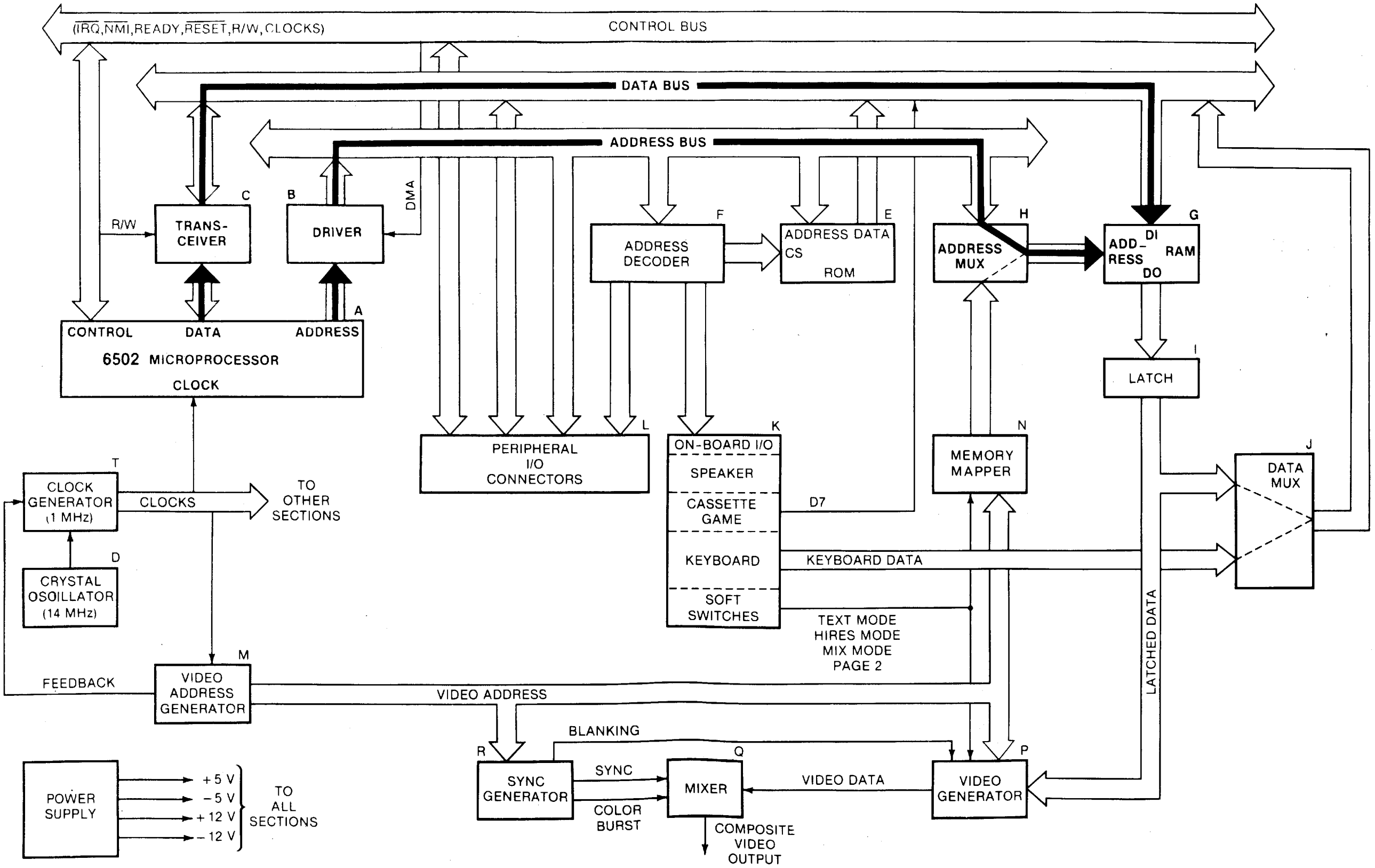



Fig. 2-3. RAM write-cycle path. 图 2 - 3 RAM 写周期的路线

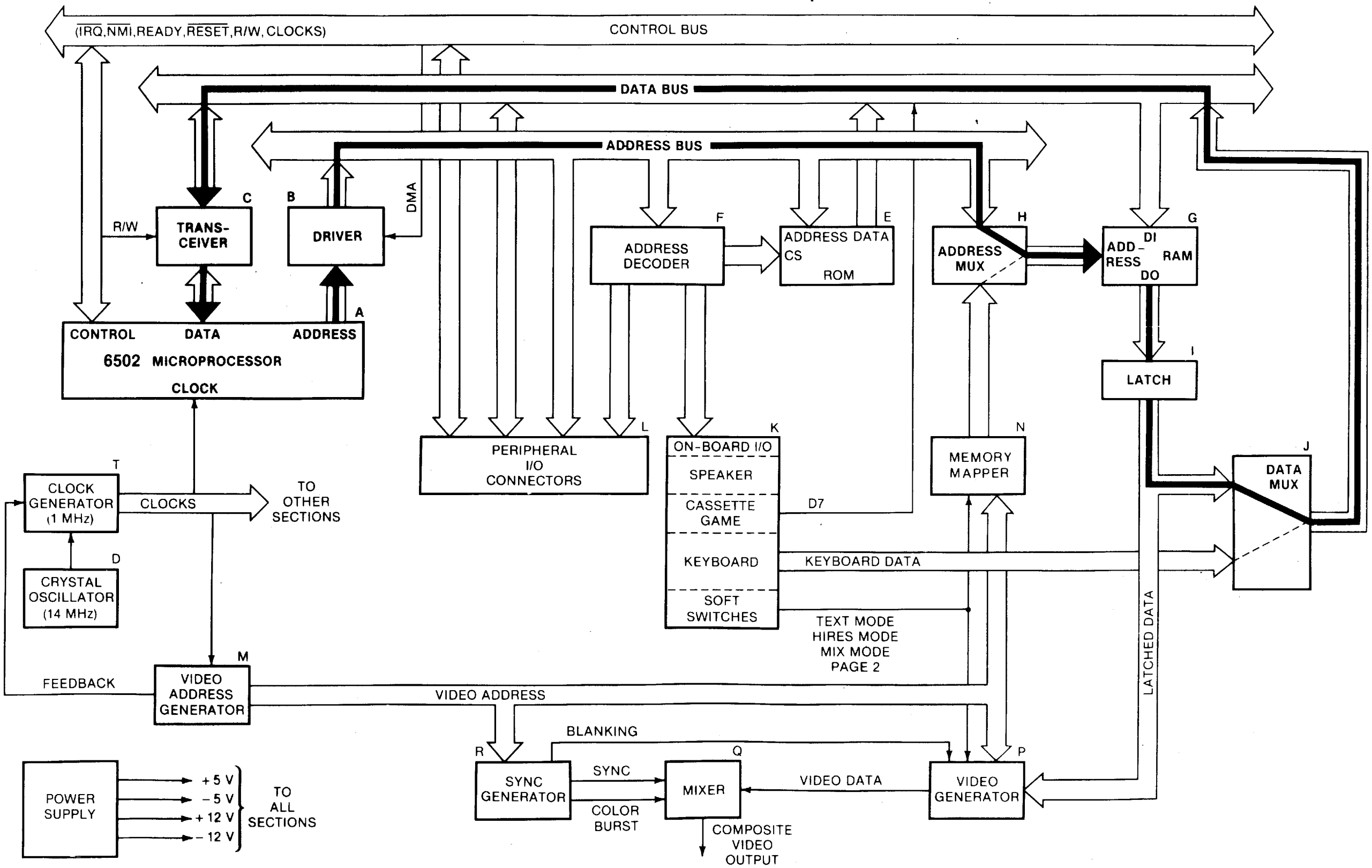



Fig. 2-4. RAM read-cycle path. **图 2 - 4** RAM 读周期的路线

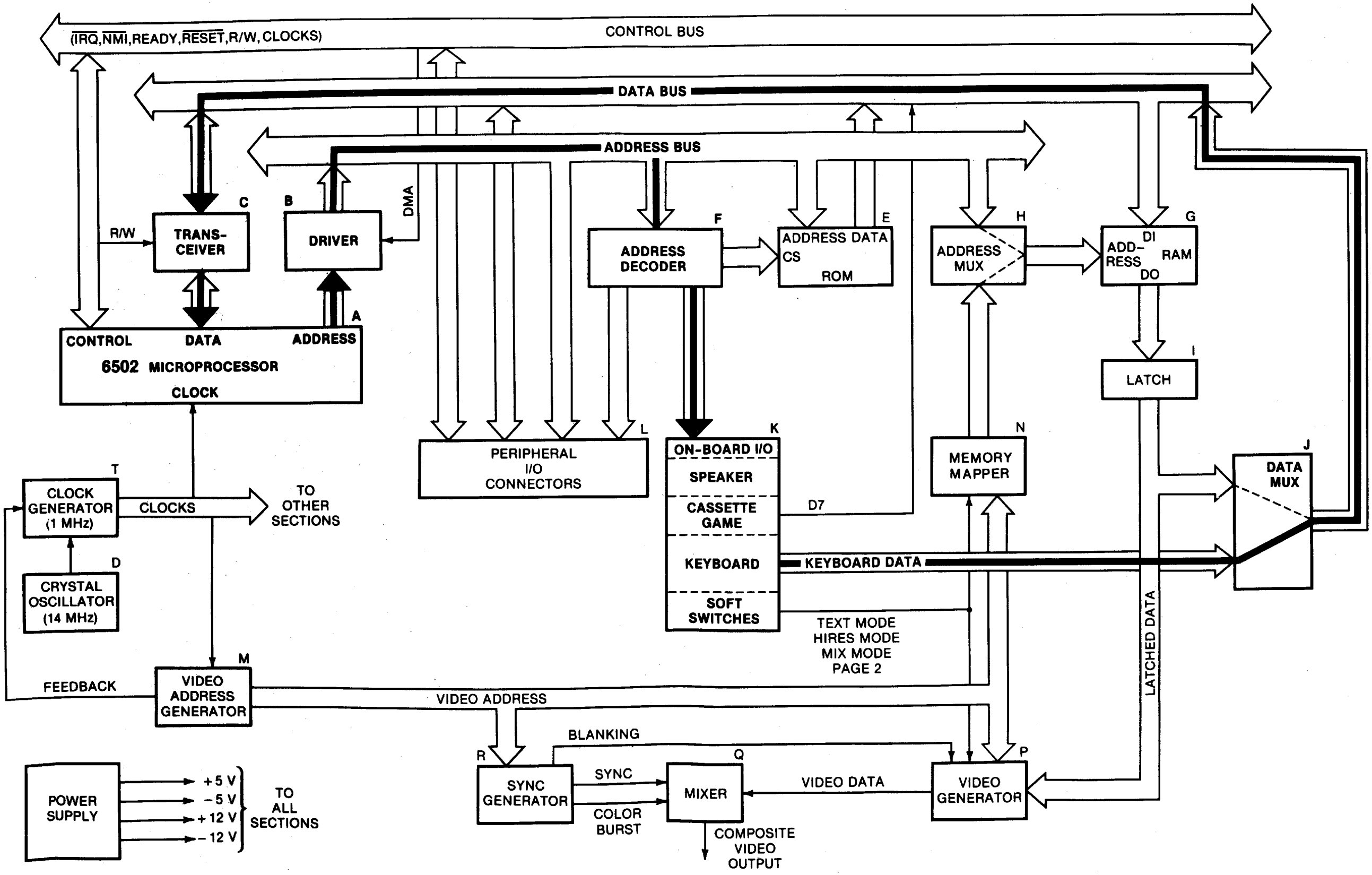



**Fig. 2-5.** Keyboard read-cycle path. **图 2 - 5** 键盘读周期的路线

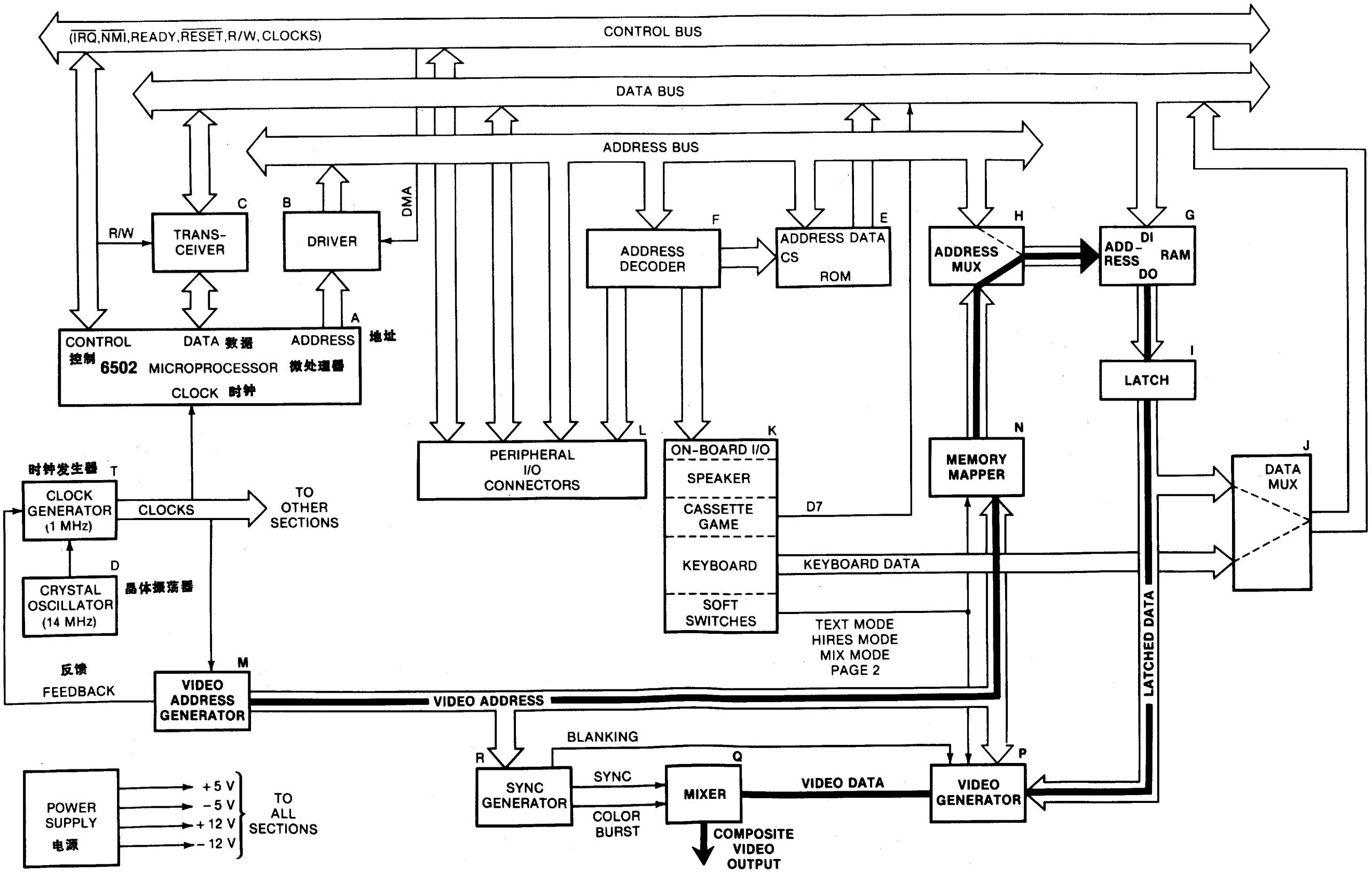
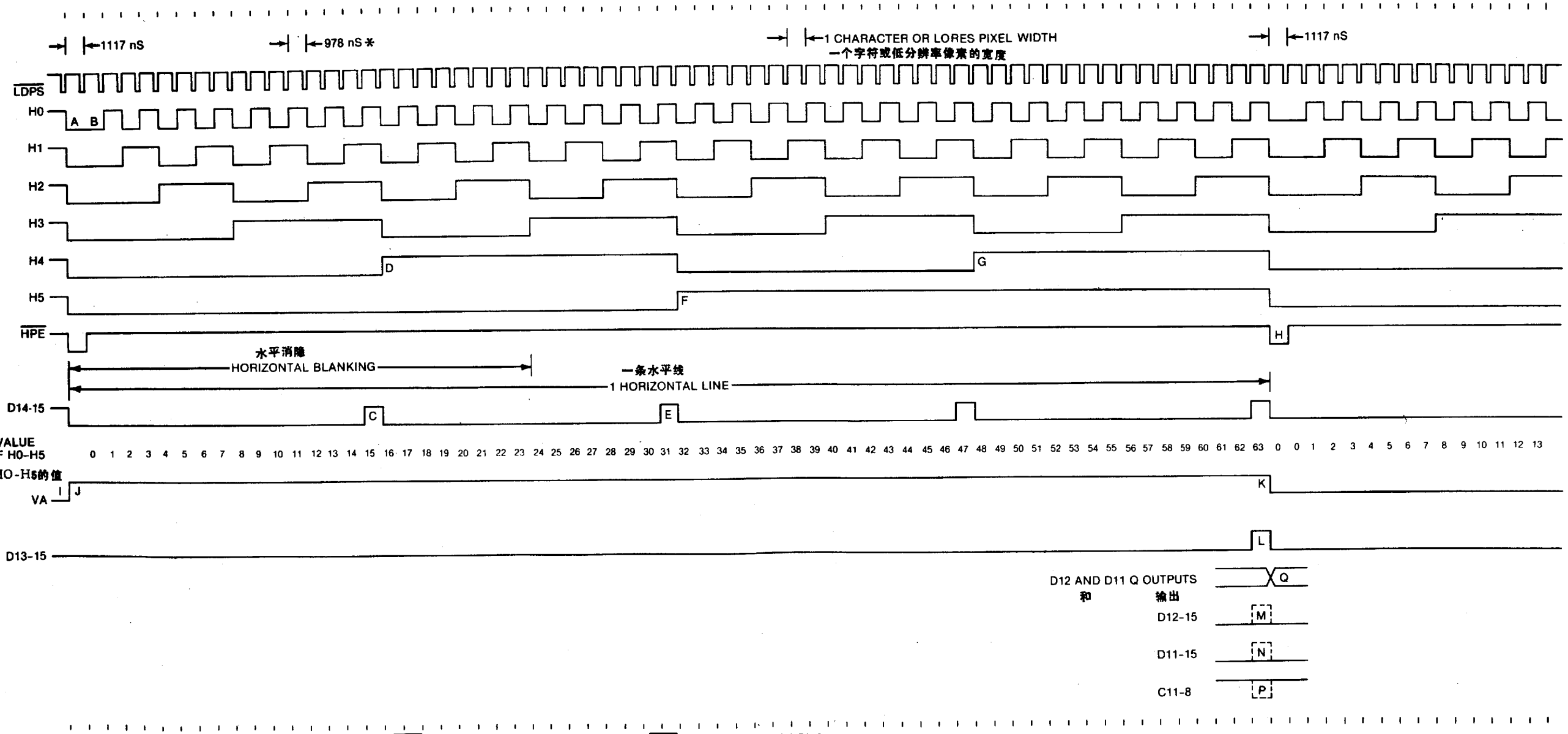



Fig. 2-6. Video-cycle path. 图 2 - 6 视频周期的路线



此为试读，需要完整PDF请访问：www.ertongbook.com




* 64 OUT OF 65 $\overline{\text{LDPS}}$ CYCLES ARE 978 nS LONG, THE 65TH $\overline{\text{LDPS}}$ CYCLE IS 1117 nS LONG.

65个$\overline{\text{LDPS}}$周期中的64个为978ns宽，第65个$\overline{\text{LDPS}}$周期为1117ns宽

Fig. 3-4. Horizontal timing. 图 3 - 4 水平时间关系

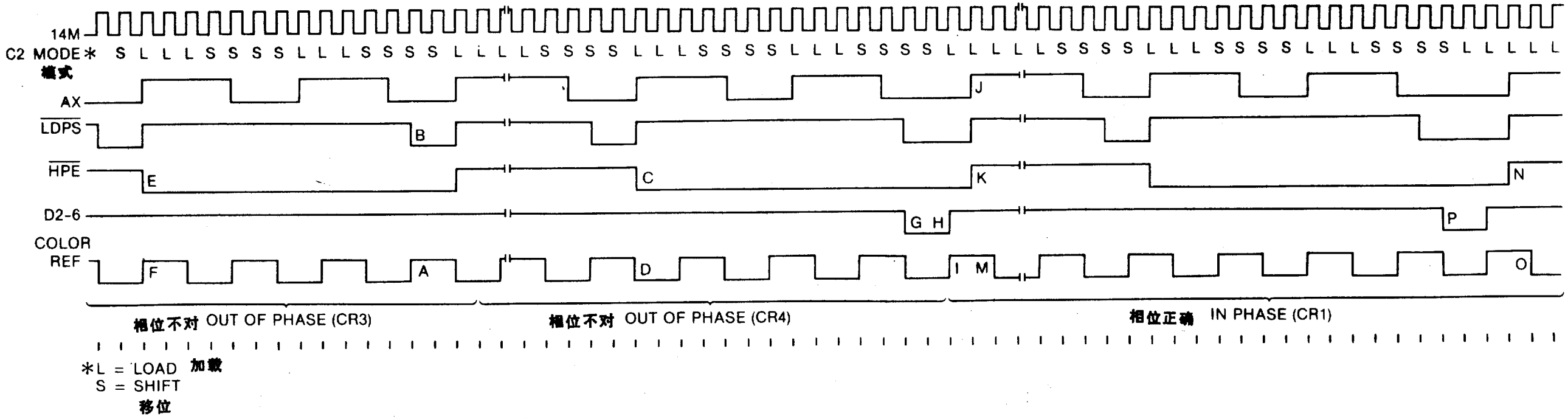
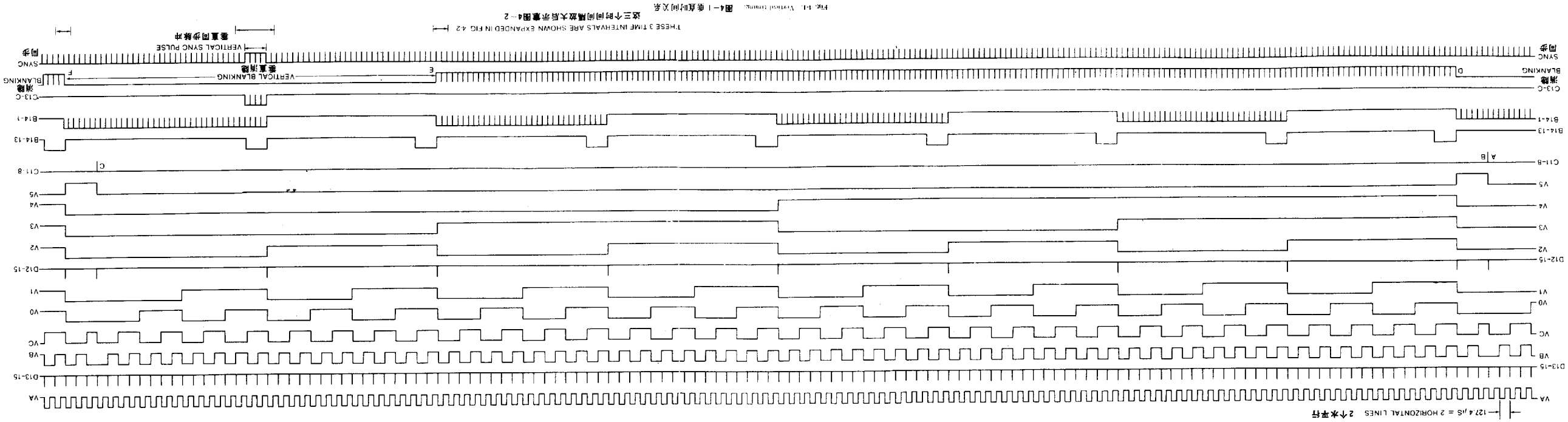



**Fig. 3-7.** Clock synchronization—CR3 and CR4. **图 3－7** 时钟的同步—CR 3 和CR 4


同步
SYNC
消隐
BLANKING
C13-C
B14-1
B14-13
C11-B
A|B
V5
V4
V3
V2
D12-15
V1
V0
VC
VB
D13-15
VA
VERTICAL SYNC PULSE
垂直同步脉冲
VERTICAL BLANKING
垂直消隐
THESE 3 TIME INTERVALS ARE SHOWN EXPANDED IN FIG. 4-2
这三个时间间隔放大后示意图4—2
FIG. 4-1 Vertical timing
图4—1 垂直时间关系
2↑*平行
127.4 μS = 2 HORIZONTAL LINES

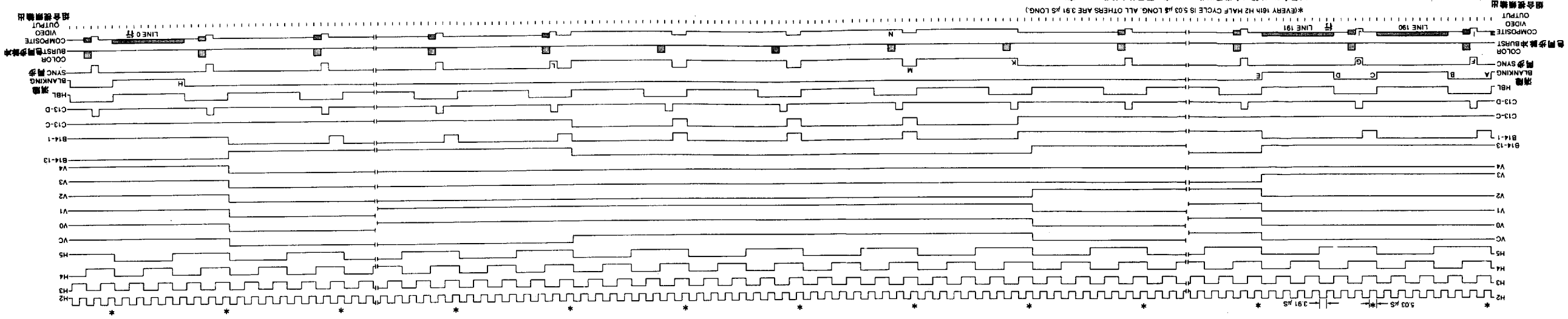



Fig. 4-2. Vertical retrace interval 图4--2 垂直回扫时间间隔

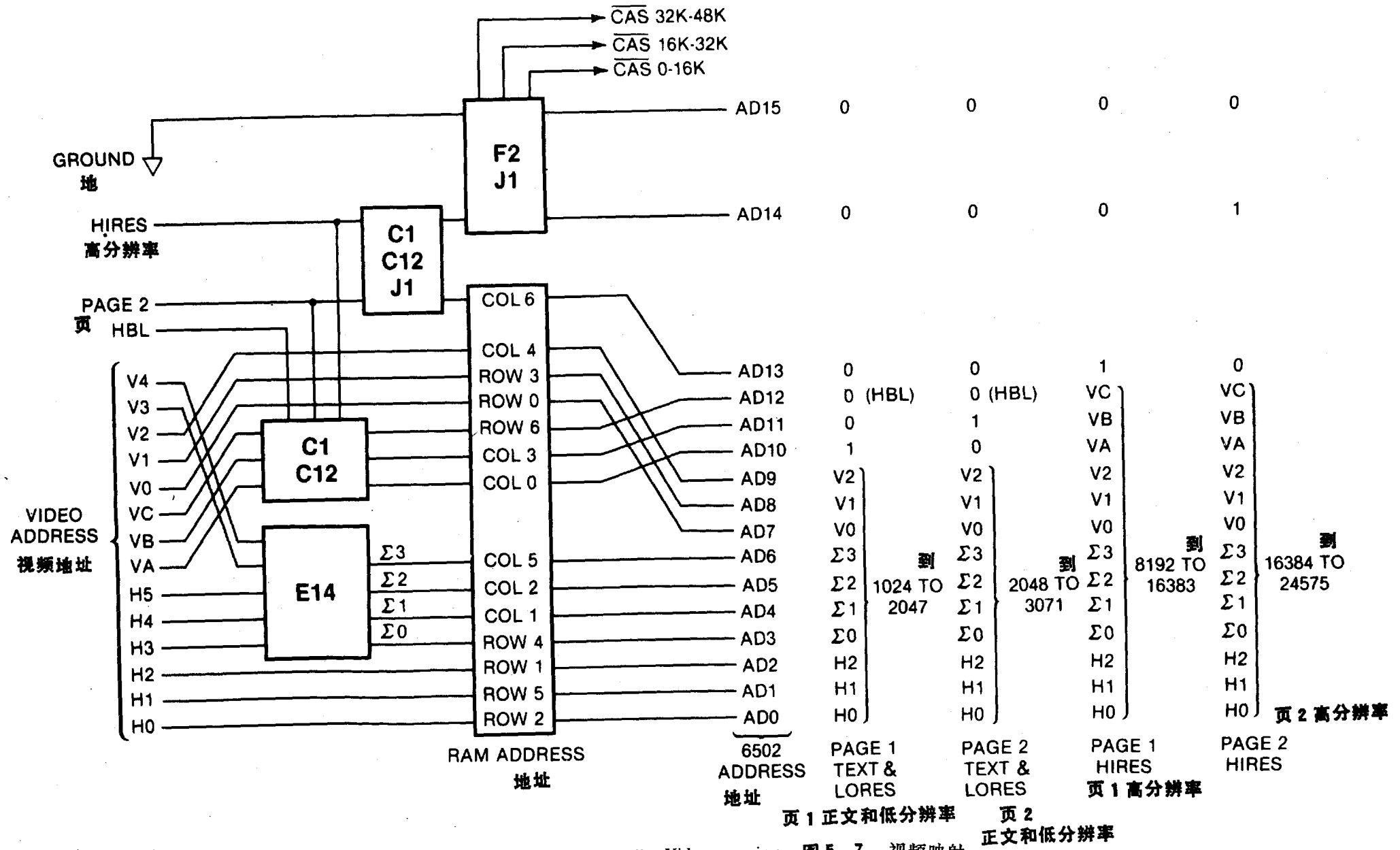



Fig. 5-7. Video mapping. 图 5 - 7 视频映射

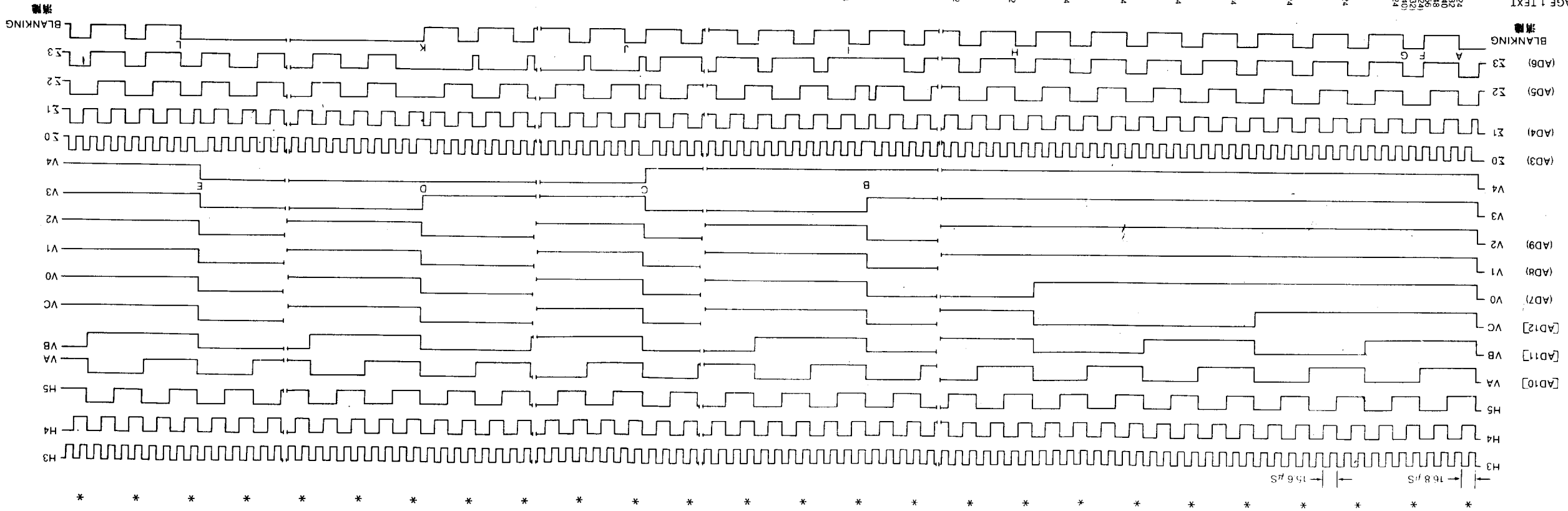



FIG. 5-8. Video address signals. 图 5 - 8 视频地址信号

此为试读，需要完整PDF请访问：www.ertongbook.com

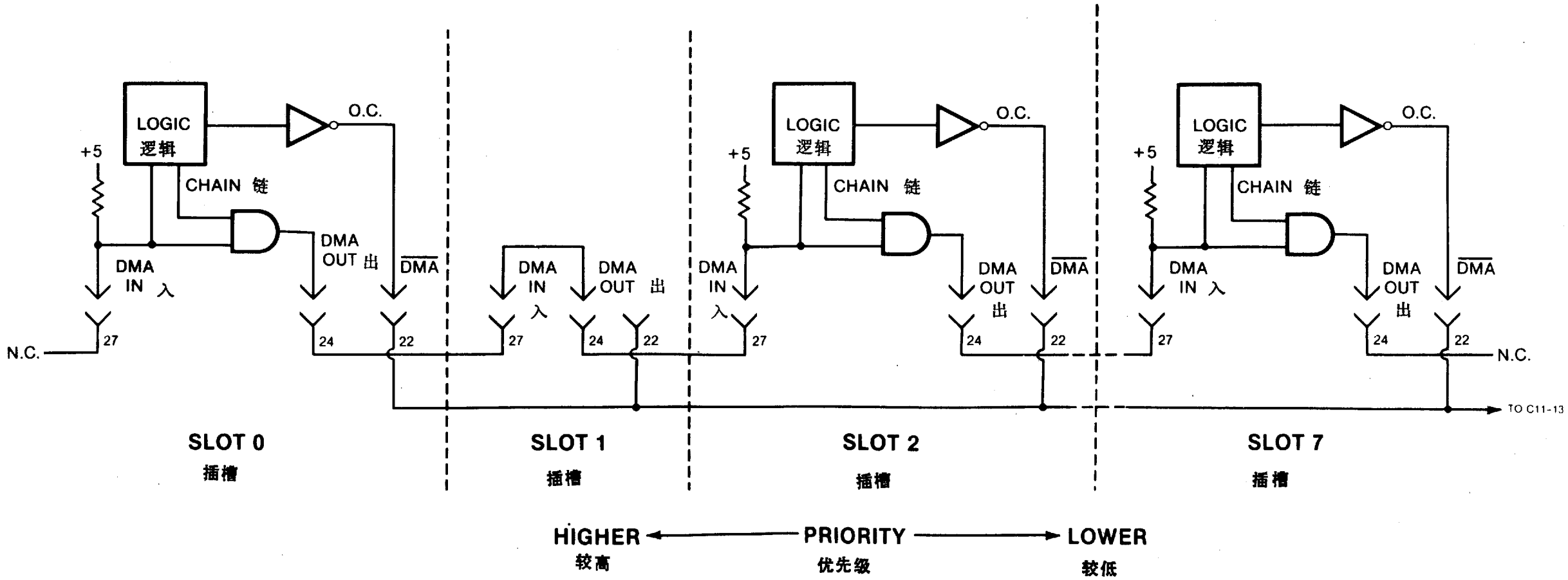



Fig. 6-11. DMA daisy chain. 图 6 -11 DMA 菊形链

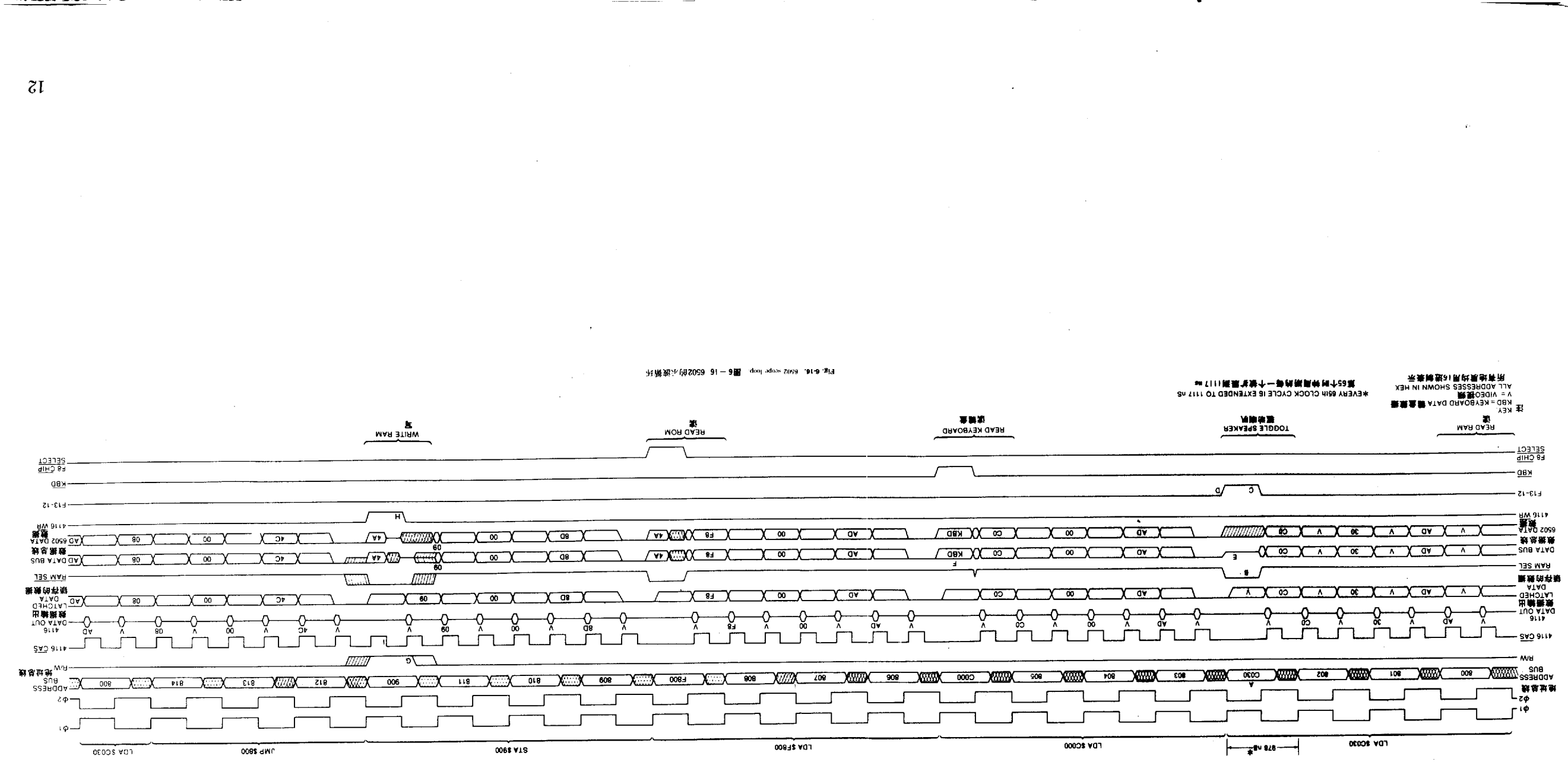



Fig. 6-16. 6502 scope loop 图6－16 6502的示波器环

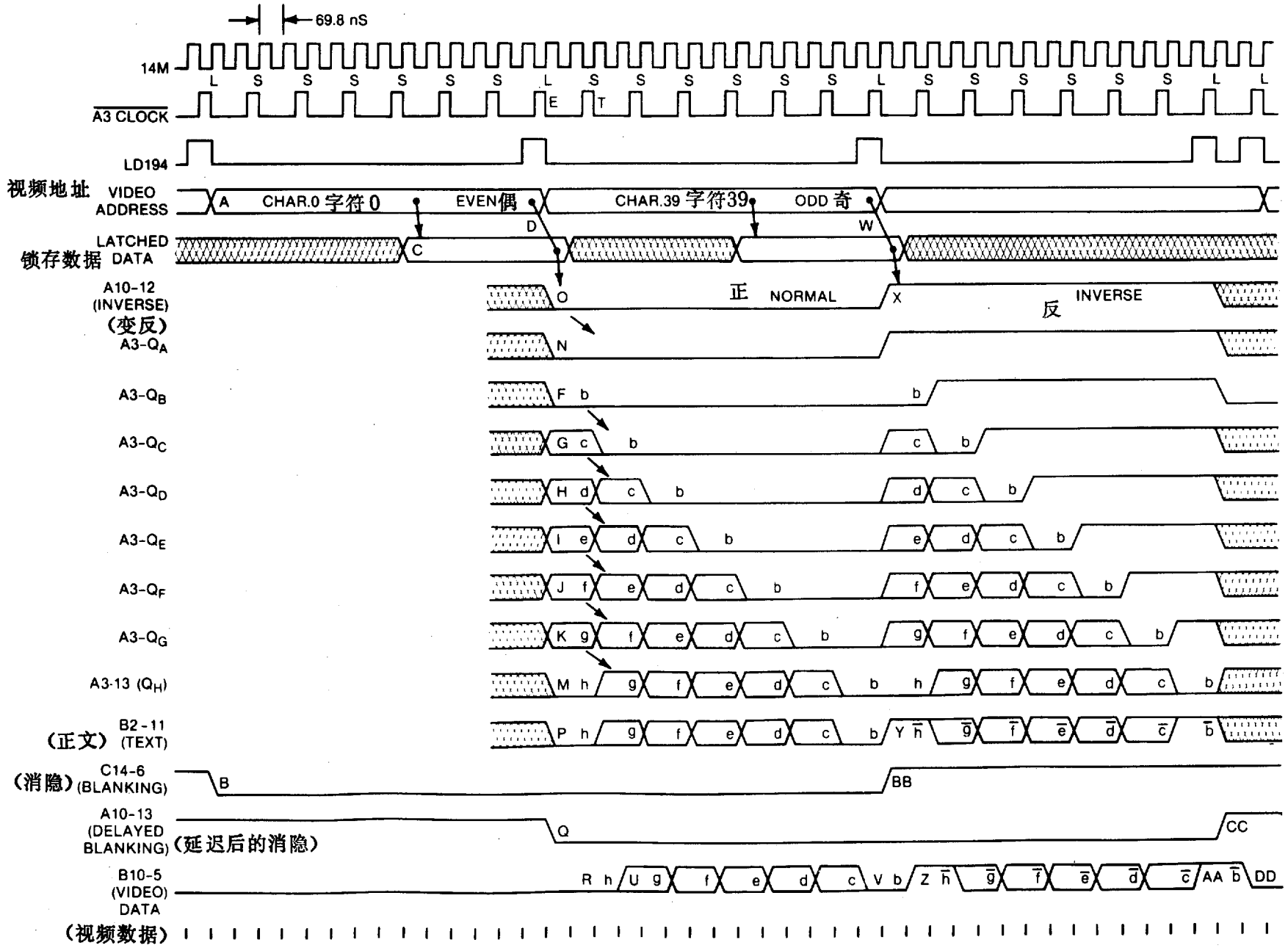



**Fig. 8-26.** Text mode timing diagram. **图 8-26** 正文模式时间关系图

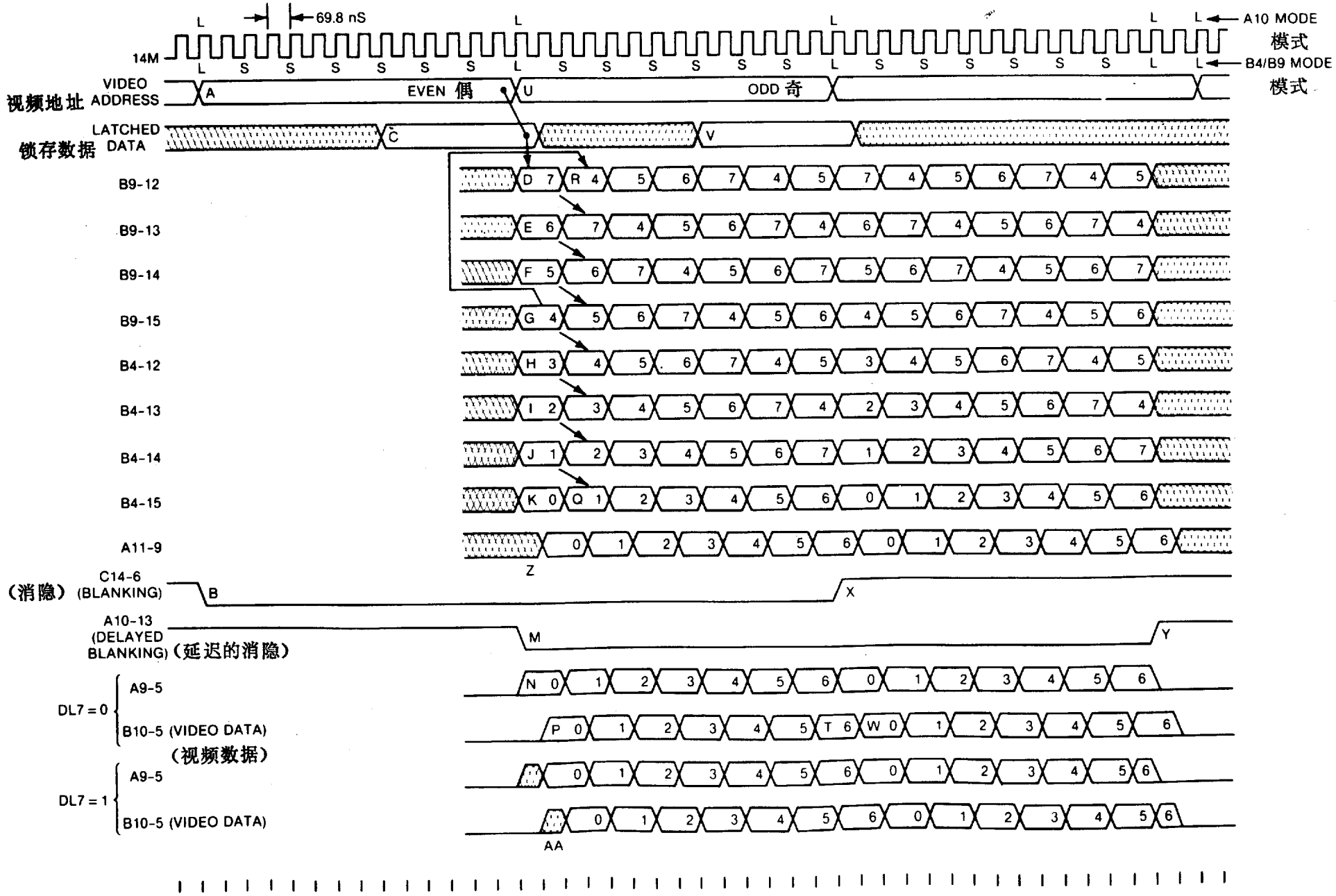



**Fig. 8-28.** HIRES-mode timing diagram. **图 8-28** HIRES 模式时间关系图

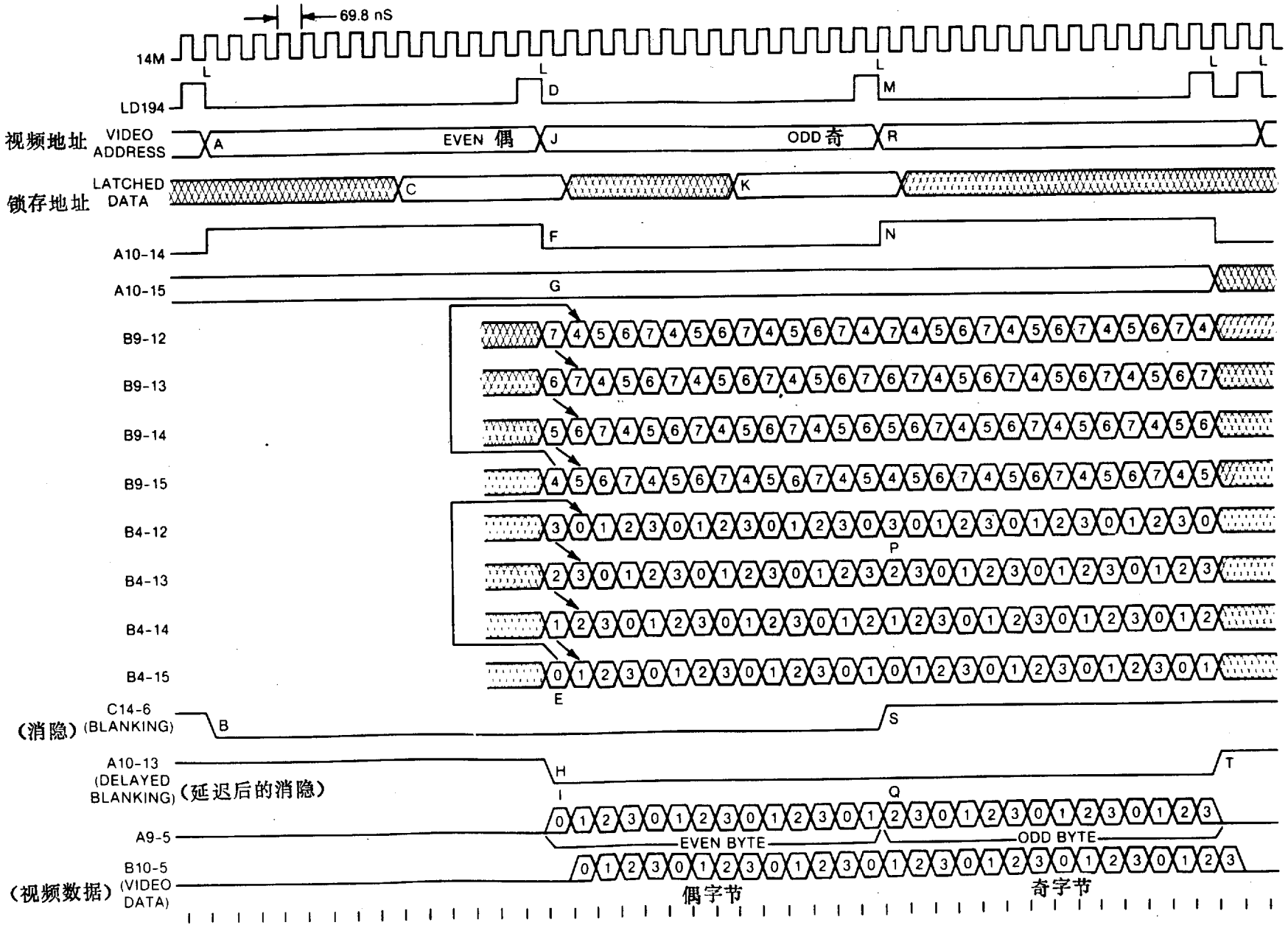



**Fig. 8-31.** LORES-mode timing diagram. **图 8 -31** LORES 模式时间关系图

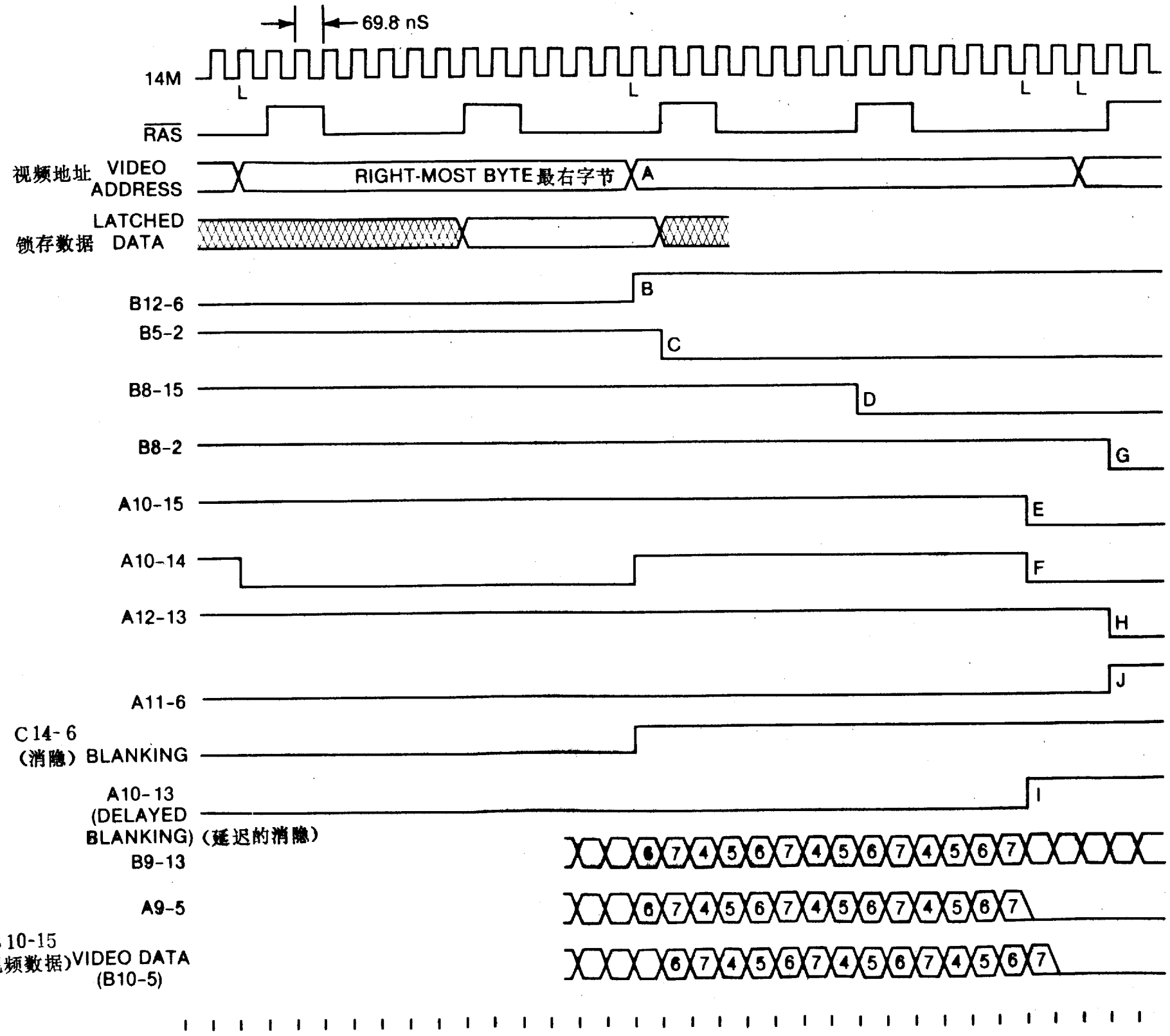



**Fig. 8-34.** Mixed LORES and text. ■ 8-34 LORES 和正文的混合



此为试读，需要完整PDF请访问：www.ertongbook.com