



教育部高等学校电子信息类专业教学指导委员会规划教材  
高等学校电子信息类专业系列教材

信息与通信工程

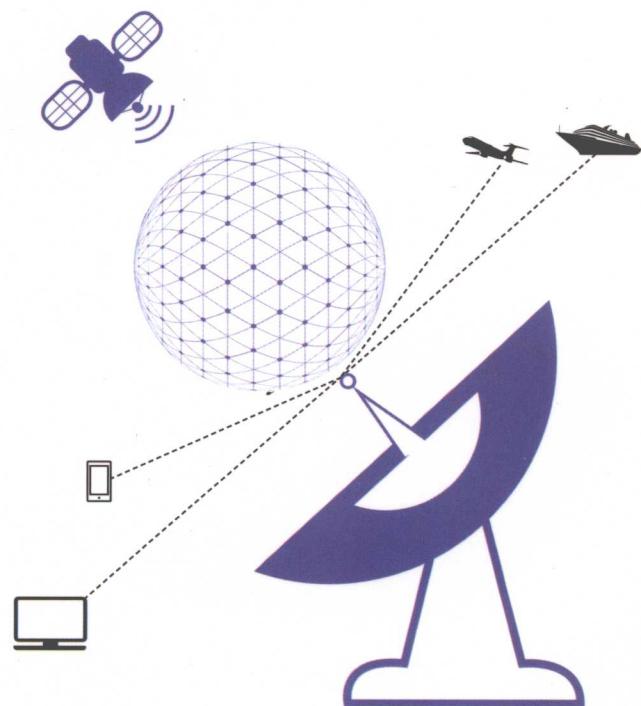
Technical English for Information Science and  
Electronic Engineering (Second Edition)

# 信息科学与电子工程 专业英语

(第2版)

吴雅婷 王朔中 黄素娟 编著

Wu Yating Wang Shuzhong Hang Sujuan



清华大学出版社



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北京

## 内 容 简 介

本书供高等院校信息科学、通信工程、电子技术、计算机应用等专业的本科生和研究生学习专业英语之用。选材兼顾经典题材和新兴技术，在编写中摈弃过分依赖语法、死记硬背的陈旧教学方法，注重培养学生以较高准确性和足够的速度阅读专业资料和文献的能力，兼顾一定的专业英语表达能力，从阅读、翻译、写作等角度提高学生对专业英语的应用能力。

全书共 17 单元，各单元包括课文、词汇、难点注释、课外阅读资料、习题。书后附有关于科技英语阅读、写作、克服中式英语等问题的指南和讨论。

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# Preface

This textbook of technical English is intended for teaching undergraduates and graduate students majoring in information technology, communication engineering, electronic engineering, computer and related subjects.

English as a medium of communication is important in students' future career. The graduates will face various scientific articles, technical documents, product manuals, commercials, and other materials in English. However, having learned English ever since they entered primary school, many university students in their junior and senior years still lack adequate experiences and abilities in using the language as a tool. They are unable to acquire information and knowledge in the fast-developing technological fields, let alone express themselves in English orally or in written form. The problem does not primarily lie in grammar or vocabulary. Indeed, many students have a good mastery of the knowledge about English, but perhaps not the English language itself. They may know almost every rule of the grammar as well as a fairly large quantity of words, even rarely used ones. Some show extraordinary skills in tackling various exams. When coming to practical uses, however, things become quite different. Many students find it difficult to read technical materials at a reasonable speed and catch the message accurately, and don't know how to write in English correctly.

In view of the above, we emphasize actual use of the language, rather than the grammar. Taking into account the limited classroom hours and the practical needs of most students, this course mainly focuses on teaching student to read. The book covers a range of topics including communications, signal and information processing, electronic circuits and systems, microwaves, optical fibers, biomedical engineering, computer science, etc. Each unit consists of a text of 2500~3500 words in two or three parts, a vocabulary, some notes on the text, materials for off-classroom reading, and exercises. The exercises are not designed for grammar review, but rather, should be used as a supplement in improving students' reading ability.

It should be noted that, without a substantial amount of reading practice outside the classroom and continuous efforts after this course, only attending the lectures is far from enough for a student to be able to use technical English proficiently. Therefore, students are strongly encouraged to read as much as possible, not confined to the materials in the textbook.

Writing is not the main objective of the course. Nonetheless, we believe that reading proficiency resulting from intensive practical use and a good habit of careful observation while reading will greatly help enhance writing ability. Some notes on technical English writing are included in the Appendix.

This textbook is a result of many years' teaching practice of the authors and all members of the teaching group. The authors wish to express their sincere thanks to Chen Quanlin, Shi Hai, Zhu Qiuyu, Shi Xuli and Li Yingjie for their contributions and invaluable help over the years.

Without doubt, this book needs further improvements. Therefore any comments or recommendations are sincerely welcome and highly appreciated.

Wang Shuozhong, Huang Sujuan, Wu Yating

October 8, 2017

# 前言

## PREFACE

本教材是为信息科学、通信工程、电子技术、计算机应用等专业的本科生、研究生学习科技英语而编写的。本书选材力求覆盖较广泛的专业方向，注重经典题材和新兴技术，对部分基本原理或新概念提供相关英文辅助资料，以便教师结合课文有选择地用英语讲述一些专业基础知识，或者供学生阅读，使他们在学习科技英语的同时扩大专业知识面。

英语是理工科学生必须掌握的实用工具。然而，不少学生在学了十多年英语以后，仍不能有效地运用英语获取专业知识和科技信息，更不要说用英语进行科技交流了。根据这种情况，结合大学英语教学现状，我们在本书编写中力求改革创新，拒绝应试教学，摈弃从语法到语法、死记硬背的陈旧教学方法，强调大量实践，主张阅读准确性和阅读速度并重，兼顾英语表达能力的提高。

我们认为大学高年级和研究生专业英语教学应以培养和提高英语运用能力为根本目的。学生并不缺少语法知识，而是缺少实践。他们很少甚至没有读过科技英语资料，不掌握丰富的表达形式，缺乏正确的语感。我国学生语法基础普遍较好，但在阅读中往往过分依赖语法分析。他们不了解语法的作用应是内在的和深层的，而不是表面的。依赖语法分析不仅阅读速度上不去，而且即使看懂了句子，读完全文可能还抓不住要点。这种现象相当普遍。实际上，理工科学生学外语并不是为了研究语言，而是要运用语言，因此应以感性认识和反复实践为主，语法知识学习为辅。基于这一认识，我们在课文注释中尽量避免使用语法术语，希望学生在阅读实践中提高阅读能力，最终甩掉语法拐棍。只有这样才能逐步做到顺序阅读而不用回头看，达到理解准确性和阅读速度的统一。

写作不是本教材的重点，但阅读能力的突破以及在阅读中的留心观察，对于写作能力的形成和提高具有关键性的作用。附录中收入了我们在科技英语阅读和写作方面的体会，其中包括一些探索性的研究心得和观点。此外，我们还讨论了普遍存在的中式英语问题，根据大量实例分析了一些典型情况，并就如何克服中式英语提出我们的看法，供读者参考并希望得到专家的指导。

本书是2008年版《信息科学与电子工程专业英语》的第2版，扩大了适用范围，充实了近年来如物联网、大数据、云计算等热点技术及其应用的内容，力求通过范文的阅读和翻译，培养学生以较高准确性和足够的速度阅读专业资料的能力，同时使学

生通过学习科技英语的用词、句型和语言风格，提高专业英语写作和表达的应用能力。

本教材反映了教学小组全体教师多年来在教学中积累的经验，编者特别要感谢陈泉林、石海、朱秋煜、石旭利、李颖洁老师所提供的帮助和支持。

因编者水平所限，书中不当之处在所难免，敬请读者不吝指正。

编者

2017年10月

# Contents

<b>Unit 1</b>	<b>Electronics: Analog and Digital</b>	<b>1</b>
Text	.....	1
Part I: Ideal Operational Amplifiers and Practical Limitations	.....	1
Part II: Data Registers and Counters	.....	3
Part III: Nature of Phase Lock	.....	6
New Words	.....	8
Notes on the Text	.....	9
Technical Tips	.....	12
Supplementary Readings: Bridging the Gap between the Analog and Digital Worlds	.....	13
Exercises	.....	17
<b>Unit 2</b>	<b>Integrated Circuits</b>	<b>21</b>
Text	.....	21
Part I: The Integrated Circuit	.....	21
Part II: Application Specific Integrated Circuit	.....	24
New Words	.....	27
Notes on the Text	.....	28
Technical Tips	.....	31
Supplementary Readings	.....	31
Exercises	.....	34
<b>Unit 3</b>	<b>EM Fields, Antenna and Microwaves</b>	<b>37</b>
Text	.....	37
Part I: Electromagnetic Field	.....	37
Part II: Microstrip Antenna	.....	38
Part III: Microwaves	.....	40
New Words	.....	43
Notes on the Text	.....	44
Technical Tips	.....	46
Supplementary Readings: What Are Microwaves?	.....	46
Exercises	.....	50
<b>Unit 4</b>	<b>Communication and Information Theory</b>	<b>53</b>

Text.....	53
Part I: Telecommunication .....	53
Part II : Data Transmission .....	55
Part III: Information Theory.....	56
New Words.....	59
Notes on the Text .....	60
Technical Tips .....	63
Supplementary Readings .....	63
Exercises.....	66
<b>Unit 5 Multiple Access Techniques.....</b>	<b>70</b>
Text.....	70
Part I: Multiple Access Techniques: FDMA, TDMA and CDMA .....	70
Part II : Orthogonal Frequency Division Multiplexing .....	76
New Words.....	79
Notes on the Text .....	80
Technical Tips .....	82
Supplementary Readings: Wavelength-Division Multiplexing .....	82
Exercises.....	85
<b>Unit 6 Mobile Communications .....</b>	<b>88</b>
Text.....	88
Part I: Mobile Communications .....	88
Part II : Fourth Generation Wireless Networks .....	91
New Words.....	94
Notes on the Text .....	95
Technical Tips .....	97
Supplementary Readings: The Road to 5G .....	98
Exercises.....	102
<b>Unit 7 Optical Communications.....</b>	<b>104</b>
Text.....	104
Part I: Electromagnetic Spectrum.....	104
Part II : Optical Fiber.....	107
New Words.....	111
Notes on the Text .....	112
Technical Tips .....	115
Supplementary Readings: Optical Systems .....	116
Exercises.....	119
<b>Unit 8 Digital Signals and Signal Processing.....</b>	<b>122</b>
Text.....	122
Part I: Digital Signal Processing .....	122

Part II : General Concepts of Digital Signal Processing .....	125
New Words.....	130
Notes on the Text .....	132
Technical Tips .....	134
Supplementary Readings: Designing Digital Filters .....	135
Exercises.....	141
<b>Unit 9 Digital Audio Compression .....</b>	<b>145</b>
Text.....	145
Part I: MPEG Audio Layer 3 .....	145
Part II : Digital Audio Compression Standard AC3 .....	147
New Words.....	151
Notes on the Text .....	152
Technical Tips .....	154
Supplementary Readings: Audio Compression Algorithm Overview .....	155
Exercises.....	159
<b>Unit 10 Digital Image Processing.....</b>	<b>162</b>
Text.....	162
Part I: Two-Dimensional Digital Images .....	162
Part II : Digital Images — Definition and Applications .....	164
Part III: Introduction to Image Processing.....	167
New Words.....	172
Notes on the Text .....	174
Technical Tips .....	180
Supplementary Readings .....	180
Exercises.....	186
<b>Unit 11 Biometrics Technology.....</b>	<b>188</b>
Text.....	188
Part I: Fingerprint Identification .....	188
Part II : Introduction to Speaker Identification.....	190
New Words.....	195
Notes on the Text .....	196
Technical Tips .....	199
Supplementary Readings: Biometrics Overview .....	200
Exercises.....	204
<b>Unit 12 Information Security .....</b>	<b>207</b>
Text.....	207
Part I: Information Security — Introduction and a Brief History .....	207
Part II : Basic Principles of Information Security .....	208
Part III: Intrusion Detection System.....	210

New Words	212
Notes on the Text	214
Technical Tips	217
Supplementary Readings: Hidden Communication	218
Exercises	223
<b>Unit 13 Telemedicine and Biomedical Signal Processing</b>	<b>226</b>
Text	226
Part I: Telemedicine	226
Part II: Computerized Tomographic Imaging	228
New Words	230
Notes on the Text	231
Technical Tips	234
Supplementary Readings: Biomedical Signal Processing	234
Exercises	237
<b>Unit 14 Computers and Networks</b>	<b>240</b>
Text	240
Part I: Evolution of Computers	240
Part II: Local Area Networks	244
New Words	249
Notes on the Text	250
Technical Tips	253
Supplementary Readings	254
Exercises	258
<b>Unit 15 Artificial Intelligence</b>	<b>262</b>
Text	262
Part I: What Is Artificial Intelligence	262
Part II: Approaches of AI	264
New Words	268
Notes on the Text	269
Technical Tips	271
Supplementary Readings: AlphaGo	272
Exercises	275
<b>Unit 16 Big Data and Cloud Computing</b>	<b>278</b>
Text	278
Part I: Big Data	278
Part II: Cloud Computing	282
New Words	286
Notes on the Text	287
Technical Tips	289

Supplementary Readings: Smart City .....	290
Exercises.....	294
<b>Unit 17 Internet of Things (IoT) .....</b>	<b>296</b>
Text.....	296
Part I: Internet of Things: Concept and Key Technologies .....	296
Part II : IoT Applications .....	299
New Words.....	303
Notes on the Text .....	304
Technical Tips.....	306
Supplementary Readings: Wireless Sensor Network.....	307
Exercises.....	310
<b>Appendices.....</b>	<b>312</b>
I. How Should We Read English .....	312
II . Writing Technical English .....	314
III. Avoid Pidgin English.....	329
IV. Title of Scientific Papers .....	337
V . How to Write Abstract.....	339
<b>Bibliography .....</b>	<b>343</b>

## Unit 1



# Electronics: Analog and Digital

Signals in electronics may be of two types, analog or digital. Digital instruments are in general more precise than analog ones and they easily transmit information even over very long distances. However, most electronic designs include a combination of both real-world analog signals and digital signals.

## Text

### Part I: Ideal Operational Amplifiers and Practical Limitations

In order to discuss the ideal parameters of operational amplifiers, we must first define the terms, and then go on to describe what we regard as the ideal values for those terms. At first sight, the specification sheet for an operational amplifier seems to list a large number of values, some in strange units, some interrelated, and often confusing to those unfamiliar with the subject. Without a real appreciation of what each definition means, the designer is doomed to failure. The objective is to be able to design a circuit from the basis of the published data, and know that it will function as predicted when the prototype is constructed.<sup>1</sup> It is all too easy with linear circuits, which appear relatively simple when compared with today's complex logic arrangements, to ignore detailed performance parameters which can drastically reduce the expected performance.<sup>2</sup>

Let us take a very simple but striking example. Consider a requirement for an amplifier having a voltage gain of 10 at 50 kHz driving into a  $10\text{ k}\Omega$  load.<sup>3</sup> A common low-cost, internally frequency-compensated op amp is chosen; it has the required bandwidth at a closed-loop gain of 10, and it would seem to meet the bill.<sup>4</sup> The device is connected, and it is found to have the correct gain. But it will only produce a few volts output swing when the data clearly shows that the output should be capable of driving to within two or three volts of the power supply.<sup>5</sup> The designer has forgotten that the maximum output voltage swing is severely limited by frequency, and that the maximum low-frequency output swing becomes limited at about 10 kHz. This sort of problem occurs regularly for the inexperienced designer. So the moral is clear: always take the necessary time to write down the full

operating requirements before attempting a design. Attention to the detail of the performance specification will always be beneficial. It is suggested the following list of performance details be considered:

- Closed loop gain accuracy, stability with temperature, time and supply voltage.
- Power supply requirements, source and load impedances, power dissipation.
- Input error voltages and bias currents. Input and output resistance, drift with time and temperature.
- Frequency response, phase shift, output swing, transient response, slew rate, frequency stability, capacitive load driving, overload recovery.
- Linearity, distortion and noise.
- Input, output or supply protection required. Input voltage range, common-mode rejection.
- External offset trimming requirement.

Not all of these terms will be relevant, but it is useful to remember that it is better to consider them initially rather than to be forced into retrospective modifications.

#### **All parameters are subject to wide variations**

Never forget this fact. How many times has a circuit been designed using typical values, only to find that the circuit does not work because the device used is not typical?<sup>6</sup> The above statement thus poses a tricky question: when should typical values and when should worst-case values be used in the design? This is where the judgment of the experienced designer must be brought to bear. Clearly, if certain performance requirements are mandatory, then worst-case values must be used. In many cases, however, the desirability of a certain defined performance will be a compromise between ease of implementation, degree of importance, and economic considerations.<sup>7</sup>

#### **Do not over-specify or over-design**

In the end, we are all controlled by cost. Simplicity is of the essence since the low parts count implementation is invariably cheaper and more reliable.<sup>8</sup>

As an example of this judgment about worst-case design, consider a low-gain DC transducer amplifier required to amplify 10 mV from a voltage source to produce an output of 1 V with an accuracy of  $\pm 1\%$  over a temperature range of 0~70°C.<sup>9</sup> Notice that the specification calls for an accuracy of  $\pm 1\%$ . This implies that the output should be 1 V  $\pm 10$  mV from 0~70°C. The first step is, of course, to consider our list above, and decide which of the many parameters are relevant. Two of the most important to this specification are offset voltage drift and gain stability with temperature. We will assume that all initial errors are negligible (rarely the case in practice). The experienced designer would know that most op amps have a very large open-loop gain, usually very much greater than 10000. A closed-loop gain change of  $\pm 1\%$  implies that the loop gain (as explained later) should change by less than  $\pm 100\%$  for a closed-loop gain of 100.<sup>10</sup> This is clearly so easily fulfilled that the designer knows immediately that he can use typical open-loop gain values in his

calculations. However, offset voltage drift is another matter. Many op amp specifications include only typical values for offset voltage drift; this may well be in the order of  $5 \mu\text{V}/^\circ\text{C}$ , with an unquoted maximum for any device of  $30 \mu\text{V}/^\circ\text{C}$ .<sup>11</sup> If by chance we use a device which has this worst-case drift, then the amplifier error could be  $30 \times 70 = 2100 \mu\text{V} = 2.1 \text{ mV}$  over temperature, which is a significant proportion of our total allowable error from all sources.

## Part II : Data Registers and Counters

### Data register

The simplest type of register is a data register, which is used for the temporary storage of a “word” of data. In its simplest form, it consists of a set of  $N$  D flip-flops, all sharing a common clock. All of the digits in the  $N$  bit data word are connected to the data register by an  $N$ -line “data bus”. Figure 1.1 shows a 4 bit data register, implemented with four D flip-flops. The data register is said to be a synchronous device, because all the flip-flops change state at the same time.

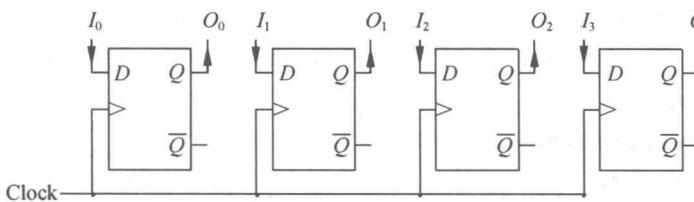


Figure 1.1 Four-bit D register

### Shift registers

Another common form of register used in computers and in many other types of logic circuits is a shift register. It is simply a set of flip-flops (usually D latches or RS flip-flops) connected together so that the output of one becomes the input of the next, and so on in series.<sup>1</sup> It is called a shift register because the data is shifted through the register by one bit position on each clock pulse.<sup>2</sup> Figure 1.2 shows a 4 bit shift register, implemented with D flip-flops.

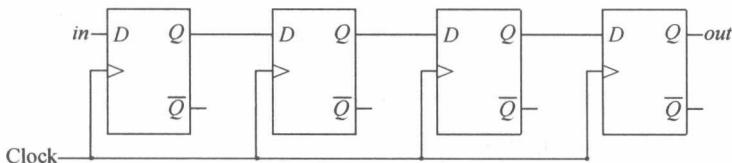


Figure 1.2 Four-bit serial-in serial-out shift register

On the leading edge of the first clock pulse, the signal on the DATA input is latched in the first flip-flop. On the leading edge of the next clock pulse, the contents of the first flip-flop is stored in the second flip-flop, and the signal which is present at the DATA input is stored in the first flip-flop, etc.<sup>3</sup> Because the data is entered one bit at a time, this called a

serial-in shift register. Since there is only one output, and data leaves the shift register one bit at a time, then it is also a serial out shift register. (Shift registers are named by their method of input and output; either serial or parallel.) Parallel input can be provided through the use of the preset and clear inputs to the flip-flop. The parallel loading of the flip-flop can be synchronous (i.e., occurs with the clock pulse) or asynchronous (independent of the clock pulse) depending on the design of the shift register.<sup>4</sup> Parallel output can be obtained from the outputs of each flip-flop as shown in Figure 1.3.

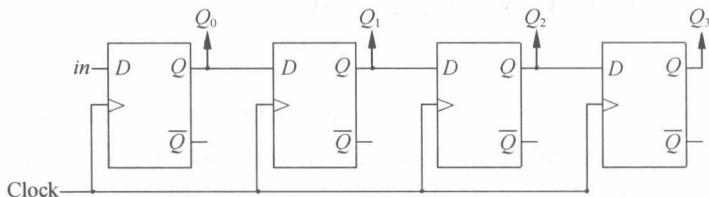


Figure 1.3 Four-bit serial-in parallel-out shift register

Communication between a computer and a peripheral device is usually done serially, while computation in the computer itself is usually performed with parallel logic circuitry. A shift register can be used to convert information from serial form to parallel form, and vice versa. Many different kinds of shift registers are available, depending upon the degree of sophistication required.

### Counters — weighted coding of binary numbers

In a sense, a shift register can be considered a counter based on the unary number system. Unfortunately, a unary counter would require a flip-flop for each number in the counting range. A binary weighted counter, however, requires only flip-flops to count to  $N$ . A simple binary weighted counter can be made using  $T$  flip-flops. The flip-flops are attached to each other in a way so that the output of one acts as the clock for the next, and so on. In this case, the position of the flip-flop in the chain determines its weight; i.e., for a binary counter, the “power of two” it corresponds to.<sup>5</sup> A 3-bit (modulo 8) binary counter could be configured with  $T$  flip-flops as shown in Figure 1.4. A timing diagram corresponding to this circuit is shown in Figure 1.5.

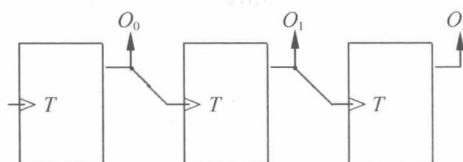


Figure 1.4 Three-bit binary counter

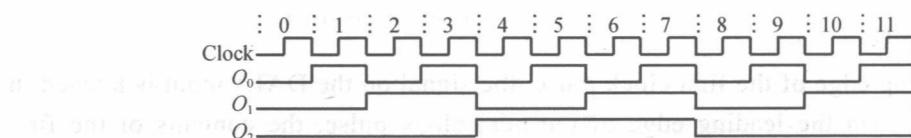


Figure 1.5 Three-bit counter timing diagram

Note that a set of lights attached to  $O_0$ ,  $O_1$ ,  $O_2$  would display the numbers of full clock pulses which had been completed, in binary (modulo 8), from the first pulse.<sup>6</sup> As many T flip-flops as required could be combined to make a counter with a large number of digits.

Note that in this counter, each flip-flop changes state on the falling edge of the pulse from the previous flip-flop. Therefore there will be a slight time delay, due to the propagation delay of the flip-flops between the time one flip-flop changes state and the time the next one changes state, i.e., the change of state ripples through the counter, and these counters are therefore called ripple counters.<sup>7</sup> As in the case of a ripple carry adder, the propagation delay can become significant for large counters.

It is possible to make, or buy in a single chip, counters which will count up, count down, and which can be preset to any desired number. Counters can also be constructed which count in BCD and base 12 or any other number base.

A count down counter can be made by connecting the  $\bar{Q}$  output to the clock input in the previous counter. By the use of preset and clear inputs, and by gating the output of each T flip flop with another logic level using AND gates (say logic 0 for counting down, logic 1 for counting up), then a presettable up-down binary counter can be constructed.<sup>8</sup> Figure 1.6 shows an up-down counter, without preset or clear.

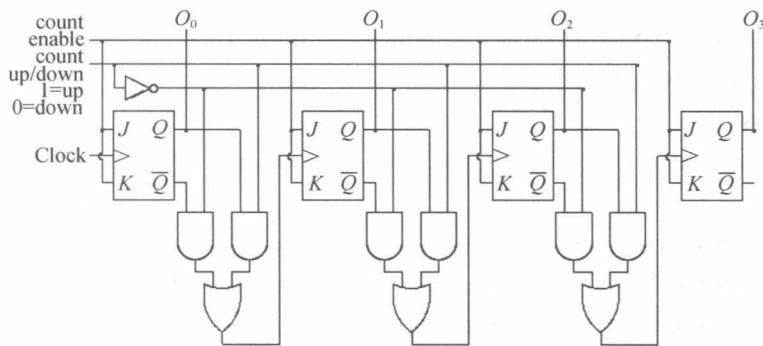


Figure 1.6 Programmable up-down counter\*

### Synchronous counters

The counters shown previously have been “asynchronous counters”; so called because the flip-flops do not all change state at the same time, but change as a result of a previous output. The output of one flip-flop is the input to the next; the state changes consequently “ripple through” the flip-flops, requiring a time proportional to the length of the counter.<sup>9</sup> It is possible to design synchronous counters, using JK flip-flops, where all flip flops change state at the same time; i.e., the clock pulse is presented to each JK flip-flop at the same time. This can be easily done by noting that, for a binary counter, any given digit changes its value (from 1 to 0 or from 0 to 1) whenever all the previous digits have a value of 1.<sup>10</sup>

\* 本书所使用英文资料中的电路未改为国标符号。