ENGLISH FOR ELECTRONIC SCIENCE AND TECHNOLOGY

电子科学与技术专业英语

闫小兵　师建英　赵　瑞　马　蕾　编著

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内容简介

本书根据作者在电子科学与技术专业英语教学过程中长期积累的经验总结而成. 全书分为四个章节：半导体器件、集成电路、电路，以及学术写作. 第 1 章介绍了 pn 结、双极型器件和太阳能电池的特性；第 2 章介绍了集成电路的发展历程、FPGA 与 ASIC、集成电路的分类以及集成电路设计工具；第 3 章介绍了二极管和整流器电路、双极晶体管的历史和典型应用电路、信号操作处理以及直流稳压电源设计；第 4 章介绍了科技英语文章各部分的写作方法、齐头式写作格式以及一些易错点与注意事项. 全书涵盖了微电子技术领域的基础知识，同时又介绍了该领域的一些较新的发展状况.

本书可作为电子科学与技术专业的高年级本科生的专业英语教材，也可供相关专业研究生以及从事相关专业领域的工程技术人员使用.

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前　言

在信息全球化的21世纪，英语已经成为国际交流的重要工具. 在高等院校的理工类专业教学中，专业英语课程已然占据了极为重要的一部分，它的教学目的是衔接英语这门语言与具体理工类专业的基础知识与运用. 通过此类课程的学习，学生可以掌握科技英语技能，熟练阅读和翻译文献，撰写英文科技文章，进而了解国际上本专业的科技发展新动态. 本书的目的是满足电子科学与技术专业的本科生与研究生专业英语教学的需要.

本书主要分为四个章节：第1章是半导体器件方面的知识，主要包括：pn结、双极型器件和太阳能电池的特性. 第2章是集成电路部分，主要包括：集成电路的发展历程、FPGA与ASIC的介绍、集成电路的分类以及集成电路的设计工具. 第3章是电路部分的知识，主要包括二极管和整流器电路、双极晶体管的历史和典型应用电路、信号操作处理以及直流稳压电源设计. 第4章是写作指导部分，主要介绍科技英语文章各部分的写作方法、齐头式写作格式以及一些易错点与注意事项.

为了满足上下文的连贯性以及篇幅的限制，书中的内容做了部分删减. 为了有利于学生理解并巩固课上学习的知识，每章内容的最后都附有主要的专业词汇注释以及章节词汇与句子的翻译练习题.

本书可由教师根据自身学校的课时与专业需要选择合适的内容教学. 其他非本专业的读者也可以阅读，可提高阅读、翻译与创作科技英文文章的能力，放宽眼界.

作者在编写本书的过程中得到了多位电子科学与技术专业老师与学生的帮助，在此表示真诚的感谢. 由于编者的水平有限，疏漏之处在所难免，期待各界读者批评指正.

闫小兵

2017年5月

Preface

In the 21st century of information globalization, English has become an important part of international communication. In the teaching of science and engineering in colleges and universities, the professional English course with its teaching purpose is to link the basic knowledge and application of the language and specific science and engineering majors, has already occupied an extremely important part. Through the study of such courses, students can master technical English skills, be proficient in reading and translating documents, and write English scientific and technical articles to understand the new developments in the science and technology of the international profession. The purpose of this book is to meet the needs of advanced undergraduate and postgraduate professional English teaching in electronic science and technology.

This book is divided into four chapters: Chapter 1 is the knowledge of semiconductor devices, including the pn junction, bipolar devices and solar cell characteristics. Chapter 2 is an integrated circuit part, which mainly covers the development of integrated circuits, the introduction of FPGAs and ASICs, the classification of integrated circuits, and the design tools of integrated circuits. Chapter 3 is part of the circuit, including diode and rectifier circuits, the history of dual-board transistors and typical application circuits, signal processing, and DC regulated power supply design. Chapter 4 is the writing guidance section, which mainly introduces the writing methods of each part of the scientific English article, the head-to-head writing format and some easy-to-follow points and precautions.

In order to meet the consistency of the context and the limitations of the space, the contents of the book were partially cut. Each chapter is accompanied by major professional vocabulary notes and translation exercises for chapter vocabulary and sentences, to help students understand and consolidate the knowledge of class learning.

The teaching content of this book can be selected by the teacher according to the class time and professional needs of their own school. The readers who are not in the professional might also read it, which could improve the ability of reading, translating and creating English articles in science and technology, and broaden the horizon.

In the process of writing this book, the author has received the help of many teachers and students of electronic science and technology profession. I would like to express my sincere gratitude. Due to the limited level of editors, there are inevitable omissions in the book, and readers from all walks of life are expected to criticize and correct.

Xiaobing Yan
2017.05

Contents

Preface

Chapter 1 Semiconductor Device

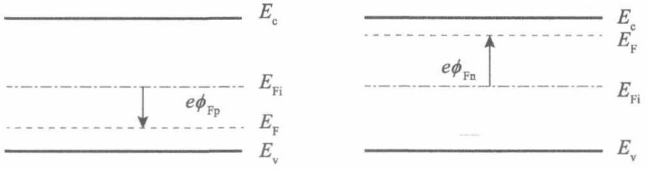
1.1 pn Junction

The structure formed by p-type semiconductor and n-type semiconductor metallurgical contact is called pn junction. pn junction is the basic unit in almost all semiconductor devices. Actually pn junction itself is a device—rectifier, in addition to those devices that use Schottky junction. To master the physical mechanism of pn junction is the basis for learning the physics of other semiconductor devices.

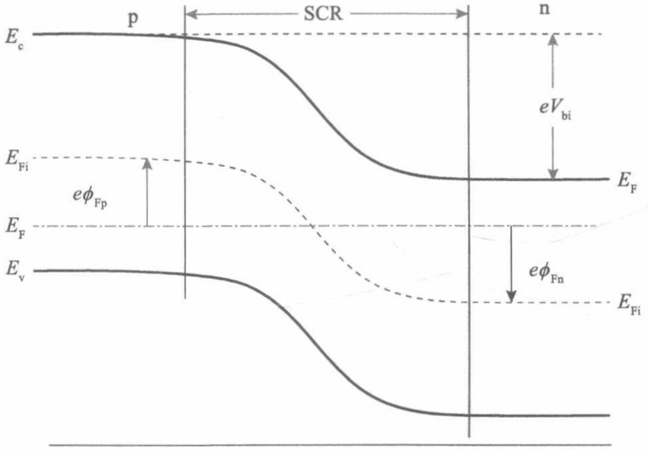
1.1.1 pn Junction Space Charge Region and Contact Potential Difference

When the semiconductor materials of n-type do not contact with that of p-type, the Fermi level of the n-type materials is near the bottom of the conduction band and the Fermi level is near the top of the valence band in p-type materials, as shown in Figure 1-1(a). When the p-type materials are in contact with the n-type materials at the atomic level, and the whole system is in a state of thermal equilibrium, the Fermi level of the whole system must be equal everywhere. Otherwise, according to the modified Ohm's law, the current will flow through the system.

When the n-type and p-type semiconductor materials metallurgically contact each other, majority carriers (holes) in p-type materials diffuse to n-type side. At the same time, majority carriers (electrons) in n-type materials diffuse to p-type side. So, immovable donor ions and acceptor ions will be formed on both sides of the interface, which are described as space charges. An electric field is formed between the positive and negative space charges, which is called the built-in electric field. The built-in electric field causes the electrons and holes drift in the opposite direction of the carrier diffusion. As the diffusion goes on, the drift effect is also gradually enhanced. When the drift and diffusion effects reach the equilibrium, the movement of the carriers achieves dynamic balance so that the net current flowing through the region is zero. At this time, a stable region composed of space charges is formed at the interface between n-type and p-type semiconductor materials, which is described as space charge region (SCR), as shown in Figure 1-1(b).



(a) p-type and n-type semiconductors



(b) pn junction

Figure 1-1 Energy band schematic diagram of p-type and n-type semiconductors and pn junction

A built-in electric field is formed in the pn junction space charge region at the equilibrium state. The electric field forms a potential difference between the n side and the p side, and the height of the built-in potential is

$$V_{bi} = \left|\phi_{Fn}\right| + \left|\phi_{Fp}\right| \tag{1-1}$$

The potential difference causes the formation of carrier diffusion barrier, so the space charge region is also called barrier region.

For pn junction that is in a state of equilibrium,

$$n_{n0} = N_D = n_i \exp\left(\frac{E_F - E_{Fi}}{kT}\right) \tag{1-2}$$

$$p_{p0} = N_A = n_i \exp\left(\frac{E_{Fi} - E_F}{kT}\right) \tag{1-3}$$

where N_D and N_A represent the effective doping concentration of n region and p region, respectively. From Figure 1-1(b), we have

$$e\phi_{Fn} = E_{Fi} - E_F = -kT \ln\left(\frac{N_D}{n_i}\right) \tag{1-4}$$

$$e\phi_{Fp} = E_{Fi} - E_F = kT \ln\left(\frac{N_A}{n_i}\right) \tag{1-5}$$

So

$$V_{bi} = |\phi_{Fn}| + |\phi_{Fp}| = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right) = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right) \tag{1-6}$$

Contact potential difference is related to the impurity concentration, the intrinsic carrier concentration and thermal voltage.

1.1.2 Electric Field and Potential in the Depletion Layer

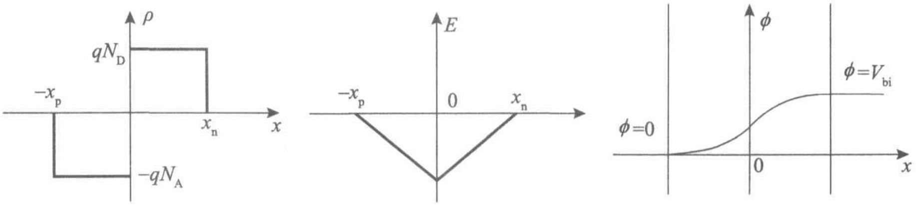
The built-in field is generated by the space charges in the space charge region. The relationship between the electric field intensity and the charge density is determined by the Poisson equation

$$\frac{d^2\phi(x)}{dx^2} = \frac{-\rho(x)}{\varepsilon_s} = -\frac{dE(x)}{dx} \tag{1-7}$$

where ϕ is the potential, E is the electric field strength, ρ is the charge density, and ε_s is the permittivity. According to the depletion approximation theory, from Figure 1-2(c), the charge density of the p side and the n side is

$$\rho(x) = -qN_A, \quad -x_p < x < 0 \tag{1-8a}$$

$$\rho(x) = qN_D, \quad 0 < x < x_n \tag{1-8b}$$



(a) Space charge profile　　(b) Electric field　　(c) Electric potential

Figure 1-2　Space charge profile, electric field and electric potential

The electric field of the p side can be obtained by integrating the $\rho(x)$ to yield

$$E=-\int\frac{qN_A}{\varepsilon_s}\mathrm{d}x=\frac{-qN_A}{\varepsilon_s}x+C_1=\frac{-qN_A}{\varepsilon_s}\left(x+x_p\right),\quad -x_p<x<0 \tag{1-9a}$$

$$E=\int\frac{qN_D}{\varepsilon_s}\mathrm{d}x=\frac{qN_D}{\varepsilon_s}x+C_2=\frac{-qN_D}{\varepsilon_s}\left(x_n-x\right),\quad 0<x<x_n \tag{1-9b}$$

where C_1 and C_2 are integration constants and are determined by the boundary condition $E=0$ at $x=x_p$ and $x=x_n$, respectively. The field must be continuous at the interface ($x=0$) between the n side and the p side, i.e.

$$E=\frac{-qN_Ax_p}{\varepsilon_s}=\frac{-qN_Dx_n}{\varepsilon_s} \tag{1-10}$$

The following result can be derived from Eq. (1-10)

$$N_Ax_p=N_Dx_n \tag{1-11}$$

Eq. (1-11) implies that the overall space charge region is electrically neutral and that the number of the positive space charge is equal to the number of negative space charge. The following expression can be derived from Eq. (1-11).

$$\frac{x_p}{x_n}=\frac{N_D}{N_A} \tag{1-12}$$

where x_n and x_p are the widths of the n-type depletion layers and the p-type depletion layers respectively. They are inversely proportional to the dopant concentration of the corresponding side; the more heavily doped side holds a smaller portion of the depletion layer.

According to the relationship between the electric field and the electric potential, integrating Eq. (1-9a) with making the voltage zero at $x = x_p$ yields as the reference point for $V = 0$ yields

$$\begin{aligned} \phi(x) &= -\int E(x)\,\mathrm{d}x = \int \frac{qN_A}{\varepsilon_s}(x + x_p)\,\mathrm{d}x \\ \Rightarrow \phi(x) &= \frac{qN_A}{2\varepsilon_s}(x + x_p)^2 \quad (-x_p \leqslant x \leqslant 0) \end{aligned} \tag{1-13}$$

Similarly, on the n side, we integrate Eq. (1-9b) once more to obtain

$$\begin{aligned} \phi(x) &= -\int E(x)\,\mathrm{d}x = \int \frac{qN_D}{\varepsilon_s}(x_n - x)\,\mathrm{d}x \\ \Rightarrow \phi(x) &= \frac{qN_D}{\varepsilon_s}\left(x_n x - \frac{x^2}{2}\right) + \frac{qN_D}{2\varepsilon_s}x_n^2 \quad (0 \leqslant x \leqslant x_n) \end{aligned} \tag{1-14}$$

So, we can obtain

$$V_{bi} = |\phi(x = x_n)| = \frac{q}{2\varepsilon_s}\left(N_D x_n^2 + N_A x_p^2\right) \tag{1-15}$$

1.1.3 Space Charge Region Width

Using Eq. (1-11) together with Eq. (1-15), one obtains

$$x_n = \left\{\frac{2\varepsilon_s V_{bi}}{q}\left[\frac{N_A}{N_D}\right]\left[\frac{1}{N_A + N_D}\right]\right\}^{1/2} \tag{1-16a}$$

$$x_p = \left\{\frac{2\varepsilon_s V_{bi}}{q}\left[\frac{N_D}{N_A}\right]\left[\frac{1}{N_A + N_D}\right]\right\}^{1/2} \tag{1-16b}$$

Then using Eq. (1-16), we can obtain the width of the space charge region as

$$W = x_n + x_p = \left\{ \frac{2\varepsilon_s V_{bi}}{q} \left[\frac{N_A + N_D}{N_A N_D} \right] \right\}^{1/2} \tag{1-17}$$

if $N_A \gg N_D$, as in a p^+n junction,

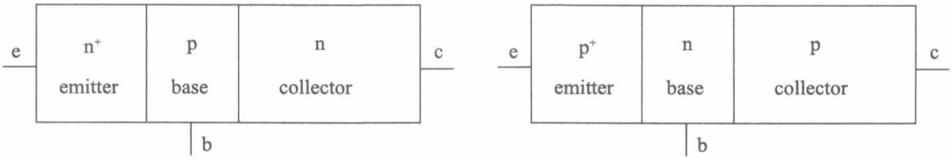
$$W \approx x_n = \left\{ \frac{2\varepsilon_s V_{bi}}{qN_D} \right\}^{1/2} \tag{1-18a}$$

if $N_A \ll N_D$, as in a pn^+ junction,

$$W \approx x_p = \left\{ \frac{2\varepsilon_s V_{bi}}{qN_A} \right\}^{1/2} \tag{1-18b}$$

1.2 Bipolar Junction Transistor

At the end of 1947, Shockley, Bardeen and Brattain invented the point contact transistor at Bell Telephone Laboratories, New Jersey, USA, which was the first solid state device in the world. The invention of the transistor has opened a new era of solid state electronics. It can be said that the invention of the transistor was one of the greatest inventions of the 20th century. In 1951, the alloy junction transistor was made of germanium displaced the point contact transistor, existing for about 20 years, which had played a significant role in the practical application of solid electronic devices. In the 1970s, with the rapid development of silicon planar technology, the planar transistor fabricated by planar technology replaced the alloy junction transistor. Planar transistor includes two types, i.e. npn and pnp (Figure 1-3). In npn and pnp transistors, electrons and holes are both involved in the current transmission, so they are called bipolar junction transistor (BJT).



(a) npn BJT　　(b) pnp BJT

Figure 1-3　Schematic diagram of npn BJT and pnp BJT

1.2.1 Basic Structure of BJT

According to the uses, a wide variety of transistors can be divided into low frequency and high frequency transistors, low power and high power transistors, low noise transistors and high reverse bias voltage transistors and so on. According to the manufacturing process, transistors also can be divided into alloy transistor, diffusion transistor and ion injection transistor, etc.

The basic structures of various transistors are the same: p-type (or n-type) semiconductor thin layer is sandwiched between two n-type (or p-type) semiconductor layers. One of the two sides is heavily doped while the other side is lightly doped. So the transistor has two kinds of structures, i.e. npn and pnp. What's more, the thickness of the interlayer must be much smaller than the diffusion length of minority carriers.

Inside the transistor, transport process of carriers in the base region decides many physical properties, such as current gain, frequency characteristic and power characteristic. After determining geometric parameters (such as base width, emitter junction and collector junction area), the impurity distribution in the base region becomes the key factor affecting the carrier transport process. Although there are many types of transistors, for the sake of convenience, the transistor is usually divided into uniform base transistor and graded base transistor according to the base impurity distribution as one analyzes the carrier transport process in theory.

The base impurity is evenly distributed in uniform base transistors, such as the above mentioned alloy transistor. In this type of transistors, the carrier transport in the base mainly depends on the diffusion mechanism, so it is called diffusion transistor.

The impurity distribution profile is graded in graded base transistor, such as diffusion transistor. A built-in electric field caused by graded distribution of impurities is formed in the base. Due to the existence of built-in electric field, carriers not only carry out the diffusion movement, but also carry out the drift motion. The drift motion is dominant. Therefore, the graded base transistor is also called drift transistor.

1.2.2 Energy Band and Carrier Distribution of BJT

1.2.2.1 Equilibrium BJT

The energy band and carrier distribution of the uniform base transistor without applied voltage (i.e., the equilibrium state) is shown in Figure 1-4. The emitter, base and collector are evenly distributed. The doping concentration of the emitter is the highest, the doping concentration of the base is lower than that of emitter, and that of the collector is the lowest. U_{De} and U_{Dc} denote the contact potential difference of the emitter and collector junction. At the equilibrium state, the transistor has a uniform Fermi level.

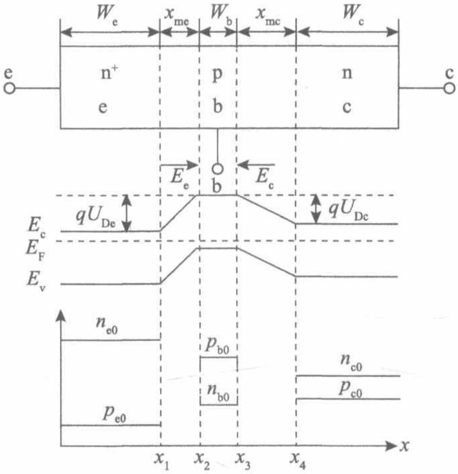


Figure 1-4 Schematic diagram of energy band and carrier distribution in an equilibrium transistor

1.2.2.2 Non-equilibrium BJT

When the transistor is operating under the amplification configuration, the emitter junction is forward biased (represented by U_e) and the collector junction is applied to reverse bias (denoted by U_c). At this time, the transistor emitter and collector junction are in the non-equilibrium condition. Therefore, The Fermi energy level is not consistent throughout the system. The schematic diagram of energy band is shown in Figure 1-5 (b).

Under the amplification conditions, the distribution of carriers in BJT is shown in Figure 1-5(c). A forward bias of U_e reduces the barrier height from qU_{De} to $q(U_{De}-U_e)$. This decreases the drift field and breaks the balance between diffusion and drift that exists at zero bias. Therefore, electrons can diffuse from the emitter (the n side) into the base (the p side). This process is called minority carrier injection. Electrons (minority) accumulate at the base boundary and diffuse into the base region. Simultaneously, the