

国外计算机科 学教材系列

# 数字逻辑与计算机 硬件设计基础 (第二版)

Logic and Computer Design Fundamentals  
Second Edition Updated

英文原版

[美] M. Morris Mano 著  
Charles R. Kime



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## 内 容 简 介

本书是根据美国重点大学新版计算机教学计划而编写的教材,全书共分为数字逻辑设计、计算机硬件设计和计算机设计三个部分,主要包括信息的二进制表示及布尔逻辑、组合电路的分析和设计基础、VHDL和Verilog语言、时序电路的概念和设计、结构化时序电路设计、RAM和可编程逻辑设计、数据通路和控制单元的设计、寄存器传输操作的时序设计、指令集结构、数据传输总线设计和存储系统设计等。

与传统的数字逻辑教材相比,本书内容广泛,更加面向硬件设计。它在介绍数字逻辑的基础上,直接介绍了硬件设计和计算机设计的知识,其设计内容反映了当今最新技术的发展趋势。此外,书中有大量的练习题,以帮助读者掌握和巩固所学知识。

本书可作为国内计算机专业数字逻辑和计算机组织结构课程的教材和辅助教科书,也可作为计算机硬件爱好者的参考书。

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电子工业出版社秉承多年来引进国外优秀图书的经验,翻译出版了“国外计算机科学教材系列”丛书,这套教材覆盖学科范围广、领域宽、层次多,既有本科专业课程教材,也有研究生课程教材,以适应不同院系、不同专业、不同层次的师生对教材的需求,广大师生可自由选择 and 自由组合使用。这些教材涉及的学科方向包括网络与通信、操作系统、计算机组织与结构、算法与数据结构、数据库与信息处理、编程语言、图形图像与多媒体、软件工程等。同时,我们也适当引进了一些优秀英文原版教材,本着翻译版本和英文原版并重的原则,对重点图书既提供英文原版又提供相应的翻译版本。

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此外,我们还将与国外著名出版公司合作,提供一些教材的教学支持资料,希望能为授课老师提供帮助。今后,我们将继续加强与各高校教师的密切联系,为广大师生引进更多的国外优秀教材和参考书,为我国计算机科学教学体系与国际教学体系的接轨做出努力。

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# PREFACE

The general premise of the first edition of this book was a balanced treatment of logic design, digital system design and computer design basics. Prior to the first edition, the advancing scale of integration of digital electronic circuits and accelerated use of logic synthesis tools had raised much of digital system design to levels above gates and flip-flops. Register transfer level treatment of datapaths and controls, including hardware description language use, became central to industrial practice. Moreover, the movement of computer design toward the so-called RISC (Reduced Instruction Set Computer) had penetrated to the very core of the domain of the CISC (Complex Instruction Set Computer). The RISC, with the accompanying pipelined implementation, became the predominate architecture for processors and served as the core component in CISC designs as well. Additionally, the use of multiple levels of memory hierarchy had become a dominant part of contemporary computers. The first edition of *Logic and Computer Design Fundamentals* provided an appropriate balance of topics for a contemporary treatment of design consistent with these changes in technology and industrial practice.

During the past four years, continuing advances in the scale of integration of digital electronic circuits and expanding application of logic and behavioral synthesis tools have established hardware description languages (HDLs) as the primary vehicle for describing digital and computer systems during design. Other changes in technology include broader application of dynamic RAM, increased interest in stack architectures with the emergence of Java, and the adoption of packet-based serial transfer standards for communication between computers and their peripherals. In responding to these trends, the second edition introduces both Verilog and VHDL, replacing content on IEEE standard graphic symbols. Also included is new material on dynamic RAM, stack architecture, and packet-based communication for input-output.

Pedagogical changes include added sequential circuit formulation material in Chapter 4 and computer examples in Chapter 8 that include the hardware for branch and jump instructions. The latter examples now permit a complete basic treatment of computer design, exclusive of the detailed designs in Chapter 10. Almost half of the many homework problems are either new or modified. A Companion Website is provided at <http://www.prenhall.com/mano>.

The approach used in the introductions to VHDL and Verilog contrasts with that in the typical programming or description language text. Here, the introductions emphasize the vital tie of HDL descriptions to hardware, causing the reader to recognize clearly that a language description represents actual hardware with real cost rather than just program code to be stored in memory and executed. Further, the introductions are informal, permitting beginning students to be able to read and write in a limited, but powerful, subset of

an HDL, while achieving a balance between language study and basic fundamentals appropriate for an introductory course. The organization of the VHDL and Verilog material is intended to provide three choices: coverage of VHDL, coverage of Verilog, or neither. These choices permit the instructor to tailor the material covered to the objectives of the course and exercise preference for one language over the other as well. If a greater language component is desired in a given course offering, VHDL and Verilog material provided on the Companion website serves this need.

Chapters 1 through 5 of the book treat logic design, and chapters 6 through 8 deal with digital system design using computer subsystem examples. Chapters 9 through 12 focus directly on computer design. This arrangement provides solid digital system design fundamentals while accomplishing a gradual, bottom-up development of fundamentals for use in top-down computer design in later chapters. Summaries of the topics covered in each chapter follow.

**Chapter 1** introduces digital and computer systems and information representation. Binary number and character representations and basic binary arithmetic are the focus of most of the chapter.

**Chapter 2** introduces logic gates and deals with basic concepts and techniques for designing gate circuits. The chapter presents Boolean algebra and Karnaugh maps as logic simplification tools and covers design using NAND, NOR and XOR gates. The chapter finishes with a brief treatment of fundamental properties of gates with a focus on propagation delay.

**Chapter 3** covers combinational circuit analysis and design. It introduces design hierarchy, computer-aided design, top-down design, synthesis, and presents computer-based digital simulation as an analysis tool. Several types of functional blocks which correspond to medium scale integrated (MSI) circuits are introduced or designed. Simplification of arithmetic hardware serves as motivation for the presentation of complement arithmetic. Introductions to the hardware description languages, VHDL and Verilog, are provided with the expectation that at most one of the languages will be covered.

**Chapter 4** presents sequential circuit concepts and design. This chapter introduces latches and flip-flops as storage elements and demonstrates sequential circuit analysis procedures. Design procedures include an expanded introduction to developing state diagrams and state tables from specifications. The design procedures focus on design using D flip-flops or J-K flip-flops. The introduction of VHDL and Verilog is extended to storage elements and to sequential circuits.

**Chapter 5** deals with structured sequential circuits, notably registers and counters. Shift registers are introduced and applied to serial operations. The discussion of counters focuses on the synchronous binary type. VHDL and Verilog descriptions of shift registers and counters are presented.

**Chapter 6** presents random access memory (RAM) and programmable logic. The RAM section deals with the structure of static and dynamic RAM integrated circuits and the interconnection of such circuits to form a memory. In addition to treating three basic forms of programmable logic, this chapter covers large scale programmable logic including field programmable gate arrays.

**Chapter 7** introduces a simple register transfer language and shows its relationship to hardware description languages. It treats register transfer operations and introduces methods for implementing transfers with and without buses. A major part of Chapter 7 is the design of a basic computer datapath including a pipelined version. This datapath design serves as the foundation for all computer datapaths treated in the remainder of the book. The introduction of the simple hardware description language permits the remainder of the material in the text to be presented independently of Verilog and VHDL.

**Chapter 8** deals with the sequencing of register transfer operations. It introduces the algorithmic state machine (ASM) chart as a representation for sequencing and controlling operations. Hardwired and microprogrammed versions of a binary multiplier illustrate ASM use and sequential control design. In addition, the binary multiplier serves as an example for introducing the use of VHDL and Verilog in describing combined datapath and control. A simple computer is built upon the basic datapath from Chapter 7 by adding hardwired control. A more complex microprogrammed control is described and the chapter finishes with a simple pipelined computer.

**Chapter 9** introduces many facets of instruction set architecture. It deals with address count, addressing modes, architectures, and the various types of instructions including data transfer, data manipulation, floating point, program control and program interrupt. Addressing modes and other aspects of instructions are illustrated with brief segments of instruction code.

**Chapter 10** illustrates and compares two different CPU designs, one CISC and one RISC. Except for a bit of comparison, the designs are independent, so either one or both may be covered based on the audience and on the time available. The CISC design uses a conventional datapath and microprogrammed control. The RISC design uses a pipelined datapath and hardwired control. The chapter concludes with a brief overview of more advanced concepts in CPU design.

**Chapter 11** deals with data transfer between the CPU, input-output interfaces and peripheral devices. Discussion of a keyboard, a CRT display and a hard disk as peripherals is included and a keyboard interface is illustrated. Other topics covered range from serial communication, including the Universal Serial Bus (USB) as an illustration, to I/O processors.

**Chapter 12** covers memory systems with a particular focus on memory hierarchies. The concept of locality of reference is introduced and illustrated by consideration of the cache/main memory and main memory/hard disk relationships. An overview of cache design parameters is provided. The treatment of memory management focuses on paging and a translation lookaside buffer structure.

**Companion Website** (<http://www.prenhall.com/mano>) content includes the following material:

1. Book sections from the first edition, but not appearing in the second edition,
2. Additional VHDL and Verilog topics, including problems for Chapters 5, 6, 7 and 8,
3. VHDL and Verilog source files for all examples,
4. Solutions for about one-third of all text and Web site problems, and
5. Transparency originals for all complex figures and tables.



**Instructor's Manual** content includes suggestions for use of the book, information for obtaining alternative CAD tools, and all problem solutions. This manual is available to course instructors from Prentice Hall.

Because of its broad coverage of both logic and computer design, with the proper selection of material, this book can serve several different objectives in sophomore through junior level courses. Text coverage, described next for each objective in terms of a 3-credit to 4-credit, semester course, can be appropriately adjusted for other credit and term constraints. Chapters 1 through 9 plus 11 provide an overview of hardware for computer science, computer engineering, and electrical engineering students in a single semester course. Coverage of Chapters 1 through 8 in a semester, perhaps with some supplementary material or a laboratory, provides a contemporary logic design treatment. Coverage of the entire book, with supplementary material including a laboratory, can provide a two-semester sequence in logic design and computer architecture. Finally, due to its moderately paced treatment of a wide range of topics, the book is ideal for self-study by engineers and computer scientists.

Among the contributions of many people to this book, feedback on the proposal for the second edition provided by Cherrice Traver, Union College; David W. Capson, McMaster University; Alexandros Eleftheriadis, Columbia University; D. D. Freund, California State University- Sacramento; Jim Harris, California Polytechnic State University- San Luis Obispo; Robert F. Hodson, Christopher Newport University; John A. Rupf, Southern Polytechnic State University; and Yu Hen Hu, University of Wisconsin- Madison heavily influenced the second edition. A special thanks is due to those providing corrections to the first edition, notably Professor Stephen Mann and his colleagues at the University of Waterloo, for providing significant corrections to the CISC processor in Chapter 10.

We thank those at Prentice Hall who have had a role in bringing about this edition. Notable are: Tom Robbins, for his sound guidance, support and patience, Alice Dworkin, for her help on many details, and Scott Disanno, for coordinating and contributing to the final text production in record time.

Finally, a very special thanks is extended to Val Kime for her inexhaustible support and understanding throughout the development of the second edition.

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# 目录概览

第 1 章	数字计算机与信息·····	3
	Digital Computers and Information	
第 2 章	组合逻辑电路·····	27
	Combinational Logic Circuits	
第 3 章	组合逻辑设计·····	91
	Combinational Logic Design	
第 4 章	时序电路·····	183
	Sequential Circuits	
第 5 章	寄存器与计数器·····	249
	Registers and Counters	
第 6 章	存储器与可编程逻辑设备·····	285
	Memory and Programmable Logic Devices	
第 7 章	寄存器传输与数据通路·····	339
	Register Transfers and Datapaths	
第 8 章	时序与控制·····	391
	Sequencing and Control	
第 9 章	指令集结构·····	467
	Instruction Set Architecture	
第 10 章	中央处理器设计·····	511
	Central Processing Unit Designs	
第 11 章	输入输出与通信·····	575
	Input-Output and Communication	
第 12 章	存储系统·····	613
	Memory Systems	

# CONTENTS

## □ Chapter 1 3

---

### DIGITAL COMPUTERS AND INFORMATION

- 1-1 Digital Computers
  - Information Representation
  - Computer Structure
  - More on the Generic Computer
- 1-2 Number Systems
  - Binary Numbers
  - Octal and Hexadecimal Numbers
  - Number Ranges
- 1-3 Arithmetic Operations
  - Conversion from Decimal to Other Bases
- 1-4 Decimal Codes
  - BCD Addition
- 1-5 Alphanumeric Codes
  - ASCII Character Code
  - Parity Bit
- 1-6 Chapter Summary
  - References
  - Problems

## □ CHAPTER 2 27

---

### COMBINATIONAL LOGIC CIRCUITS

- 2-1 Binary Logic and Gates
  - Binary Logic
  - Logic Gates
- 2-2 Boolean Algebra
  - Basic Identities of Boolean Algebra
  - Algebraic Manipulation
  - Complement of a Function

2-3	Standard Forms	39
	Minterms and Maxterms	39
	Sum of Products	43
	Product of Sums	44
2-4	Map Simplification	45
	Two-Variable Map	46
	Three-Variable Map	47
	Four-Variable Map	52
2-5	Map Manipulation	55
	Essential Prime Implicants	55
	Nonessential Prime Implicants	57
	Product-of-Sums Simplification	58
	Don't-Care Conditions	60
2-6	NAND and NOR Gates	62
	NAND Circuits	64
	Two-Level Implementation	65
	Multilevel NAND Circuits	67
	NOR Circuits	69
2-7	Exclusive-OR Gates	71
	Odd Function	73
	Parity Generation and Checking	74
2-8	Integrated Circuits	76
	Levels of Integration	76
	Digital Logic Families	76
	Positive and Negative Logic	79
	Transmission Gates	81
2-9	Chapter Summary	82
	References	83
	Problems	83

## □ CHAPTER 3 **91**

---

	COMBINATIONAL LOGIC DESIGN	91
3-1	Combinational Circuits	91
3-2	Design Topics	92
	Design Hierarchy	93
	Top-Down Design	96
	Computer-Aided Design	96
	Hardware Description Languages	97
	Logic Synthesis	99
3-3	Analysis Procedure	100
	Derivation of Boolean Functions	101
	Derivation of the Truth Table	102
	Logic Simulation	103

3-4	Design Procedure	105
	Code Converters	107
3-5	Decoders	111
	Decoder Expansion	113
	Combinational Circuit Implementation	114
3-6	Encoders	116
	Priority Encoder	117
3-7	Multiplexers	119
	Combinational Circuit Implementation	122
	Demultiplexer	124
3-8	Binary Adders	125
	Half Adder	125
	Full Adder	126
	Binary Ripple Carry Adder	127
	Carry Lookahead Adder	129
3-9	Binary Subtraction	132
	Complements	134
	Subtraction with Complements	135
3-10	Binary Adder-Subtractors	137
	Signed Binary Numbers	138
	Signed Binary Addition and Subtraction	140
	Overflow	142
3-11	Binary Multipliers	144
3-12	Decimal Arithmetic	145
	Use of Complements in Decimal	147
3-13	HDL Representations – VHDL	148
	Structural Description	150
	Dataflow Description	153
	Hierarchical Description	155
	Behavioral Description	157
3-14	HDL Representations - Verilog	159
	Structural Description	160
	Dataflow Description	161
	Hierarchical Description	165
	Behavioral Description	165
3-15	Chapter Summary	167
	References	168
	Problems	168

## □ CHAPTER 4 **183**

---

SEQUENTIAL CIRCUITS	183
4-1 Sequential Circuit Definitions	184

4-2	Latches	186
	SR and S R Latches	187
	D Latch	190
4-3	Flip-Flops	191
	Master-Slave Flip-Flop	192
	Edge-Triggered Flip-Flop	195
	Standard Graphics Symbols	197
	Characteristic Tables	199
	Direct Inputs	200
4-4	Sequential Circuit Analysis	201
	Input Equations	201
	State Table	202
	Analysis with JK Flip-Flops	206
	State Diagram	206
4-5	Sequential Circuit Design	208
	Design Procedure	208
	Finding State Diagrams and State Tables	209
4-6	Designing with D Flip-Flops	214
	Designing with Unused States	215
4-7	Designing with JK Flip-Flops	218
	Flip-Flop Excitation Tables	218
	Design Procedure	219
4-8	HDL Representation for Sequential Circuits – VHDL	224
4-9	HDL Representation for Sequential Circuits – Verilog	232
4-10	References	239
	Problems	240

## □ CHAPTER 5 **249**

---

<b>REGISTERS AND COUNTERS</b>		<b>249</b>
5-1	Definition of Register and Counter	249
5-2	Registers	250
	Register with Parallel Load	251
5-3	Shift Registers	253
	Serial Transfer	254
	Serial Addition	256
	Shift Register with Parallel Load	258
	Bidirectional Shift Register	260
5-4	Ripple Counter	261
5-5	Synchronous Binary Counters	263
	Design of Binary Counters	264
	Counter with D Flip-Flops	267
	Serial and Parallel Counters	268
	Up-Down Binary Counter	269
	Binary Counter with Parallel Load	270

5-6	Other Counters	273
	BCD Counter	273
	Arbitrary Count Sequence	274
5-7	HDL Representation for Shift Registers and Counters	276
5-8	HDL Representation for Shift Registers and Counters	278
5-9	Chapter Summary	279
	References	280
	Problems	280

## □ CHAPTER 6 **285**

---

	MEMORY AND PROGRAMMABLE LOGIC DEVICES	285
6-1	Memory and Programmable Logic Device	285
	Definitions	286
6-2	Random-access Memory	287
	Write and Read Operations	289
	Timing Waveforms	290
	Properties of Memory	292
6-3	RAM Integrated Circuits	292
	Three-State Buffers	296
	Coincident Selection	297
	Dynamic RAM ICs	301
6-4	Array of RAM ICs	307
	Arrays of Dynamic RAM ICs	310
6-5	Programmable Logic Technologies	310
6-6	Read-only Memory	312
	Combinational Circuit Implementation	315
6-7	Programmable Logic Array	317
6-8	Programmable Array Logic Devices	321
6-9	VLSI Programmable Logic Devices	326
	Altera MAX 7000 CPLDs	326
	Xilinx XC4000 Structure	328
	Xilinx Interconnections	330
	Xilinx Logic	331
6-10	Chapter Summary	333
	References	334
	Problems	335

## □ CHAPTER 7 **339**

---

	REGISTER TRANSFERS AND DATAPATHS	339
7-1	Datapaths and Operations	340



7-2	Register Transfer Operations	341
	A Note For VHDL And Verilog Users Only	344
7-3	Microoperations	345
	Arithmetic Microoperations	345
	Logic Microoperations	347
	Shift Microoperations	349
7-4	Multiplexer-based Transfer	350
7-5	Bus-based Transfer	351
	Three-State Bus	353
	Memory Transfer	355
7-6	Datapaths	357
7-7	The Arithmetic/Logic Unit	360
	Arithmetic Circuit	360
	Logic Circuit	363
	Arithmetic/Logic Unit	364
7-8	The Shifter	366
	Barrel Shifter	367
7-9	Datapath Representation	368
7-10	The Control Word	370
7-11	Pipelined Datapath	376
	Execution of Pipeline Microoperations	381
7-12	Chapter Summary	382
	References	383
	Problems	383

## □ CHAPTER 8 **391**

---

	SEQUENCING AND CONTROL	391
8-1	The Control Unit	392
8-2	Algorithmic State Machines	393
	The ASM Chart	393
	Timing Considerations	396
8-3	Design Example: Binary Multiplier	397
	Binary Multiplier	397
	Multiplier Datapath	399
	ASM Chart for Multiplier	400
8-4	Hardwired Control	402
	Sequence Register and Decoder	404
	One Flip-Flop per State	406
8-5	HDL Representation of the Binary Multiplier - VHDL	410
8-6	HDL Representation of the Binary Multiplier - Verilog	413
8-7	Microprogrammed Control	416
	Binary Multiplier Example	418