国外计算机科学教材系列

数字逻辑与计算机硬件设计基础

（第二版）

Logic and Computer Design Fundamentals

Second Edition Updated

英文原版

[美] M. Morris Mano
Charles R. Kime 著

Prentice Hall

電子工業出版社
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内容简介

本书是根据美国重点大学新版计算机教学计划而编写的教材，全书共分为数字逻辑设计、计算机硬件设计和计算机设计三个部分，主要包括信息的二进制表示及布尔逻辑、组合电路的分析和设计基础、VHDL和Verilog语言、时序电路的概念和设计、结构化时序电路设计、RAM和可编程逻辑设计、数据通路和控制单元的设计、寄存器传输操作的时序设计、指令集结构、数据传输总线设计和存储系统设计等。

与传统的数字逻辑教材相比，本书内容广泛，更加面向硬件设计。它在介绍数字逻辑的基础上，直接介绍了硬件设计和计算机设计的知识，其设计内容反映了当今最新技术的发展趋势。此外，书中有大量的练习题，以帮助读者掌握和巩固所学知识。

本书可作为国内计算机专业数字逻辑和计算机组织结构课程的教材和辅助教科书，也可作为计算机硬件爱好者的参考书。

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出 版 说 明

21世纪初的5至10年是我国国民经济和社会发展的重要时期，也是信息产业快速发展的关键时期。在我国加入WTO后的今天，培养一支适应国际化竞争的一流IT人才队伍是我国高等教育的重要任务之一。信息科学和技术方面人才的优劣与多寡，是我国面对国际竞争时成败的关键因素。

当前，正值我国高等教育特别是信息科学领域的教育调整、变革的重大时期，为使我国教育体制与国际化接轨，有条件的高等院校正在为某些信息学科和技术课程使用国外优秀教材和优秀原版教材，以使我国在计算机教学上尽快赶上国际先进水平。

电子工业出版社秉承多年来引进国外优秀图书的经验，翻译出版了“国外计算机科学教材系列”丛书，这套教材覆盖学科范围广、领域宽、层次多，既有本科专业课程教材，也有研究生课程教材，以适应不同院系、不同专业、不同层次的师生对教材的需求，广大师生可自由选择和自由组合使用。这些教材涉及的学科方向包括网络与通信、操作系统、计算机组织与结构、算法与数据结构、数据库与信息处理、编程语言、图形图像与多媒体、软件工程等。同时，我们也适当引进了一些优秀英文原版教材，本着翻译版本和英文原版并重的原则，对重点图书既提供英文原版又提供相应的翻译版本。

在图书选题上，我们大都选择国外著名出版公司出版的高校教材，如Pearson Education培生教育出版集团、麦格劳－希尔教育出版集团、麻省理工学院出版社、剑桥大学出版社等。撰写教材的许多作者都是蜚声世界的教授、学者，如道格拉斯·科默（Douglas E. Comer）、威廉·斯托林斯（William Stallings）、哈维·戴特尔（Harvey M. Deitel）、尤利斯·布莱克（Uyless Black）等。

为确保教材的选题质量和翻译质量，我们约请了清华大学、北京大学、北京航空航天大学、复旦大学、上海交通大学、南京大学、浙江大学、哈尔滨工业大学、华中科技大学、西安交通大学、国防科学技术大学、解放军理工大学等著名高校的教授和骨干教师参与了本系列教材的选题、翻译和审校工作。他们中既有讲授同类教材的骨干教师、博士，也有积累了几十年教学经验的老教授和博士生导师。

在该系列教材的选题、翻译和编辑加工过程中，为提高教材质量，我们做了大量细致的工作，包括对所选教材进行全面论证；选择编辑时力求达到专业对口；对排版、印制质量进行严格把关。对于英文教材中出现的错误，我们通过与作者联络和网上下载勘误表等方式，逐一进行了修订。

此外，我们还将与国外著名出版公司合作，提供一些教材的教学支持资料，希望能为授课老师提供帮助。今后，我们将继续加强与各高校教师的密切联系，为广大师生引进更多的国外优秀教材和参考书，为我国计算机科学教学体系与国际教学体系的接轨做出努力。

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PREFACE

The general premise of the first edition of this book was a balanced treatment of logic design, digital system design and computer design basics. Prior to the first edition, the advancing scale of integration of digital electronic circuits and accelerated use of logic synthesis tools had raised much of digital system design to levels above gates and flip-flops. Register transfer level treatment of datapaths and controls, including hardware description language use, became central to industrial practice. Moreover, the movement of computer design toward the so-called RISC (Reduced Instruction Set Computer) had penetrated to the very core of the domain of the CISC (Complex Instruction Set Computer). The RISC, with the accompanying pipelined implementation, became the predominate architecture for processors and served as the core component in CISC designs as well. Additionally, the use of multiple levels of memory hierarchy had become a dominant part of contemporary computers. The first edition of *Logic and Computer Design Fundamentals* provided an appropriate balance of topics for a contemporary treatment of design consistent with these changes in technology and industrial practice.

During the past four years, continuing advances in the scale of integration of digital electronic circuits and expanding application of logic and behavioral synthesis tools have established hardware description languages (HDLs) as the primary vehicle for describing digital and computer systems during design. Other changes in technology include broader application of dynamic RAM, increased interest in stack architectures with the emergence of Java, and the adoption of packet-based serial transfer standards for communication between computers and their peripherals. In responding to these trends, the second edition introduces both Verilog and VHDL, replacing content on IEEE standard graphic symbols. Also included is new material on dynamic RAM, stack architecture, and packet-based communication for input-output.

Pedagogical changes include added sequential circuit formulation material in Chapter 4 and computer examples in Chapter 8 that include the hardware for branch and jump instructions. The latter examples now permit a complete basic treatment of computer design, exclusive of the detailed designs in Chapter 10. Almost half of the many homework problems are either new or modified. A Companion Website is provided at http://www, prenhall.com/mano.

The approach used in the introductions to VHDL and Verilog contrasts with that in the typical programming or description language text. Here, the introductions emphasize the vital tie of HDL descriptions to hardware, causing the reader to recognize clearly that a language description represents actual hardware with real cost rather than just program code to be stored in memory and executed. Further, the introductions are informal, permitting beginning students to be able to read and write in a limited, but powerful, subset of

an HDL, while achieving a balance between language study and basic fundamentals appropriate for an introductory course. The organization of the VHDL and Verilog material is intended to provide three choices: coverage of VHDL, coverage of Verilog, or neither. These choices permit the instructor to tailor the material covered to the objectives of the course and exercise preference for one language over the other as well. If a greater language component is desired in a given course offering, VHDL and Verilog material provided on the Companion website serves this need.

Chapters 1 through 5 of the book treat logic design, and chapters 6 through 8 deal with digital system design using computer subsystem examples. Chapters 9 through 12 focus directly on computer design. This arrangement provides solid digital system design fundamentals while accomplishing a gradual, bottom-up development of fundamentals for use in top-down computer design in later chapters. Summaries of the topics covered in each chapter follow.

Chapter 1 introduces digital and computer systems and information representation. Binary number and character representations and basic binary arithmetic are the focus of most of the chapter.

Chapter 2 introduces logic gates and deals with basic concepts and techniques for designing gate circuits. The chapter presents Boolean algebra and Karnaugh maps as logic simplification tools and covers design using NAND, NOR and XOR gates. The chapter finishes with a brief treatment of fundamental properties of gates with a focus on propagation delay.

Chapter 3 covers combinational circuit analysis and design. It introduces design hierarchy, computer-aided design, top-down design, synthesis, and presents computer-based digital simulation as an analysis tool. Several types of functional blocks which correspond to medium scale integrated (MSI) circuits are introduced or designed. Simplification of arithmetic hardware serves as motivation for the presentation of complement arithmetic. Introductions to the hardware description languages, VHDL and Verilog, are provided with the expectation that at most one of the languages will be covered.

Chapter 4 presents sequential circuit concepts and design. This chapter introduces latches and flip-flops as storage elements and demonstrates sequential circuitanalysis procedures. Design procedures include an expanded introduction to developing state diagrams and state tables from specifications. The design procedures focus on design using D flip-ilops or J-K flip-ilops. The introduction of VHDL and Verilog is extended to storage elements and to sequential circuits.

Chapter 5 deals with structured sequential circuits, notably registers and counters. Shift registers are introduced and applied to serial operations. The discussion of counters focuses on the synchronous binary type. VHDL and Verilog descriptions of shift registers and counters are presented.

Chapter 6 presents random access memory (RAM) and programmable logic. The RAM section deals with the structure of static and dynamic RAM integrated circuits and the interconnection of such circuits to form a memory. In addition to treating three basic forms of programmable logic, this chapter covers large scale programmable logic including field programmable gate arrays.

Chapter 7 introduces a simple register transfer language and shows its relationship to hardware description languages. It treats register transfer operations and introduces methods for implementing transfers with and without buses. A major part of Chapter 7 is the design of a basic computer datapath including a pipelined version. This datapath design serves as the foundation for all computer datapaths treated in the remainder of the book. The introduction of the simple hardware description language permits the remainder of the material in the text to be presented independently of Verilog and VHDL.

Chapter 8 deals with the sequencing of register transfer operations. It introduces the algorithmic state machine (ASM) chart as a representation for sequencing and controlling operations. Hardwired and microprogrammed versions of a binary multiplier illustrate ASM use and sequential control design. In addition, the binary multiplier serves as an example for introducing the use of VHDL and Verilog in describing combined datapath and control. A simple computer is built upon the basic datapath from Chapter 7 by adding hardwired control. A more complex microprogrammed control is described and the chapter finishes with a simple pipelined computer.

Chapter 9 introduces many facets of instruction set architecture. It deals with address count, addressing modes, architectures, and the various types of instructions including data transfer, data manipulation, floating point, program control and program interrupt. Addressing modes and other aspects of instructions are illustrated with brief segments of instruction code.

Chapter 10 illustrates and compares two different CPU designs, one CISC and one RISC. Except for a bit of comparison, the designs are independent, so either one or both may be covered based on the audience and on the time available. The CISC design uses a conventional datapath and microprogrammed control. The RISC design uses a pipelined datapath and hardwired control. The chapter concludes with a brief overview of more advanced concepts in CPU design.

Chapter 11 deals with data transfer between the CPU, input-output interfaces and peripheral devices. Discussion of a keyboard, a CRT display and a hard disk as peripherals is included and a keyboard interface is illustrated. Other topics covered range from serial communication, including the Universal Serial Bus (USB) as an illustration, to I/O processors.

Chapter 12 covers memory systems with a particular focus on memory hierarchies. The concept of locality of reference is introduced and illustrated by consideration of the cache/main memory and main memory/hard disk relationships. An overview of cache design parameters is provided. The treatment of memory management focuses on paging and a translation lookaside buffer structure.

Companion Website (http://www. prenhall.com/mano) content includes the following material:

1. Book sections from the first edition, but not appearing in the second edition,
2. Additional VHDL and Verilog topics, including problems for Chapters 5, 6, 7 and 8,
3. VHDL and Verilog source files for all examples,
4. Solutions for about one-third of all text and Web site problems, and
5. Transparency originals for all complex figures and tables.

Instructor's Manual content includes suggestions for use of the book, information for obtaining alternative CAD tools, and all problem solutions. This manual is available to course instructors from Prentice Hall.

Because. of its broad coverage of both logic and computer design, with the proper selection of material, this book can serve several different objectives in sophomore through junior level courses. Text coverage, described next for each objective in terms of a.3-credit to 4-credit. semester course, can be appropriately adjusted for other credit and term constraints. Chapters 1 through 9 plus. 11 provide an overview of hardware for computer science, computer engineering, and electrical engineering students in a single semester course. Coverage of Chapters 1 through 8 in a semester, perhaps with some supplementary material or a laboratory, provides a contemporary logic design treatment. Coverage of the entire book, with supplementary material including a laboratory, can provide a two-semester sequence in logic design and computer architecture. Finally, due to its moderatelypaced treatment of a wide range of topics, the book is ideal for self-study by engineers and computer scientists.

Among the contributions of many people to this book, feedback on the proposal for the second edition provided by Cherrice Traver, Union College; David W.Capson, McMaster University; Alexandros Eleftheriadis, Columbia University; D. D. Freund, California State University- Sacramento; Jim Harris, California Polytechnic State University- San Luis Obispo; Robert F Hodson, Christopher Newport University; John A. Rupf, Southern Polytechnic State University; and Yu Hen Hu, University of Wisconsin- Madison heavily influenced the second edition. A special thanks is due to those providing corrections to the first edition, notably Professor Stephen Mann and his colleagues at the University of Waterloo, for providing significant corrections to the CISC processor in Chapter 10.

We thank those at Prentice Hall who have had a role in bringing about this edition. Notable are: Tom Robbins, for his sound guidance, support and patience, Alice Dworkin, for her help on many details, and Scott Disanno, for coordinating and contributing to the final text production in record time.

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M. Morris Mano
Charles R. Kime

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