世界TTL/IC規格、互換表

THE WORLD TTL, IC DATA & CROSS-REFERENCE GUIDE

最新版

MITSUBISHI

TEXAS INSTRUMENTS

MOTOROLA

SIEMENS

NEC

signetics

HITACHI

NS

PHILIPS

TOSHIBA

FAIRCHILD

FUJITSU

AMD

全華科技圖書股份有限公司 印行

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PREFACE
(序　言)

電晶體發明以來，電子技術的進步很迅速，特別是以空間電子技術爲背景產生的積體電路 (Integrated Circuit；IC) ，與電子工業界所要求的經濟化、多機能化、小型化的要求，彼此恰能相輔相成，而造成了繼電晶體時代後的新時代。

IC使電子機器更具經濟性，且使設計更合理化，因此廣泛用於民生、通信及工業機器領域。技術的開發使IC性能飛躍提高，低消費電力化、高速化、高積體化、高可靠性化，使得IC由電路導向(SSI、MSI)走向系統導向(LSI、VLSI)。

這幾年來新IC群陸續出現，種類繁多，對設計者而言，選用適當的IC成爲主題。在這種局勢下Bipolar Digital(雙極性數位)IC中，還是以TTL(Transistor-Transistor-Logic)IC爲主，其種類繁多、高可靠信與經濟性，因此不僅用於電子工業，也常用於其他工業的機器。

邏輯用IC主流的TTL IC，第一代（SN54/74HXX、SN54/74XX、SN54/74LXX）採金摻雜技術，第二代（SN54/74LSXX、SN54/74/SXX）採肖特基技術，第三代（SN54/74ALSXX、SN54/74ASXX、FAST TTL），考慮性能指數採氧化絕緣及離子注入技術，此第三代TTL成爲今後雙極性數位IC的主流。

各廠商銷售的TTL IC的型名、規格逐漸趨向統一化，但還不太完全。維護各種電子機器或設計製作各種電子電路時，要將各廠商的資料手册隨置於側，實有其困難，因此依各廠商的最新資料，將TTL IC群和TEXAS INSTRUMENTS的主要TTL IC，特別是以第二代、第三代TTL IC爲中心做成規格互換表。

希望本書在機器維護，及瞭解各廠牌TTL IC的互換與規格上，能對讀者有所幫助，以便置於座右常加應用。

本書內容承蒙德州儀器公司亞洲分公司的田中和彥氏，及日本摩托羅拉公司的中林善泰氏，提供很多寶貴的意見，在此謹致謝意，並對提供各項資料的德州儀器公司，及各廠商表達謝意。

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我們的宗旨：

感謝您選購全華圖書
希望本書能滿足您求知的慾望

為保護您的眼睛，本公司特別採用不反光的米色印書紙!!

PRACTICAL GUIDE

（使用指導）

PRACTICAL GUIDE（使用指導）

本資料手册主要的部份爲互換表及資料單，互換表係以德州儀器公司（T.I.）之數位TTL積體電路爲主體，與世界上代表的12家廠商製造的數位積體電路列爲一互換表。

而資料單係以T.I.公司的數位TTL積體電路爲代表，記載其電氣上的特性及接脚分配圖、功能表、電路圖、功能方塊圖等。

這13家廠商之IC，其互換性係以電路功能、接脚分配、主要電氣特性、温度範圍爲主，其他電氣上的特性、温度範圍及電路圖之細節並不一定完全相同，使用時，只要針對其使用用途，確定兩者之規格完全相同，即可互換使用。

最後，如互換後，若有產生不良之後果，敬請原諒。

各廠家記載之規格如需要更詳細的資料，請與下列公司連絡。

TEXAS INSTRUMENTS	03 (498) 2111	德州儀器公司
FAIRCHILD	03 (400) 8351	日本快捷半導體公司
MOTOROLA	03 (440) 3311	日本摩托羅拉公司
N.S.C.	03 (349) 0811	日本ノャパン
PHILIPS	03 (448) 5555	日本菲立普公司
SIGNETICS	03 (230) 1521	日本SIGNETICS公司
SIEMENS	03 (490) 2171	日本西門子公司
FUJITSU	03 (502) 0161	日本富士通公司
HITACHI	03 (270) 2111	日立公司（日本）
MITSUBISHI	03 (218) 3349	三菱電機公司（日本）
NEC	03 (453) 5511	日本電氣公司（日本）
TOSHIBA	03 (522) 2111	東芝電氣公司（日本）
A.M.D.	03 (329) 2751	Advanced Micro Devices公司（美國）

PRACTICAL GUIDE （使用指導）

○Cross-Reference Table Guide（交叉參考表指引）

Example：

2

	Schottky TTL					High-Speed TTL					Low-Power Schottky TTL					Standard TTL					Low-Power TTL				
	Device Type	Package				Device Type	Package				Device Type	Package				Device Type	Package				Device Type	Package			
		C	P	M	CF		C	P	M	CF		C	P	M	CF		C	P	M	CF		C	P	M	CF
T.I.	SN54S00	J①	N①		W①	SN54H00	J①			W①	SN54LS00	J①				SN5400	J①			W②	SN54L00	J①	N①	T②	
	SN74S00	J①	N①			SN74H00	J①	N①			SN74LS00	J①	N①			SN7400	J①	N①			SN74L00	J①	N①	T②	

1 3 4 3 4 3 4 3 4 3 4

1 Manufacturer（製造商）

T.I.	Texas Instruments Incorporated 德州儀器公司（美國）
FAIRCHILD	Fairchild Camera and Instrument Corporation 快捷半導體公司（美國）
MOTOROLA	Motorola Semiconductor Products Inc. 摩托羅拉公司（美國）
N.S.C.	National Semiconductor Corporation 國際半導體公司（美國）
PHILIPS	Philips Gloelampenfabrieken, Eindoven 菲立普公司（荷蘭）
SIGNETICS	Signetics Corporation SIGNETICS公司（美國）
SIEMENS	Siemens Aktiengesellschaft 西門子公司（西德）
FUJITSU	富士通公司（日本）
HITACHI	日立公司（日本）
MITSUBISHI	三菱電機公司（日本）
NEC	日本電氣公司（日本）
TOSHIBA	東芝電氣公司（日本）
A.M.D.	Advanced Micro Devices 公司（美國）

2 Classification of TTL（TTL的種類）

Schottky TTL（蕭特基TTL）
High-Speed TTL（高速TTL）
Low-Power Schottky TTL（低功率蕭特基TTL）
Standard TTL（標準TTL）
Low-Power TTL（低功率TTL）
Advanced Low-Power Schottky TTL（高級低功率蕭特基TTL）
Advanced Schottky TTL（高級蕭特基TTL）
FAST TTL（快速TTL）

3 Device Type（型號）

Upper Side 上段：Military Use（上段：軍用）
Lower Side 下段：Commercial／industry Use（下段：商業／工業用）

4 Package Type（包裝型式）

C：Ceramic Dual In-Line Package（陶質，並行接腳包裝）
P：Plastic Dual In-Line Package（塑膠，並行接腳包裝）
M：Metal Flat Package（金屬，平面接腳包裝）
CF：Ceramic Flat Package（陶質，平面接腳包裝）

The digit number in package sections refer to the figured number in the Pin Assignments.
（包裝部份之數字號碼是表示其接腳安排之圖形號碼。）

○Data Sheet Guide（資料表指引）

In this book, the each technical data used on the individual data sheet is that of Texas Instruments Digital TTL Integrated Circuits and the each device type for the individual data sheet represents as follows:
（本書中，各個資料表中所使用的每一個技術資料都是以德州儀器的數位TTL積體電路爲主，且各個資料表的每一裝置之型式表示如下：）

Example：Electrical Characteristics SN5400／SN7400

LETTER SYMBOLS, TERMS, AND DEFINITIONS

(文字記號，術語，定義)

LETTER SYMBOLS, TERMS, AND DEFINITIONS

(文字記號，術語，定義)

VOLTAGE

V_{IH} **High-level input voltage** **輸入高電位**

An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables.

Note: A minimum is specified that is the least positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} **Low-level input voltage** **輸入低電位**

An input voltage level within the less positive (more negative) of the two ranges of values used to represent the binary variables.

Note: A maximum is specified that is the most positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IK} **Input clamp voltage** **輸入箝位電壓**

An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.

V_{OH} **High-level output voltage** **輸出高電位**

The voltage at an output terminal with input conditions applied that according to the product specification will establish a high level at the output.

V_{OL} **Low-level output voltage** **輸出低電位**

The voltage at an output terminal with input conditions applied that according to the product specification will establish a low level at the output.

$V_{O(on)}$ **On-state output voltage** **導通狀態之輸出電壓**

The voltage at an output terminal with input conditions applied that according to the product specification will cause the output switching element to be in the on state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

$V_{O(off)}$ **Off-state output voltage** **截止狀態之輸出電壓**

The voltage at an output terminal with input conditions applied that according to the product specification will cause the output switching element to be in the off state.

Note: This characteristic is usually specified only for outputs not having internal pull-up elements.

V_{T+} **Positive-going threshold voltage** **輸入端由低電位升爲高電位之定限電壓**

The voltage level at an input that causes operation of the logic element according to specification as the input voltage rises from a level below the negative-going threshold voltage, V_{T-}.

V_{T-} **Negative-going threshold voltage** **輸入端由高電位降爲低電位之定限電壓**

The voltage level at an input that causes operation of the logic element according to specification as the input voltage falls from a level above the positive-going threshold voltage, V_{T+}.

CURRENT

I_{IH} **High-level input current** **高電位輸入電流**

The current into* an input when a high-level voltage is applied to that input.

I_{IL} **Low-level input current** **低電位輸入電流**

The current into* an input when a low-level voltage is applied to that input.

I_{OH} **High-level output current** **高電位輸出電流**

The current into* an output with input conditions applied that according to the product specification will establish a high level at the output.

I_{OL} **Low-level output current** **低電位輸出電流**

The current into* an output with input conditions applied that according to the product specification will establish a low level at the output.

$I_{O(off)}$ **Off-state output current** **截止狀態之輸出電流**

The current flowing into* an output with input conditions applied that according to the product specification will cause the output switching element to be in the off state.

Note: This parameter is usually specified for open-collector outputs intended to drive devices other than logic circuits.

I_{OZ} **Off-state (high-impedance-state) output current (of a three-state output)** **三態輸出的截止狀態(高阻抗狀態)輸出電流**

The current into* an output having three-state capability with input conditions applied that according to the product specification will establish the high-impedance state at the output.

I_{OS} **Short-circuit output current** **輸出短路電流**

The current into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).

I_{CC} **Supply current** **電源供給電流**

The current into* the V_{CC} supply terminal of an integrated circuit.

I_{CCH} **Supply current, output(s) high** **輸出高電位時之電源供給電流**

The current flowing into* the V_{CC} supply terminal of a circuit when the reference output(s) is (are) at a high-level voltage.

I_{CCL} **Supply current, output(s) low** **輸出低電位時之電源供給電流**

The current flowing into* the V_{CC} supply terminal of a circuit when the reference output(s) is (are) at a low-level voltage.

* Current flowing out of a terminal is a negative value.

LETTER SYMBOLS, TERMS, AND DEFINITIONS

(文字記號，術語，定義)

CLOCK FREQUENCY

f_{max} Maximum clock frequency 最高工作頻率

The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.

PULSE WIDTH

t_w Pulse width 脈衝寬

The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

RECOVERY TIME

t_{SR} Sense recovery time 檢出回復時間

The time interval needed to switch a memory from a write mode to a read mode and to obtain valid data signals at the output.

RELEASE TIME

$t_{release}$ Release time 釋放時間

The time interval between the release from a specified input terminal of data intended to be recognized and the occurrence of an active transition at another specified input terminal.

Note: When specified, the interval designated "release time" falls within the setup interval and constitutes, in effect, a negative hold time.

HOLD TIME

t_h Hold time 持續時間

The interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal.

Notes: 1. The hold time is the actual time between two events and may be insufficient to accomplish the intended result. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.

2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of data and the active transition) for which correct operation of the logic element is guaranteed.

SETUP TIME

t_{su} Setup time 設置時間

The time interval between the application of a signal that is maintained at a specified input terminal and a consecutive active transition at another specified input terminal.

Notes: 1. The setup time is the actual time between two events and may be insufficient to accomplish the setup. A minimum value is specified that is the shortest interval for which correct operation of the logic element is guaranteed.

2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the logic element is guaranteed.

PROPAGATION TIME

t_{PD} Propagation delay time 傳輸延遲時間

The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level.

t_{PLH} Propagation delay time, low-to-high-level output 輸出由低電位至高電位之傳輸延遲時間

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.

t_{PHL} Propagation delay time, high-to-low-level output 輸出由高電位至低電位之傳輸延遲時間

The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.

LETTERS SYMBOLS, TERMS, AND DEFINITIONS

(文字記號，術語，定義)

OUTPUT ENABLE AND DISABLE TIME

$t_{PZH}(t_{PZL})$ Output enable time (of a three-state output) to high level (or low level)
三態輸出由不動作至高電位或低電位所需時間
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high (or low) level.

t_{PZX} Output enable time (of a three-state output) to high or low level
三態輸出的位準由截止狀態到高或低電位的輸出可動作時間
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low).

$t_{PHZ}(t_{PLZ})$ Output disable time (of a three-state output) from high level (or low level)
三態輸出的位準由高(低)電位到截止狀態的輸出不動作時間
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from the defined high (or low) level to a high-impedance (off) state.

t_{PXZ} Output disable time (of a three-state output) from high or low level
三態輸出的位準由高或低電位到截止狀態的輸出不動作時間
The propagation delay time between the specified reference points on the input and output voltage waveforms with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state.

TRANSITION TIME

t_{TLH} Transition time, low-to-high-level 輸出由低電位至高電位之轉換時間.
The time between a specified low-level voltage and a specified high-level voltage on a waveform that is changing from the defined low level to the defined high level.

t_{THL} Transition time, high-to-low-level 輸出由高電位至低電位之轉換時間
The time between a specified high-level voltage and a specified low-level voltage on a waveform that is changing from the defined high level to the defined low level.

CLASSIFICATION OF CIRCUIT COMPLEXITY 依電路複雜性而分類

Gate Equivalent Circuit 閘等值電路
A basic unit-of-measure of relative digital-circuit complexity. The number of gate equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

SSI Small-Scale Integration 小型積體電路
Integrated circuits of less complexity than medium-scale integration (MSI).

MSI Medium-Scale Integration 中型積體電路
A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

LSI Large-Scale Integration 大型積體電路
A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context a major subsystem or system, whether digital or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

VLSI Very-Large-Scale Integration 超大型積體電路
A concept whereby a complete system function is fabricated as a single microcircuit. In this context, a system, whether digital or linear, is considered to be one that contains 1000 or more gates or circuitry of similar complexity.

NOMENCLATURE OF TTL INTEGRATED CIRCUITS

(數位TTL積體電路之命名法)

NOMENCLATURE OF TTL INTEGRATED CIRCUITS
(數位TTL積體電路之命名法)

TEXAS INSTRUMENS

Examples:

	(1)	(2)	(3)	(4)	(5)	(6)
SN	74	LS	195	A	J	
SN	2	9000	N			

(1) SN: Standard Prefix of TEXAS INSTRUMENTS (德州儀器公司標準字首)

(2) Operating Temperature Range (動作溫度範圍)

54: 55℃ to + 125℃ 2: 0℃ to + 75℃

74: 0℃ to + 70℃ 3: 55℃ to + 125℃

(3) Classification of TTL (TTL之分類)

54S/74S Schottky TTL 蕭特基 TTL

54H/74H High-Speed TTL 高速 TTL

54LS/74LS Low-Power Schottky TTL 低功率蕭特基 TTL

54/74 Standard TTL 標準 TTL

54L/74L Low-Power TTL 低功率 TTL

54ALS/74ALS Advanced Low-Power Schottky TTL

54AS/74AS Advanced Schottky TTL

(4) Consecutive Numbers to indicate the Each Type

(表示各種類之一連續數字編號)

(5) Alphabet: Series improved

(表示改良型之一連續文字符號)

(6) Package Type (包裝型式)

J: Ceramic Dual in-Line Package 陶瓷並行接腳包裝型式

JT: Ceramic Dual in-Line Package 陶瓷並行接腳包裝型式

JG: Ceramic Dual in-Line Package 陶瓷並行接腳包裝型式

N: Plastic Dual in-Line Package 塑膠並行接腳包裝型式

NT: Plastic Dual in-Line Package 塑膠並行接腳包裝型式

P: Plastic Dual in-Line Package 塑膠並行接腳包裝型式

T: Metal Flat Package 金屬平面接腳包裝型式

W: Ceramic Flat Package 陶瓷平面接腳包裝型式

MOTOROLA

Examples:

	(1)	(2)	(3)	(4)	(5)	(6)
MC	74	F	00	N		
SN	74	LS	113	A	N	
MC	8	300	P			

(1) MC: 55℃ of MOTOROLA MC-Number Series

SN: Prefix of MOROLA SN-Number Series

(2) Operating Temperature Range (動作溫度範圍)

54: -55℃ to + 125℃ 74: 0℃ to + 70℃

31: -55℃ to + 125℃ 30: 0℃ to 70℃

9: 55℃ to + 125℃ 8: 0℃ to + 75℃

(3) Classification of TTL (TTL之分類)

MC54/MC74 Standard TTL

MC54F/MC74F FAST Scottky TTL

SN54LS/SN74LS Low-Power Schottky TTL

SN54ALS/SN74ALS Advanced Low-Power Scottky TTL

(4) Consecutive Numbers to indicate the Each Type.

(表示各別種類之一連續數字編號)

(5) Alphabet: Series Improved

(表示改良型之一連續文字編號)

(6) Package Type (包裝型式)

J: Ceramic Dual In-Line Package

L: Ceramic Dual In-Line Package 陶瓷並行接腳包裝型式

P: Plastic Dual In-Line Package 塑膠並行接腳包裝型式

N: Plastic Dual In-Line Package 塑膠並行接腳包裝型式

F: Ceramic Flat Package 陶瓷平面接腳包裝型式

FAIRCHILD

Examples:

	(1)	(2)	(3)	(4)	(5)	(6)
F	74LS	125	A	D	C	
F	93S	10	D	C		

Note: In this book type description of FAIRCHILD TTL integrated circuit is as follows

(本書所記載之FAIRCHILD公司TTL積體電路係以下列方式表示)

Examples:

	(1)	(2)	(3)	(4)	(5)	(6)
F	C	74LS	125	A	D	
F	C	93S	10	D		

(1) F: Prefix of TTL (TTL之分類)

54S/74S Series Schottky TTL 蕭特基 TTL

54H/74H Series High-Speed TTL 高速 TTL

54/74 Series Standard TTL 標準 TTL

54F/74F Series Fairchild Advanced Schottky TTL (FAST)

9000 Series Medium Speed SSI 中速 SSI 93S00 Series Scottky MSI 蕭特基 MSI

9S00 Series Schottky SSI 蕭特基 SSI 9300 Series Standard MSI 標準 MSI

9H00 Series High-Speed SSI 高速 SSI 93L00 Series Low-Power MSI 低功率 MSI

9N00 Series Standard SSI 標準 SSI 9600 Series Monostable SSI 單穩態 SSI

9L00 Series Low-Power SSI 低功率 SSI 93400 Series Memory Elements 記憶元件

(3) Consecutive Numbers to indicate the Each Type

(表示各種類之一系列數字編號)

(4) Alphabet: Series Improved

(表示改良型之一系列英文字母)

(5) Package Type (包裝型式)

D: Ceramic Dual In-Line Package 陶瓷並行接腳時包裝型式

P: Plastic Dual In-Line Package 塑膠並行接腳時包裝型式

F: Ceramic Flat Package 陶瓷平面接腳包裝型式

(6) Operating Temperature Range (動作溫度範圍)

C: Commercial/Industrial 0℃ to + 70℃ (or 75℃)

M: Military: 55℃ to + 125℃

NATIONAL SEMICONDUCTOR

Examples:

	(1)	(2)	(3)	(4)	(5)	(6)
DM	74	LS	73	A	N	
DM	8	300	N			

(1) DM: Digital Monolithic TTL of NATIONAL SEMICONDUCTOR
(NS公司單晶數位TTL積體電路字首)

(2) Operating Temperature Range (動作溫度範圍)

54: 55℃ to + 125℃

74: 0℃ to + 70℃

9: 55℃ to + 125℃

8: 0℃ to + 70℃ (or 75℃)

(3) Classification of TTL (TTL之分類)

S: Schottky TTL 蕭特基 TTL

H: High-Speed TTL 高速 TTL

(BLANK): Standard TTL 標準 TTL

L: Low-Power TTL 低功率 TTL

ALS: Advanced Low-Power Schottky TTL

AS: Advanced Schottky TTL

(4) Consecutive Numbers to Indicate the Each Type

(表示各別種類之一連續數字編號)

(5) Alphabet: Series Improved

(表示改良型之一連續文字編號)

(6) Package Type (包裝型式)

J: Ceramic Dual In-Line Package 陶瓷並行接腳包裝型式

N: Plastic Dual In-Line Package 塑膠並行接腳包裝型式

F: Glass/Metal Flat Package 玻璃/金屬平面接腳包裝型式

W: Glass Hermetic Flat Package

NOMENCLATURE OF TTL INTEGRATED CIRCUITS

(數位TTL積體電路之命名法)

PHILIPS

Example: FJ (1) H (2) 13 (3) 1 (4)

(1) Digital Family Types of PHILIPS
- FJ : FJ Family FJ交換
- GJ : GJ Family GJ交換

(2) Circuit Function (電路功能)
- H : Combinational Circuit 組合邏輯電路
- J : Bistable or Multistable Sequential circuit 雙穩或多穩順序電路
- K : Monostable Sequential Circuit 單穩順序電路
- L : Level Converter 位準轉換電路
- Y : Miscellaneous 其他種類電路

(3) Consecutive Numbers to Indicate the Each Type
(表示各種類之一連續數字編號)

(4) Operating Temperature Range (動作溫度範圍)
- 1 : 0℃ to + 70℃ or Wider

(5) Classification of Package (包裝分類)
- 14 Lead Plastic Dual In-Line Package (Type A) 14腳塑膠並行接腳包裝型式(A類)
- 16 Lead Plastic Dual In-Line Package (Type B) 16腳塑膠並行接腳包裝型式(B類)
- 24 Lead Ceramic Dual In-Line Package 24腳陶瓷並行接腳包裝型式

SIEMENS

Example: FL (1) H (2) 29 (3) 1 (4) U (5)

(1) FL : TTL Digital Family of SIEMENS
(西門子公司TTL數位積體電路字首)

(2) Circuit Function (電路功能)
- H : Combinational Circuit 組合近輯電路
- J : Bistable or Multistable Sequential Circuit 雙穩或多穩順序電路
- K : Monostable Sequential Circuit 單穩順序電路
- L : Level Converter 位準轉換電路
- O : Read/Write Memory Circuit 讀/寫記憶電路
- Y : Miscellaneous Circuit 其他種類電路

(3) Consecutive Numbers to Indicate the Each Type
(表示各種類之一連續數字編號)

(4) Operating Temperature Ranhe (動作溫度範圍)
- 1 : 0℃ to + 70℃ or Wider

(5) Modeation (變形)
Package : Plastic Dual In-Line Package
包裝法：塑膠並行接腳包裝型式

SIGNETICS

Example: N (1) 74S (2) 161 (3) A (4) N (5)

1 Operating Temperature Range (動作溫度範圍)
- S : 55℃ to + 125℃ (Military Range) (軍用)
- N : 0℃ to 70℃ (Industrial Range) (工業用)

2 Classification of TTL (TTL之分類)
- 54S/74S Scottky TTL 蕭特基 TTL
- 54H/74H High-Speed TTL 高速 TTL
- 54/74 Standard TTL 標準 TTL
- 54F/74F FAST TTL

3 Consecutive Numbers to Indicate the Each Type
(表示各種類之一連續數字編號)

4 Alphabet Series Improved
(表示改良型之一系列英文字母)

5 Package Type (包裝型式)
- F : Ceramic Dual In-Line Package 陶瓷並行接腳包裝型式
- N : Plastic Dual In-Line Package 塑膠並行接腳包裝型式
- O : Ceramic Flat Package 24-Pin 24腳陶瓷平面接腳包裝型式
- W : Ceramic Flat Package 14-16Pin 14－16腳陶瓷平面接腳包裝型式

AMD

Example: Am (1) 74 (2) LS (3) 169 (4) A (5) P (6)

1 Am : Prefix of ADVANCE MICRO DEVICES

2 Operating Temperature Range (動作溫度範圍)
- 54 : 55℃ to + 125℃
- 74 : 0℃ to + 70℃

3 Classification of TTL (TTL之分類)
- LS : Low-Power schottky TTL
- S : Scottky TTL

4 Consecutive Numbers to Indicate the Each Type
(表示各種類之一連續數字編號)

5 Alphabet Series Improved
(表示改良型之一系列英文字母)

6 Package Type (包裝型式)
- D : Hermetic Dual In-Line Package
- P : Molded Dual-In-Line Package
- F : Flat Package
- X : Dice

NOMENCLATURE OF TTL INTEGRATED CIRCUITS

(數位TTL積體電路之命名法)

FUJITSU

Examples: MB (1) 74LS (2) 125 (3) A (4) M (5)

MB (1) 4 (2) 12 (3) M (5)

(1) MB: Abbreviation of FUJITSU Semiconductor Integrated Circuit "Micro Block" (富士通公司之半導體縮寫字首)

(2) Classification of TTL (TTL之分類)
- 74S : Scottky TTL 蕭特基 TTL
- 74LS : Low-Power Scottky TTL 低功率蕭特基 TTL
- 74ALS : Advanced Low-Power Scottky TTL
- 6 : High-Speed TTL 高速 TTL
- 4 : Standard TTL 標準 TTL

(3) Consecutive Numbers to Indicate the Each Type
(表示各種類別之連續數字編號)

(4) Alphabet : Series Improved

(5) Package Type and Operating Temperature Range
(包裝型式與動作溫度範圍)
(MB74S, MB74LS, MB74ALS Series)
- M : Plastic Dual In-Line Package −20℃ to +75℃ 塑膠並行接腳包裝型式
- C : Ceramic Dual In-Line Package −20℃ to +75℃ 陶瓷並行接腳包裝型式

(MB400, MB600 Series)
- M : Plastic Dual In-Line Package 0℃ to 70℃ 塑膠並行接腳包裝型式
- (BLANK) : Ceramic Dual In-Line Package 0℃ to 70℃ 陶瓷並行接腳包裝型式

MITSUBISHI

Examples: M (1) 74 (2) LS (3) 125 (4) A (5) P (6)

M (1) 5 (2) 32 (3) 90 (4) P (6)

(1) M : Standard Type of MITSUBISHI Molectron
(三菱公司標準型式字首)

(2) Operating Ambient Temperature Range (動作溫度範圍)
- 5 : Industrial/Commercial Use 0℃ to +75℃ (工業用/民生用)
- 74 : −20℃ to +75℃

(3) Classification of TTL (TTL之分類)
- 3 : Standard TTL, 44 : Standard TTL, S0 : Scottky TTL
- 32 : Standard TTL, 45 : Standard TTL, S1 : Scottky TTL
- 33 : Standard TTL, 46 : Standard TTL,
- 43 : Standard TTL, 47 : Standard TTL,
- LS : Low-Power Scottky TTL

(4) Consecutive Numbers to Indicate the Each Types
(表示各種類別之連續數字編號)

(5) Alphabet : Series Improved

(6) Package Type (包裝型式)
- P : Plastic Molded Dual In-Line Package
(塑膠並行接腳包裝型式)

HITACHI

Examples: HD (1) 74LS (2) 125 (3) A (4) P (5)

HD (1) 25 (2) 48 (3) P (5)

(1) HD : HITACHI Digital Integrated Circuits (日立公司數位積體電路字首)

(2) Classification of TTL and Operating Temperature Range
(TTL之分類及動作溫度範圍)
- 25 : TTL, −20℃ to +75℃
- 74 : TTL, −20℃ to +75℃
- 74S : SBC TTL, 0℃ to +70℃
- 74LS : Low-Power Scottky TTL, −20℃ to +75℃
- 74ALS : Advanced Low-Power Scottky TTL, −20℃ to +75℃

(3) Consecutive Numbers to Indicate the Each Type
(表示各別種類別之連續數字編號)

(4) Alphabet : Series Improved

(5) Package Type (包裝型式)
- P : Plastic Dual In-Line Package 塑膠並行接腳包裝型式
- (BLANK) : Ceramic Dual In-Line Package 陶瓷並行接腳包裝型式

NEC

Examples: μP (1) B (2) 2000 (3) D (4) μP (1) B (2) 2500 (3) D (4)

(1) μP NEC Semiconductor Integrated Circuit
(NEC公司半導體積體電路)

(2) Circuit Type (電路型式)
- B : Bipolar Digital Circuits (雙極數位電路)

(3) Consecutive Numbers to Indicate the Each Type
(表示各種類別之連續數字編號)

(4) Package Type and Operating Temperature Range
(包裝型式與動作溫度範圍)
- C : Plastic Dual In-Line Package 塑膠並行接腳包裝型式
- D : Ceramic Dual In-Line Package 陶瓷並行接腳包裝型式

μPB 200, μPB 2000 Series
- C : −15℃ to +75℃
- D : −25℃ to +75℃

μPB 25 Series
- D : 0℃ to +70℃

TOSHIBA

Examples: TD (1) 34 (2) 00 (3) A (4) P (5)

(1) TD : TOSHIBA Bipolar Digital Integrated Circuit
(東芝公司雙極數位積體電路字首)

(2) Classification Numbers to Indicate the Each Type
(電路型式之分類號碼)
- 34 : TTL
- 35 : TTL

(3) Consecutive Numbers to Indicate the Each Type
(表示各種類別之連續數字編號)

(4) Alphabet : Series Improved
(表示改良種類之文字記號)

(5) Package Type and Operating Temperature Range
(包裝型式與動作溫度範圍)
- P : Plastic Package −30℃ to +75℃