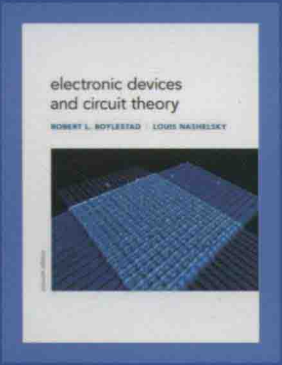
国外电子与通信教材系列

Pearson

精心改编

Electronic Devices and Circuit Theory

Eleventh Edition



electronic devices
and circuit theory
ROBERT L. BOYLESTAD | LOUIS NASHELSKY

模拟电子技术

（第二版）（英文版）

[美] Robert L. Boylestad
Louis Nashelsky 著

李立华 改编

中国工信出版集团

電子工業出版社
PUBLISHING HOUSE OF ELECTRONICS INDUSTRY
http://www.phei.com.cn

国外电子与通信教材系列

模拟电子技术

（第二版）（英文版）

Electronic Devices and Circuit Theory

Eleventh Edition

［美］ Robert L. Boylestad
Louis Nashelsky 著

李立华 改编

電子工業出版社
Publishing House of Electronics Industry
北京 • BEIJING

内容简介

本书包括半导体器件基础、二极管及其应用电路、晶体管和场效应管放大电路的基本原理及频率响应、功率放大电路、多级放大电路、差分放大电路、电流源等模拟集成电路的单元电路、反馈电路、模拟集成运算放大器、电压比较器和波形变换电路等。本书结合国内高等教育中采用英语或双语教学的特点和实际情况，对原版教材进行了改编，精简了内容，突出了重点，补充了必要知识点，内容更加新颖和系统化，反映了器件和应用的发展趋势，强调了系统工程的概念。

本书适合作为电子、计算机、通信等相关专业电子电路基础课程40学时到68学时的英语或双语教学教材。

图书在版编目（CIP）数据

模拟电子技术：第十一版=Electronic Devices and Circuit Theory, Eleventh Edition：英文/（美）罗伯特·L. 博伊斯坦（Robert L. Boylestad），（美）路易斯·纳什斯凯（Louis Nashelsky）著；李立华改编. —2版.
北京：电子工业出版社，2016.7
国外电子与通信教材系列
ISBN 978-7-121-28915-6

Ⅰ. ①模… Ⅱ. ①罗… ②路… ③李… Ⅲ. ①模拟电路－电子技术－高等学校－教材－英文 Ⅳ. ①TN710

中国版本图书馆CIP数据核字（2016）第111540号

策划编辑：马　岚
责任编辑：马　岚
印　　刷：三河市良远印务有限公司
装　　订：三河市良远印务有限公司
出版发行：电子工业出版社
　　　　　北京市海淀区万寿路173信箱　邮编：100036
开　　本：787×1092　1/16　印张：38　字数：1265千字
版　　次：2007年9月第1版（原著第9版）
　　　　　2016年7月第2版（原著第11版）
印　　次：2016年7月第1次印刷
定　　价：89.00元

凡所购买电子工业出版社图书有缺损问题，请向购买书店调换。若书店售缺，请与本社发行部联系，联系及邮购电话：（010）88254888，88258888。

质量投诉请发邮件至zlts@phei.com.cn，盗版侵权举报请发邮件至dbqq@phei.com.cn。

本书咨询联系方式：classic-series-info@phei.com.cn。

导　读

当您拿起这本书的时候一定会感到非常厚重，不过请不要担心，这是由于本书中有大量的例题和详尽的解释所致，而这也是本书的特色和非常适合作为电子电路基础入门教材的原因。下面让我们一起开启电子电路基础的入门之旅，直到您完成这本书的学习，奠定自己在电子电路领域的知识基础，掌握开启电子工程、信息与通信工程专业相关专业知识学习的钥匙。

现代几乎所有电子系统的构成基础都是半导体材料，因此首先了解一些半导体材料的基本知识，对于理解半导体元器件的工作原理很有帮助。这些知识包括原子结构、本征半导体、掺杂半导体、载流子（一种能够携带电荷的粒子）、PN结等。这部分是微电子知识，如果只关注半导体器件的使用以及外围电路的分析设计，也可以忽略这部分内容（1.1节至1.5节）。本书第1章至第8章主要讨论三种半导体电子器件及其单元电路：二极管、双极性结型晶体管（BJT）和场效应管（FET）。

二极管

二极管的内部核心是PN结，1.6节至1.14节介绍了二极管的基本工作原理及其等效电路模型，包括基本二极管和几种特殊二极管，例如齐纳二极管和发光二极管等。而二极管的应用电路在第2章详细阐述，并有丰富的例题分析，包括半波整流电路、全波整流电路、削波电路、钳位电路、利用齐纳二极管的稳幅电路等。在分析方法上，第2章介绍了负载线分析方法和等效模型分析方法。如果您的学习重点是晶体管放大器，而不是二极管，那么第1章和第2章可以作为了解和自学内容。但是需要注意，PN结也是晶体管的构成基础，因此若要研究晶体管构成并深入了解其工作原理，也需要首先掌握PN结工作原理。

双极性结型晶体管（BJT）

双极性结型晶体管是一种广泛使用的基本晶体管，第3章主要描述其内部结构、类型及3种基本组态的运用。晶体管内部结构特点及工作机理导致了其外在特性具有放大电压或者放大电流的能力，但是如果只关心晶体管的应用，也可以忽略晶体管的内部结构和微电子工作机理。晶体管的应用主要从学习3种基本组态出发，掌握各种组态的特点以及晶体管的工作区。晶体管是一种有源器件，需要设置直流工作点才能正常工作（例如，放大交流信号时，晶体管需要通过设计直流工作点使其工作在线性放大区，才能无失真地放大交流小信号）。因此，当初学者开始学习由单个晶体管构成的基本放大电路时，需要从两个方面入手。一方面是晶体管的直流偏置电路，目的是设置合适的直流工作点，使其工作在合适的工作区（详细分析见第4章）；另一方面是晶体管

交流小信号放大电路，目的是分析晶体管放大输入交流小信号的能力，例如增益、输入/输出特性等（见第5章）。值得说明的是，晶体管对于直流和交流的响应是不同的，因此第4章主要分析直流偏置电路，需要首先画出原电路的直流等效电路，再进行分析；而第5章主要分析交流小信号放大电路，需要首先画出原电路的交流等效电路再进行分析。同时，虽然晶体管是非线性器件，分析非常困难，但是当输入为交流小信号时，其变化范围很小，晶体管的非线性特性可以等效为线性特性，因此晶体管可以用其小信号微变等效模型来替代，这样获得的等效电路可以采用基本的电路分析方法进行分析，例如基尔霍夫定律等。通过学习第4章和第5章，读者将掌握单个BJT构成的基本放大电路的工作原理和性能分析。

场效应晶体管（FET）

场效应晶体管由于具有稳定性佳等优势，正逐渐取代BJT而被人们广泛应用。FET有多种类型，掌握其结构和不同类型FET的特点，例如输入特性、输出特性和转移特性，就成为学习FET的首要内容（见第6章）。建议采用与BJT相对比的方法学习FET。作为晶体管的一种，FET和BJT一样主要用于放大小信号，也是一种非线性有源器件，需要设置直流工作点，使其工作在饱和区（BJT是工作在线性放大区），才能无失真地放大交流小信号。同样，需要首先学习FET的直流偏置电路（见第7章），然后需要用小信号微变等效模型方法分析其对交流小信号的放大特性（见第8章）。但是FET从内部结构、工作区、转移特性、3种基本组态、直流偏置电路、小信号微变等效模型等方面与BJT都是不同的。通过学习第7章和第8章，读者将掌握单个FET构成的基本放大电路的工作原理和性能分析。

复杂电路和特性

通过对第1章至第8章的学习，恭喜您入门了，掌握了二极管和晶体管的基本器件知识，学会了分析基本单管放大电路，掌握了画图法、负载线分析法及等效电路分析方法。下一步，读者将进入更复杂电路和特性的学习。首先，通过学习第9章的内容，认识到晶体管（无论是BJT还是FET）对不同频率的输入信号有不同的响应，通过学习其频率响应特性加深对晶体管放大电路的认识，学会分析其频率响应以及扩展带宽的方法。这部分一般属于难点知识，重点在于对晶体管放大电路频率响应概念的理解，例如带宽、截止频率等，定量分析是比较困难的。在掌握了单个晶体管放大电路的基础上，第10章介绍多级放大电路和差分放大电路，这些单元电路是构成集成电路的基础。其中，差分放大电路的分析既是重点也是教学中的难点。同时，第10章以集成运算放大器为例介绍集成电路知识，包括其内部结构和外部特性等。运算放大器的应用电路见第11章，运算放大器的线性运用包括有源滤波器和运算单元，非线性运用包括比较器和施密特触发器。

本书讲解晶体管放大器主要是以放大交流小信号为主，分析方法以小信号微变等效模型分析方法为主，但是第12章则不同，主要介绍基于大信号的功率放大器，因此小信号微变等效模型分

析方法在此就不能使用了。这一章主要以大信号分析为主，学习功率的计算，掌握不同类型功率放大器电路的特征和分析方法。

电路在实际应用中可能存在很多问题，例如工作点不稳定而发生漂移，输出电压不稳定等等，因此改善电路性能是至关重要的，在放大电路中引入负反馈就是改善电路性能的一种重要方法，在第13章中进行阐述。在了解反馈的构成基础上，需要掌握瞬时极性法来分析反馈的类型。不同类型的反馈作用是不同的，正反馈产生自激，负反馈具有稳定电路的作用，此章主要讲述负反馈放大电路及其分析方法。负反馈有4种类型，对电路进行分析并判断是否存在反馈以及存在何种反馈是一项重要的技能。通过为放大电路引入深度负反馈来改善电路性能，例如阻抗特性、输出特性等，是电路分析和设计的重要内容。值得注意的是，当电路中引入了深度负反馈时，宜采用工程近似估算方法，而非小信号微变等效模型分析方法。

至此，通过本书的学习，读者已经掌握了电子电路的基本知识、理论和分析方法，为从事相关电路分析和设计工作以及相关专业的后续课程学习打下了扎实的基础。回顾本书的知识结构和章节构成，不难看出本书主要以半导体器件晶体管为主，以基本晶体管放大电路为基础和重点，以差分放大电路、多级放大电路、负反馈放大电路、集成运算放大电路为桥梁，逐步深入地展开电子电路基础原理和应用电路分析，同时贯穿了多种电路分析方法：画图法、小信号分析方法、大信号功率计算方法、工程近似分析方法等。值得注意的是，在学习中要勤于画各种等效电路，逐步简化电路和分析，灵活运用工程近似。

在北京邮电大学国际学院的“电子电路基础”课程中，我们采用了本书作为教材。通过几年的教学反馈，笔者深有体会，书中丰富的例题和详细的讲解，对于初学者的理解和自主学习都大有裨益。采用本书作为教材的授课教师，可联系te_service@phei.com.cn获取教学用PPT等相关资料。

Preface

The preparation of the preface for the 11th edition resulted in a bit of reflection on the 40 years since the first edition was published in 1972 by two young educators eager to test their ability to improve on the available literature on electronic devices. Although one may prefer the term semiconductor devices rather than electronic devices, the first edition was almost exclusively a survey of vacuum-tube devices—a subject without a single section in the new Table of Contents. The change from tubes to predominantly semiconductor devices took almost five editions, but today it is simply referenced in some sections. It is interesting, however, that when field-effect transistor (FET) devices surfaced in earnest, a number of the analysis techniques used for tubes could be applied because of the similarities in the ac equivalent models of each device.

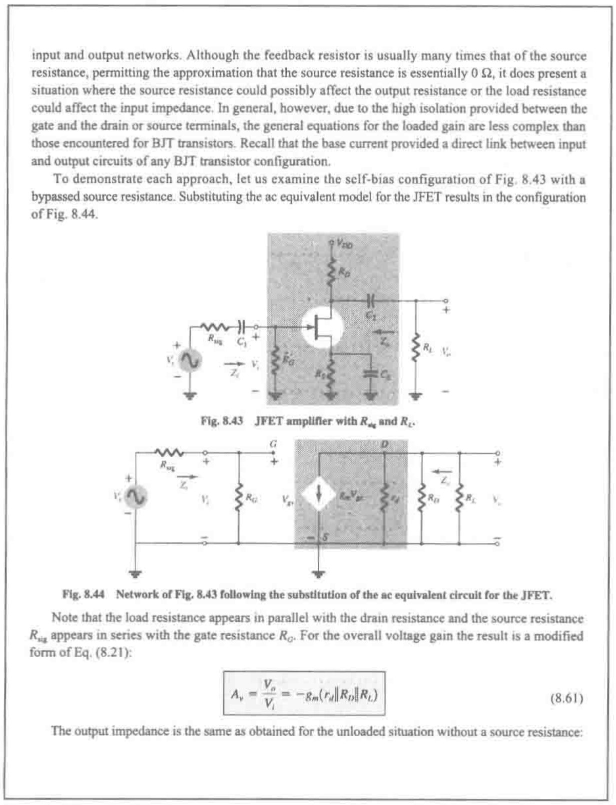
We are often asked about the revision process and how the content of a new edition is defined. In some cases, it is quite obvious that the computer software has been updated, and the changes in application of the packages must be spelled out in detail. This text was the first to emphasize the use of computer software packages and provided a level of detail unavailable in other texts. With each new version of a software package, we have found that the supporting literature may still be in production, or the manuals lack the detail for new users of these packages. Sufficient detail in this text ensures that a student can apply each of the software packages covered without additional instructional material. (Note: To meet the requirement of general Chinese teaching syllabus on electronic circuits, the contents about some software have been deleted.)

The next requirement with any new edition is the need to update the content reflecting changes in the available devices and in the characteristics of commercial devices. This can require extensive research in each area, followed by decisions regarding depth of coverage and whether the listed improvements in response are valid and deserve recognition. The classroom experience is probably one of the most important resources for defining areas that need expansion, deletion, or revision. The feedback from students results in marked-up copies of our texts with inserts creating a mushrooming copy of the material. Next, there is the input from our peers, faculty at other institutions using the text, and, of course, reviewers chosen by Pearson Education to review the text. One source of change that is less obvious is a simple rereading of the material following the passing of the years since the last edition. Rereading often reveals material that can be improved, deleted, or expanded.

For this revision, the number of changes far outweighs our original expectations. However, for someone who has used previous editions of the text, the changes will probably be less obvious. However, major sections have been moved and expanded, some 100-plus problems have been added, new devices have been introduced, the number of applications has been increased, and new material on recent developments has been added throughout the text. We believe that the current edition is a significant improvement over the previous editions.

As instructors, we are all well aware of the importance of a high level of accuracy required for a text of this kind. There is nothing more frustrating for a student than to work a problem over from many different angles and still find that the answer differs from the solution at the back of the text or that the problem seems undoable. We were pleased to find that there were fewer than half a dozen errors or misprints reported since the last edition. When you consider the number of examples and problems in the text along with the length of the text material, this statistic clearly suggests that the text is as error-free as possible. Any contributions from users to this list were quickly acknowledged, and the sources were thanked for taking the time to send the changes to the publisher and to us.

Although the current edition now reflects all the changes we feel it should have, we expect that a revised edition will be required somewhere down the line. We invite you to respond to this edition so that we can start developing a package of ideas and thoughts that will help us improve the content for the next edition. We promise a quick response to your comments, whether positive or negative.



input and output networks. Although the feedback resistor is usually many times that of the source resistance, permitting the approximation that the source resistance is essentially 0 Ω, it does present a situation where the source resistance could possibly affect the output resistance or the load resistance could affect the input impedance. In general, however, due to the high isolation provided between the gate and the drain or source terminals, the general equations for the loaded gain are less complex than those encountered for BJT transistors. Recall that the base current provided a direct link between input and output circuits of any BJT transistor configuration.

To demonstrate each approach, let us examine the self-bias configuration of Fig. 8.43 with a bypassed source resistance. Substituting the ac equivalent model for the JFET results in the configuration of Fig. 8.44.

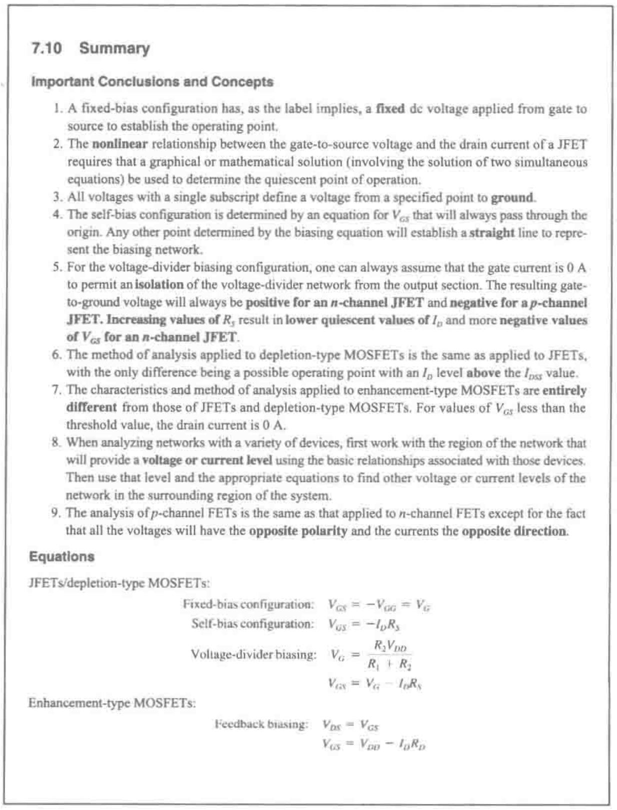
Fig. 8.43 JFET amplifier with R_{sig} and R_L.

Fig. 8.44 Network of Fig. 8.43 following the substitution of the ac equivalent circuit for the JFET.

Note that the load resistance appears in parallel with the drain resistance and the source resistance R_{sig} appears in series with the gate resistance R_G. For the overall voltage gain the result is a modified form of Eq. (8.21):

$$\boxed{A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D \| R_L)} \qquad (8.61)$$

The output impedance is the same as obtained for the unloaded situation without a source resistance:



7.10 Summary

Important Conclusions and Concepts

1. A fixed-bias configuration has, as the label implies, a **fixed** dc voltage applied from gate to source to establish the operating point.
2. The **nonlinear** relationship between the gate-to-source voltage and the drain current of a JFET requires that a graphical or mathematical solution (involving the solution of two simultaneous equations) be used to determine the quiescent point of operation.
3. All voltages with a single subscript define a voltage from a specified point to **ground**.
4. The self-bias configuration is determined by an equation for V_{GS} that will always pass through the origin. Any other point determined by the biasing equation will establish a **straight** line to represent the biasing network.
5. For the voltage-divider biasing configuration, one can always assume that the gate current is 0 A to permit an **isolation** of the voltage-divider network from the output section. The resulting gate-to-ground voltage will always be **positive for an *n*-channel JFET** and **negative for a *p*-channel JFET. Increasing values of R_S** result in **lower quiescent values of I_D** and more **negative values of V_{GS} for an *n*-channel JFET**.
6. The method of analysis applied to depletion-type MOSFETs is the same as applied to JFETs, with the only difference being a possible operating point with an I_D level **above** the I_{DSS} value.
7. The characteristics and method of analysis applied to enhancement-type MOSFETs are **entirely different** from those of JFETs and depletion-type MOSFETs. For values of V_{GS} less than the threshold value, the drain current is 0 A.
8. When analyzing networks with a variety of devices, first work with the region of the network that will provide a **voltage or current level** using the basic relationships associated with those devices. Then use that level and the appropriate equations to find other voltage or current levels of the network in the surrounding region of the system.
9. The analysis of *p*-channel FETs is the same as that applied to *n*-channel FETs except for the fact that all the voltages will have the **opposite polarity** and the currents the **opposite direction**.

Equations

JFETs/depletion-type MOSFETs:

Fixed-bias configuration: $V_{GS} = -V_{GG} = V_G$

Self-bias configuration: $V_{GS} = -I_D R_S$

Voltage-divider biasing: $V_G = \dfrac{R_2 V_{DD}}{R_1 + R_2}$

$V_{GS} = V_G - I_D R_S$

Enhancement-type MOSFETs:

Feedback biasing: $V_{DS} = V_{GS}$

$V_{GS} = V_{DD} - I_D R_D$

Contents

Chapter 1

Semiconductor Diodes

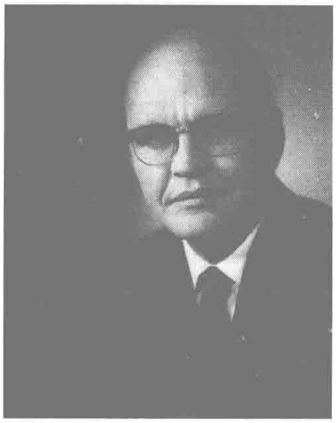
Chapter Outline

1.1 Introduction

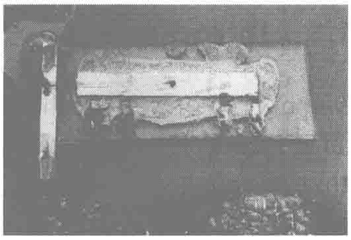
One of the noteworthy things about this field, as in many other areas of technology, is how little the fundamental principles change over time. Systems are incredibly smaller, current speeds of operation are truly remarkable, and new gadgets surface every day, leaving us to wonder where technology is taking us. However, if we take a moment to consider that the majority of all the devices in use were invented decades ago and that design techniques appearing in texts as far back as the 1930s are still in use, we realize that most of what we see is primarily a steady improvement in construction techniques and application of those devices rather than the development of new elements and fundamentally new designs. The result is that most of the devices discussed in this text have been around for some time, and that texts on the subject written a decade ago are still good references with content that has not changed very much. The major changes have been in the understanding of how these devices work and their full range of capabilities, and in improved methods of teaching the fundamentals associated with them. The benefit of all this to the new student of the subject is that the material in this text will, we hope, have reached a level where it is relatively easy to grasp and the information will have application for years to come.

The miniaturization that has occurred in recent years leaves us to wonder about its limits. Complete systems now appear on wafers thousands of times smaller than the single element of earlier networks. The first integrated circuit (IC) was developed by Jack Kilby while working at Texas Instruments in 1958 (Fig. 1.1). Today, the Intel® Pentium® 4 processor shown in Fig. 1.2 has more than 42 million transistors and a host of other components. Recent advances suggest that 1 billion transistors will soon be placed on a sliver of silicon smaller than a fingernail. We have obviously reached a point where the primary purpose of the container is simply to provide some means for handling the device or system and to provide a mechanism for attachment to the remainder of the network. Further miniaturization appears to be limited by three factors: the quality of the semiconductor material, the network design technique, and the limits of the manufacturing and processing equipment.

The first device to be introduced here is the simplest of all electronic devices, yet has a range of applications that seems endless. We devote two chapters to the device to introduce the materials commonly used in solid-state devices and review some fundamental laws of electric circuits.



Jack St. Clair Kilby, inventor of the integrated circuit and co-inventor of the electronic handheld calculator. (Courtesy of Texas Instruments.) Born: Jefferson City, Missouri, 1923. MS, University of Wisconsin. Director of Engineering and Technology, Components Group, Texas Instruments. Fellow of the IEEE. Holds more than 60 U.S. patents.



The first integrated circuit, a phaseshift oscillator, invented by Jack St. Kilby in 1958. (Courtesy of Texas Instruments.)

Fig. 1.1 Jack St. Clair Kilby.

1.2 Semiconductor Materials: Ge, Si, and GaAs

The construction of every discrete (individual) solid-state (hard crystal structure) electronic device or integrated circuit begins with a semiconductor material of the highest quality.

Semiconductors are a special class of elements having a conductivity between that of a good conductor and that of an insulator.

In general, semiconductor materials fall into one of two classes: *single-crystal* and *compound*. Single-crystal semiconductors such as germanium (Ge) and silicon (Si) have a repetitive crystal structure, whereas compound semiconductors such as gallium arsenide (GaAs), cadmium sulfide (CdS), gallium nitride (GaN), and gallium arsenide phosphide (GaAsP) are constructed of two or more semiconductor materials of different atomic structures.

The three semiconductors used most frequently in the construction of electronic devices are Ge, Si, and GaAs.

In the first few decades following the discovery of the diode in 1939 and the transistor in 1947 germanium was used almost exclusively because it was relatively easy to find and was available in fairly large quantities. It was also relatively easy to refine to obtain very high levels of purity, an important aspect in the fabrication process. However, it was discovered in the early years that diodes and transistors constructed using germanium as the base material suffered from low levels of reliability due primarily to its sensitivity to changes in temperature. At the time, scientists were aware that another material, silicon, had improved temperature sensitivities, but the refining process for manufacturing silicon of very high levels of purity was still in the development stages. Finally, however, in 1954 the first silicon transistor was introduced, and silicon quickly became the semiconductor material of choice. Not only is silicon less temperature sensitive, but it

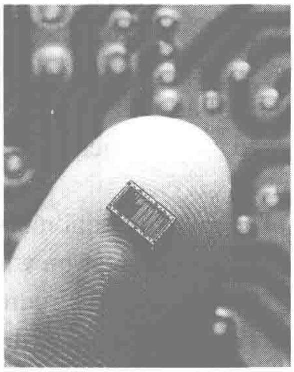


Fig. 1.2 Computer chip. (© Stock Photo/CORBIS.)

is one of the most abundant materials on earth, removing any concerns about availability. The flood gates now opened to this new material, and the manufacturing and design technology improved steadily through the following years to the current high level of sophistication.

As time moved on, however, the field of electronics became increasingly sensitive to issues of speed. Computers were operating at higher and higher speeds, and communication systems were operating at higher levels of performance. A semiconductor material capable of meeting these new needs had to be found. The result was the development of the first GaAs transistor in the early 1970s. This new transistor had speeds of operation up to five times that of Si. The problem, however, was that because of the years of intense design efforts and manufacturing improvements using Si, Si transistor networks for most applications were cheaper to manufacture and had the advantage of highly efficient design strategies. GaAs was more difficult to manufacture at high levels of purity, was more expensive, and had little design support in the early years of development. However, in time the demand for increased speed resulted in more funding for GaAs research, to the point that today it is consistently used as the base material for new high-speed, very large scale integrated (VLSI) circuit designs.

This brief review of the history of semiconductor materials is not meant to imply that GaAs will soon be the only material appropriate for solid-state construction. Germanium devices are still being manufactured, although for a limited range of applications. Even though it is a temperature-sensitive semiconductor, it does have characteristics that find application in a limited number of areas. Given its availability and low manufacturing costs, it will continue to find its place in product catalogs. As noted earlier, Si has the benefit of years of development, and is the leading semiconductor material for electronic components and ICs. GaAs is more expensive, but as manufacturing processes improve and demands for higher speeds increase, it will begin to challenge Si as the dominant semiconductor material.

1.3 Covalent Bonding and Intrinsic Materials

To fully appreciate why Si, Ge, and GaAs are the semiconductors of choice for the electronics industry requires some understanding of the atomic structure of each and how the atoms are bound together to form a crystalline structure. Every atom is composed of three basic particles: the electron, the proton, and the neutron. In the lattice structure, neutrons and protons form the nucleus and electrons appear in fixed orbits around the nucleus. The Bohr model for the three materials is provided in Fig. 1.3.

As indicated in Fig. 1.3, silicon has 14 orbiting electrons, germanium has 32 electrons, gallium has 31 electrons, and arsenic has 33 orbiting electrons (the same arsenic that is a very poisonous chemical agent). For germanium and silicon there are four electrons in the outermost shell, which are referred to as *valence electrons.* Gallium has three valence electrons and arsenic has five valence electrons. Atoms that have four valence electrons are called *tetravalent*, those with three are called *trivalent*, and those with five are called *pentavalent*. The term *valence* is used to indicate that the potential (ionization potential) required to remove any one of these electrons from the atomic structure is significantly lower than that required for any other electron in the structure.

In a pure silicon or germanium crystal the four valence electrons of one atom form a bonding arrangement with four adjoining atoms, as shown in Fig. 1.4.

This bonding of atoms, strengthened by the sharing of electrons, is called covalent bonding.

Because GaAs is a compound semiconductor, there is sharing between the two different atoms, as shown in Fig. 1.5. Each atom is surrounded by atoms of the complementary type. There is still a sharing of electrons similar in structure to that of Ge and Si, but now five electrons are provided by the As atom and three by the Ga atom.

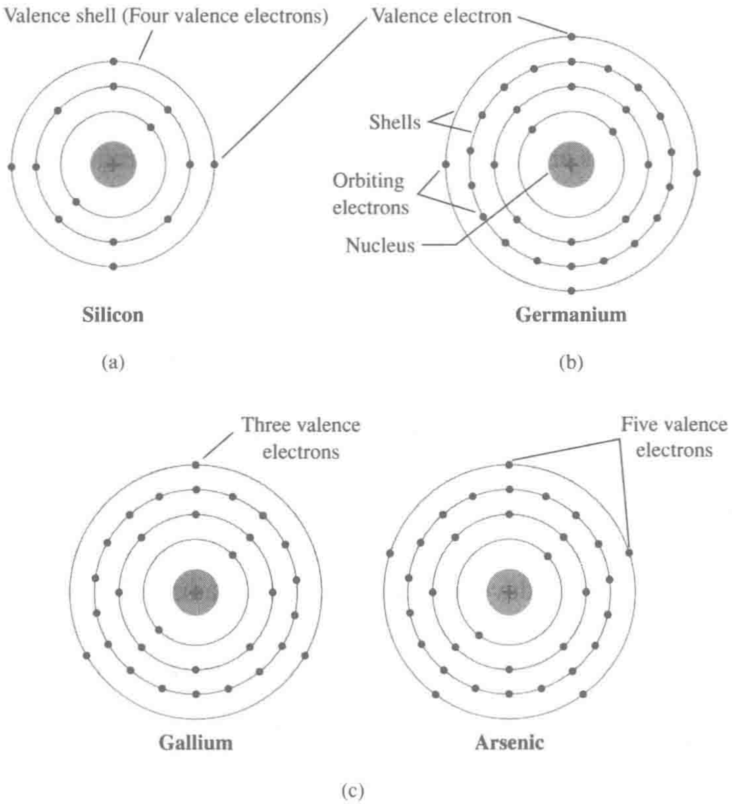


Fig. 1.3 Atomic structure of (a) silicon; (b) germanium; and (c) gallium and arsenic.

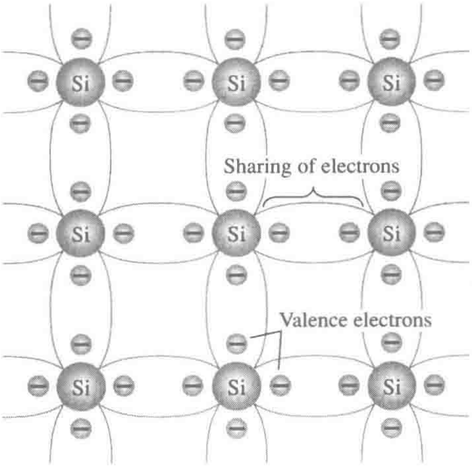


Fig. 1.4 Covalent bonding of the silicon atom.

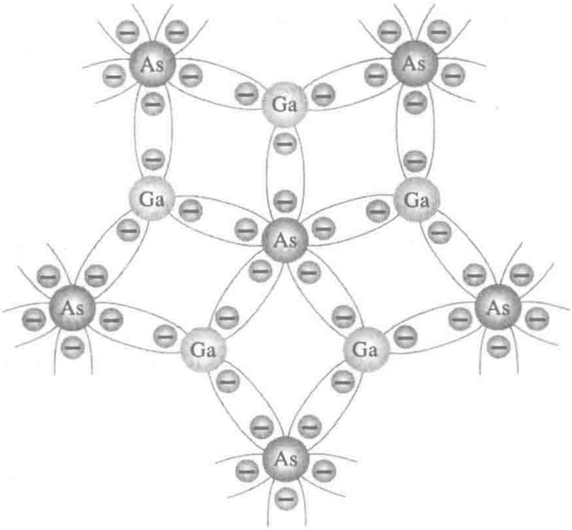


Fig. 1.5 Covalent bonding of the GaAs crystal.