CHARGE PUMP IC DESIGN

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About the Author

Feng Pan received his BS degree in EECS from the University of California, Berkeley, and MS in Electrical Engineering from Stanford University. He is a Stanford Certified Program Manager (SCPM), and is currently working as a director of NSG at Micron Technology, Inc. on 3D VNAND technology. Mr. Pan previously held various senior management and leadership positions at SanDisk and AMD. Mr. Pan is coauthor of *Charge Pump Circuit Design*, and has 51 granted patents related to power management, LDO, charge pump architectures, charge pump regulations and applications, ADC design, op-amp designs, and NAND/NOR flash memory designs.

Preface

Over the last decade or so, the portable devices, hand-held devices, smart phones, SSDs, etc., have proliferated in our daily lives. Power management and power harvesting have become important research themes in analog designs to reduce power consumption and to use alternative and renewable energy sources instead of traditional fossil fuels. The current power management has branched off to become an emerging field of its own in analog design. For on-chip DC–DC converter, like charge pump, there have been a lot of new studies and researches since *Charge Pump Circuit Design* was first published in 2006. It is the time to reflect and have a new book to systematically discuss the theories, practical designs, and applications on charge pump from real practices to emphasize on performance, power efficiency, and area efficiency.

Charge Pump IC Design has the following key focuses to make it an advanced reference book for power management design professionals.

First, it introduces and compares the various power management and power conditioning circuits at system level and at chip level. It gives a systematic approach to derive the charge pump characteristics.

Second, it discusses a systematic approach on how to design charge pump from a new perspective, with the local optimization on basic charge pump stage, which leads to the optimum final design.

Third, it discusses various design approaches to address charge pump-related circuits and regulation schemes with key emphasis on performance power and area efficiency using real design examples. This allows readers to see practical approaches and trade-offs in actual design.

Fourth, it explains in details the negative feedback control and compensation in charge pump stability analysis with practical examples.

Fifth, it introduces the new concepts of using charge pump to design current-based ADC (analog-to-digital converter). This leads to brand new approaches for signal processing, power management control, etc.

This book is based upon many years of research works in charge pump and power management design in practice. It can be served as a reference book for analog and power management IC design engineers in industry, or graduate students in the fields of power management, power harvesting, or power electronics IC designs.

Feng Pan

Acknowledgments

Since publishing *Charge Pump Circuit Design* in 2006, it is now the right time to reflect and consolidate all the thoughts in a new book from the continuous learning and practicing of analog design in power management. This is a one-and-half-year project spanning many weekends and nights in San Francisco and Fremont while accompanying my daughter to go through her talent training. It is such a magical feeling to see her growth and improvement while I am able to wrap up this book at the same time with her graduation from the training.

This book has benefited from the works and studies of doing NAND flash memory design at SanDisk. The practices of circuit design, layout, and silicon debugging have helped me to grow more confident in analog design. Many thanks go to my colleagues at SanDisk for their fruitful discussions on various analog design topics. I also thank many of my colleagues at Micron for suggesting that I write this book. I am particularly grateful to Ramin Ghodsi's support from Micron management in writing this book.

My wife, Danae Deng, has encouraged me in the last sixteen years to set higher goals and to take on greater challenges in my life. She helps me to grow in many areas. I would not have been able to write this book without her full support. My beautiful daughter, Tiffany Pan, was born in 2006 when my first book was published. She has been a treasure to me and brings a lot of happiness to my life. It is with her encouragement that I am able to complete this project in time. She told me that she wants to write a book by herself someday like her dad. I am grateful to my parents Nianen Wang, Baohua Pan, and my brother Dean Pan for all their advice and support in my life.

The timely production of this book was made possible by the hard work of the staff at McGraw-Hill, especially, Donna M. Martone, Lynn M. Messina, Molly T. Wyand, and Jeff Weeks. I would like to thank Cenveo Publisher Services, particularly Tanya Punj and her team for their figure, proofreading (Eina Malik), grammar suggestions (Patti Scott), and indexing (Edwin Durbin). I am also pleased to express my gratitude to Mike McCabe at McGraw-Hill for initiating this project and helping me in many ways to complete this book.

I learned analog design from Stanford University and U.C. Berkeley. I want to express my gratitude to my schools and professors here.

Feng Pan
January 2015

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CHAPTER 1

Regulators and Power Converters

In the semiconductor field, at either the system level or the chip level, the available power supplies given may not be suitable to meet all the power specifications of the loading chips or the loading circuits. The needs for power conversion between supplies or power supply conditioning may arise from one or more of the following design requirements: converting power between AC power supply and DC power supply, inverting the polarity of the power supply from the available power supply, modifying the magnitude of the power supply, improving the power efficiency of the power conversion or power conditioning circuits or reducing the output noise seen by loads from the given power supply. In general, the achievement of both high power efficiency and low output supply noise is the most challenging design goal in power converter or power conditioning design. With a single design solution it is difficult to achieve both design goals at the same time. Several designs solutions at different levels of integration are required to work together to achieve the highest power efficiency and lowest output supply noise in the overall system.

Based upon the location or the purpose of the solution, power circuit designs could be sorted into three main categories: (1) linear regulator, (2) switch mode power supply (SMPS), and (3) charge pump. A combination of SMPS and a low dropout (LDO), a combination of SMPS and a charge pump, or some other forms of combinations are common in today's overall system design. Each serves an important role in many electronic systems to ensure the overall power supply integrity of designs and power efficiency of the system as a whole.

1.1 Linear Regulator

A linear regulator is used in an electronic system to maintain a clean and steady power supply to the load. Despite variations or noises from the input power supply, or the faster switching nature of the

loadings, a linear regulator should be able to (1) reject or filter noises from either the input supply or loadings and (2) maintain the target regulation within design specifications under all conditions. Several configurations of linear regulators are commonly used by designers. The high dropout (HDO) regulator and low dropout (LDO) regulator are two of the most popular architectures that could be found in many integrated circuits (ICs) and systems. Given the demands for higher power efficiency and higher power integrity with the proliferation of handheld devices storage and processing requirements in the cloud, the LDO regulator has gained significant popularity in recent years and has been spun off into a separate branch of study of its own, as have many other analog systems, such as data converter design and high-speed I/O design.

1.1.1 Input Power Supply Noise Rejection

Figure 1.1 illustrates the waveforms of the input power supply noise rejection of an ideal linear regulator with constant current load. With constant current load, for an ideal linear regulator with infinite bandwidth and gain, the regulator should be able to reject input supply noises from V_{cc} at any magnitude and at any frequency. The output supply V_{sup} would be regulated at the target value regardless of how the input supply V_{cc} varies.

Line regulation (LNR)[1-3] is an important DC performance parameter of the linear regulator. It refers to how much the output voltage changes with respect to the input power supply DC change. The input supply is at DC. It is equivalent to the DC gain

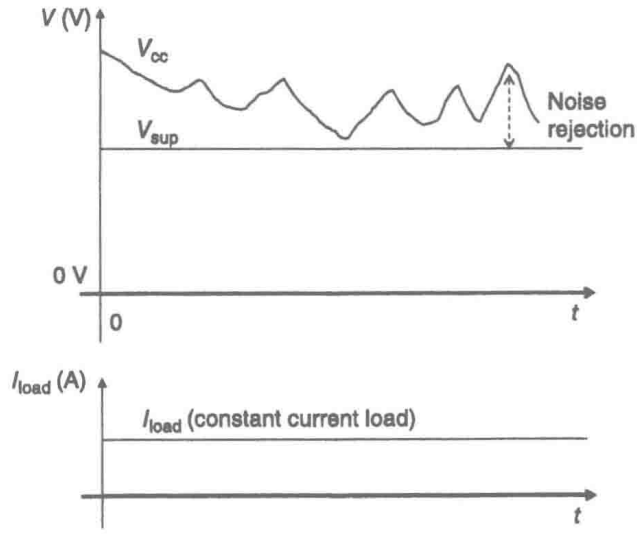

Figure 1.1 Input power supply noise rejection of ideal linear regulator with constant current load.

from the input power supply V_{cc} to the output power supply V_{sup}, as in Eq. (1.1).

$$\text{LNR} = A_v(s=0) = \frac{\Delta V_{sup}}{\Delta V_{cc}} \tag{1.1}$$

$$\text{PSR} \approx \frac{1}{A_v(s)} = \frac{\Delta V_{cc}(s)}{\Delta V_{sup}(s)} \tag{1.2}$$

The power supply rejection (PSR)[2] or ripple rejection, on the other hand, is the parameter used to measure the output supply rejection to the input supply variation over the entire frequency spectrum, as defined in Eq. (1.2). With limited bandwidth, linear regulator would not be able to reject input supply noise exceeds its closed-loop bandwidth. The input supply noise that exceeds the closed-loop bandwidth must be filtered out by the decoupling capacitance on the output. If input supply disturb causes a large signal excursion, regulator would not be able to response to hold the design specification. With increased bandwidth of circuits or added larger decoupling capacitance could address the issue.

1.1.2 Load Noise Rejection

Figure 1.2 illustrates the waveforms of the load noise rejection of the ideal linear regulator with constant input supply. With the input power supply V_{cc} unchanged, regardless of how the current load I_{load} switches, the ideal regulator with infinite bandwidth and gain should respond instantaneously to the change of load current with any

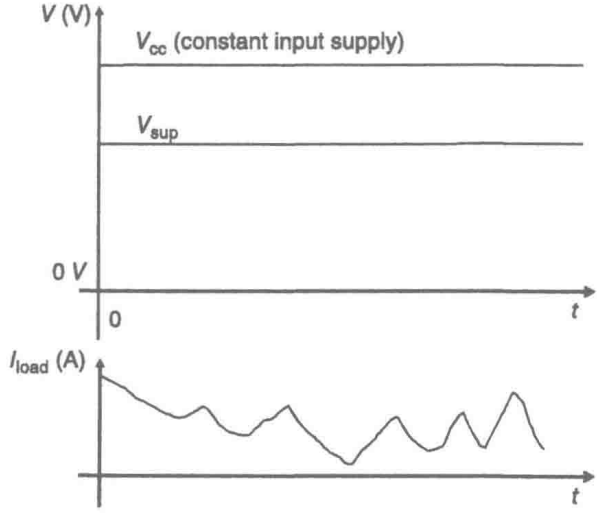

Figure 1.2 Load noise rejection of ideal linear regulator with constant input supply.

frequency and with any magnitude, and still be able to maintain the target output regulation voltage within design specifications.

Load regulation (LDR)[2] is an important DC performance parameter of a linear regulator. It refers to how much the output supply V_{sup} changes with respect to the change in load current I_{load}. The load current is DC. Load regulation is equivalent to the output impedance of the regulator at DC, as shown in Eq. (1.3).

$$\text{LDR} = Z_{out}(s=0) = \frac{\Delta V_{sup}}{\Delta I_{load}} \tag{1.3}$$

With limited bandwidth and gain of circuits, the linear regulator would not be able to reject load noise that exceeds its closed-loop bandwidth. The noise of the closed-loop bandwidth must be filtered out by the decoupling capacitance on the output. In a similar argument, if the load dump disturbance causes a very large signal excursion in the output of the regulator, the regulator may not be able to hold the design specification. Either adding more decoupling capacitance or increasing the bandwidth of regulator could address the issue.

1.1.3 Topologies of Linear Regulators

Linear regulators could be categorized into two basic configurations: serial regulators and shunt regulators. The topology of the serial or shunt regulator depends on whether the regulator is connected in parallel or series with the load.

1.1.3.1 Serial Regulator

If the regulator is in serial with the load and is in between the input supply and output supply, this topology is a serial regulator.

Figure 1.3 illustrates the equivalent model of the serial linear regulator. The load is modeled as a variable resistor R_{load} to mimic the

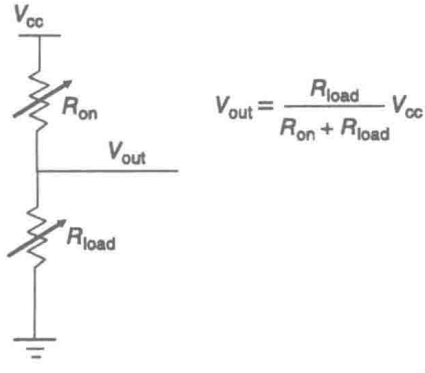

Figure 1.3 Equivalent model of serial linear regulator.

dynamic nature of the load switching. The serial regulator is modeled as a second variable resistor R_{on}, which is adjusted by the negative feedback control loop. The output voltage is given by Eq. (1.4).

$$V_{out} = \frac{R_{load}}{R_{on} + R_{load}} V_{cc} \tag{1.4}$$

Assuming the input supply V_{cc} was constant, as the load current varies, R_{load} would vary. To maintain the output voltage V_{out} unchanged, R_{on} would be changed by the regulation loop to ensure that the resistor divider ratio remains unchanged. This is the basic mechanism of how the serial regulator operates. Similarly, analysis can be applied to LNR. Assuming the output load current was constant, as the input supply V_{cc} varies, R_{on} would be changed by the regulation loop to maintain the target regulation voltage on output.

Figure 1.4 illustrates the circuit design model of the serial linear regulator. Negative feedback control is used in the design to control the regulation. Regardless of the causes of variations or changes, the variations on V_{out} are sampled and compared with a known reference. The negative feedback control loop would adjust R_{on} to bring V_{out} back on target.

1.1.3.2 Shunt Regulator

If the regulator is in parallel with the load in operation, this configuration is a shunt regulator.

Figure 1.5 illustrates the equivalent model of a shunt linear regulator. The load is modeled as a variable resistor R_{load} to mimic the dynamic nature of the load switching. The shunt regulator is modeled

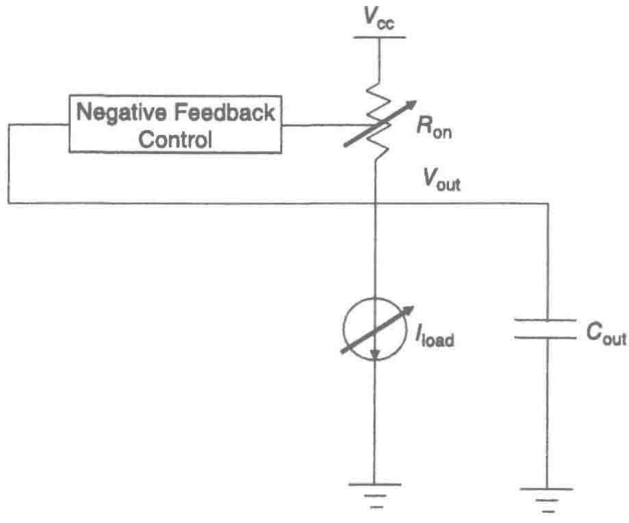

Figure 1.4 Serial linear regulator model.

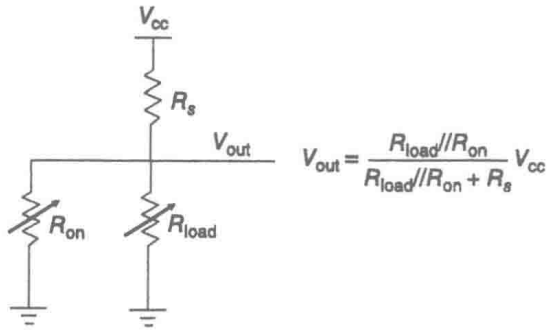

Figure 1.5 Equivalent model of shunt linear regulator.

as a second variable resistor R_{on} in parallel with R_{load} in between V_{out} and ground. And R_s is the impedance of power passing element connected between V_{cc} and V_{out}. Output voltage V_{out} could be derived from Eq. (1.5).

$$V_{out} = \frac{R_{load}//R_{on}}{R_{load}//R_{on} + R_s} V_{cc} \tag{1.5}$$

Assuming V_{cc} was constant for LDR, if the output load current changes, R_{load} would change. With negative feedback control, R_{on} would be modified accordingly to ensure the resistor divider ratio is unchanged. Shunting unneeded supply current away from the load is the basic mechanism of how shunt regulator operates. Since shunt regulator has to divert unused supply current to ground at any given time, it makes the shunt regulator much less efficient than the serial regulator, particularly under low-load or no-load current conditions.

The analysis for LNR is similar. With fixed load current, as V_{cc} varies, R_{on} would change accordingly to maintain the regulation in control.

Figure 1.6 illustrates the circuit design model for shunt linear regulator. Negative feedback control is applied in the design to control the value of R_{on}. Regardless of the causes of variation or noise on the output voltage V_{out}, the negative feedback control would adjust R_{on} so that V_{out} will be at target regulation level.

1.1.3.3 Application of Linear Regulators

A linear regulator is an element commonly used in many designs. It is simple and easy to design without the involvement of electromagnetic parts—such as inductors or transformers. Linear regulators are preferred if target output voltage and input supply voltage are not far apart. For heavy load operation, the SMPS can operate much more efficiently in power conversion. For applications where the target