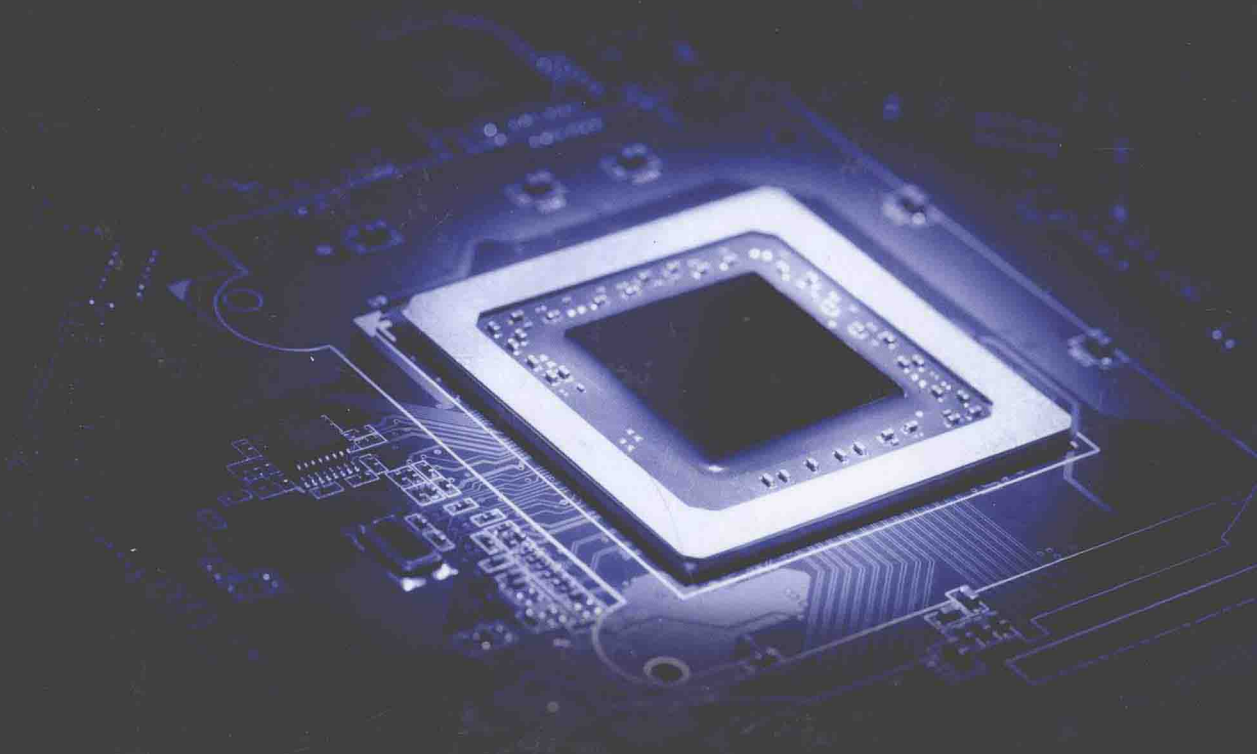
Power Management Techniques for Integrated Circuit Design



Ke-Horng Chen

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POWER MANAGEMENT TECHNIQUES FOR INTEGRATED CIRCUIT DESIGN

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To my respected parents, Li-Yun Wu and He-Nan Chen, and my wife, Hsin-Hua Pai

About the Author

Ke-Horng Chen received his B.S., M.S., and Ph.D. degrees in electrical engineering from the National Taiwan University, Taipei, Taiwan in 1994, 1996, and 2003, respectively.

From 1996 to 1998, he was a part-time IC Designer at Philips, Taipei, Taiwan. From 1998 to 2000, he was an Application Engineer at Avanti Ltd., Taiwan. From 2000 to 2003, he was a Project Manager at ACARD Ltd., where he was engaged in designing power management ICs. He is currently Director of the Institute of Electrical Control Engineering and a Professor with the Department of Electrical and Computer Engineering, National Chiao Tung University, Hsinchu, Taiwan, where he has organized a Mixed-Signal and Power Management IC Laboratory. He is the author or coauthor of more than 200 papers published in journals and conferences, and also holds several patents. His current research interests include power management ICs, mixed-signal circuit designs, and display algorithm and driver designs of liquid crystal display (LCD) TVs.

Dr. Chen has served as an Associate Editor of *IEEE Transactions on Power Electronics* and *IEEE Transactions on Circuits and Systems – Part II: Express Briefs*. He is also an Associate Editor of *IEEE Transactions on Circuits and Systems – Part I*. He joined the Editorial Board of *Analog Integrated Circuits and Signal Processing* in 2013. He is on the IEEE Circuits and Systems (CAS) VLSI Systems and Applications Technical Committee, and the IEEE CAS Power and Energy Circuits and Systems Technical Committee. He belongs to the Society for Information Display (SID) and International Display Manufacturing Conference (IDMC) Technical Program Sub-committees. He is Tutorial Co-Chair of IEEE Asia Pacific Conference on Circuits and Systems (APCCAS) 2012 and Track Chair of Integrated Power Electronics, IEEE International Conference on Power Electronics and Drive Systems (PEDS) 2013. He is Technical Program Co-Chair of IEEE International Future Energy Electronics Conference (IFEEC) 2013. He has served as CAS Taipei Section Chair since 2015. He is also Technical Program Committee Member, European Solid-State Circuits Conference (ESSCIRC) 2014–present.

Preface

Over the past three decades, power management technology has become more important as portable and wearable electronics have become part of our daily lives. It is important to realize the detailed design of power management circuits, including low dropout (LDO) regulators, switching power converters (SWRs), switched-capacitor designs among others, if battery usage lifetime and power-conversion efficiency need to be extended. Although some circuits can be found in analog or power electronics books, the reader cannot get an overall understanding of power management designs. Thus, I have written this book to collect useful material related to power management designs in recent years.

Power management IC designs use low-voltage (LV) and high-voltage (HV) devices. The specialty of this book is including LV and HV power management designs. Moreover, the objective of the book is to let the reader understand the process trend and demand of today's applications from the first. The mathematical analysis in the book is simplified, because in my opinion the reader needs to have the ability to understand the function of power management circuits. After that, the reader can analyze the whole power system and derive the complicated mathematical results. Thus, I have used many easy-to-understand figures in the book to let the reader realize why and how power management should be implemented. Although the reader can understand this via derived equations in some similar books, they can have the fun of thinking about and implementing their own designs if they study the circuits in this book by inspection rather than by equations. Moreover, digital and analog design techniques are introduced because a combination of digital and analog skills can give maximum performance of power management in system-on-chip (SoC) applications.

I have taught most of the material in this book both at the National Chiao Tung University, Hsinchu, Taiwan and in Taiwan industry. The order, the format, and the content are all carefully polished when I deliver the material to readers. It is a pity that much material is not included in this book. However, I encourage the reader to apply the concepts to similar power management designs. I have included some design guidelines in this book to let the reader realize the objective of each design.

Chapter 1 provides the reader with knowledge of LV and HV device characteristics and structure in different advanced technologies for learning the material in this book.

Chapter 2 describes the general design of an LDO regulator used in many power management circuits. Compensation skills are introduced to let the reader realize how to ensure power stability in case of any disturbance from input, output, and loading. A digital LDO regulator is also included for LV applications.

Chapter 3 includes the design guidelines of voltage-mode and current-mode switching power regulators. Compensation skills are also introduced to quantify the behavior of basic pulse-width-modulation (PWM) SWRs by inspection.

Chapter 4 introduces the ripple-based control technique for some applications that demand the features of fast transient response, low power consumption, and compact size solution. In particular, fast transient response is the trend for SWR designs to improve the performance of dynamic voltage/frequency scaling techniques and/or reference tracking techniques.

Chapter 5 shows some ripple-based control techniques to improve the performance of basic designs. Even if parasitic effects become large, the techniques presented here can still have excellent performance. Readers can train themselves by using the circuits in this book, proved for silicon, to implement useful power management circuits.

Chapter 6 shows state-of-the-art single-inductor multiple-output (SIMO) converters used in SoC to minimize the power module size. The power stage design and controller design are included in this chapter. We use the design concepts introduced in Chapters 2–5. The reader can obtain advanced training in power management designs here.

Chapter 7 shows the switching-based battery charger to complete the full function of power management in SoC designs. The basic stability proved by some behavior simulators can let the reader know how to model and increase the whole battery charger system.

Chapter 8 includes some energy-harvesting techniques to let the reader realize the possibility of obtaining energy from the environment. How to convert and how to improve efficiency are shown in this chapter.

Acknowledgments

This book has benefited from the recent research results of my Master and Ph.D. students. Many experts in both this research field and industry contributed much useful material to this book. Among them are Shen-Yu Peng (National Chiao Tung University, Hsinchu, Taiwan), Meng-Wei Chien (RealTek Corporation, Hsinchu, Taiwan), and Ying-Wei Chou (MediaTek Inc., Hsinchu, Taiwan). I say "thank you" to them.

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My wife, Hsin-Hua, has made some contributions to this book. She encouraged me to complete the whole book using a range of useful circuits proved for silicon. She collected much useful material, including simulation and experimental results.

The book's production was made possible with the cooperation of staff at John Wiley. I thank James Murphy, Preethi Belkese, Maggie Zhang, Gunalan Lakshmipathy, Revathy Kaliyamoorthy, and Clarissa Lim. Without their help, there would be no book.

Contents

1

Introduction

1.1 Moore's Law

Over the past few decades, the number of transistors per square inch on integrated circuits (ICs) has doubled every 18 months, which is the forecast of Moore's law and is a continuing condition. However, a physical limitation appears when the transistor size shrinks to 28 nm. Several technology performance boosters, for example dual stress liner (DSL) technology, strained silicon techniques, and the stress memorization technique (SMT), are required to retain the performance of transistors. The industry has failed to keep to the trend predicted by Moore's law. Figure 1.1 depicts how the rate of transistor size scaling has slowed down and is likely to break Moore's law by the end of 2015.

1.2 Technology Process Impact: Power Management IC from 0.5 micro-meter to 28 nano-meter

1.2.1 MOSFET Structure

The voltage stress issue of metal–oxide–semiconductor field-effect transistors (MOSFETs) in drivers and power MOSFETs needs careful consideration. The evolution of MOSFETs and their applications are based on different input supply voltage (Figure 1.2). In advanced processes (i.e., 40, 28, and 22 nm), core MOSFETs with characteristics of small silicon size and high speed are used in low-voltage applications. Moreover, conventional low-voltage MOSFETs are applied for low supply voltage conditions in normal processes, such as 22 nm, 0.18 μm, 0.25 μm, and 0.5 μm. Nevertheless, the drain-to-source voltage, V_{DS} of low-voltage MOSFETs cannot tolerate a high voltage and punches, and will break the MOSFET when the input supply voltage increases. Therefore, double-diffused metal–oxide–semiconductors (DMOSs), vertical

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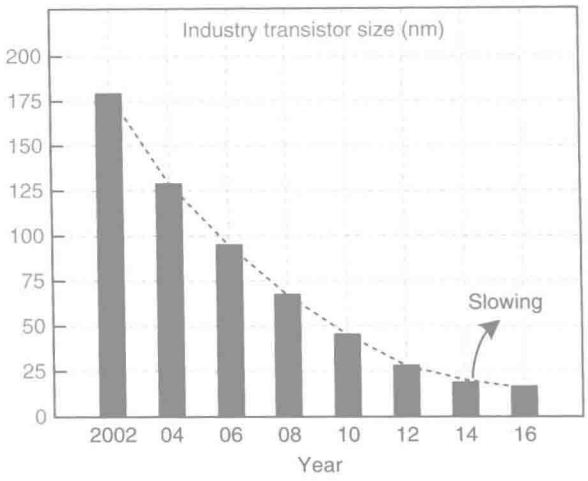

Figure 1.1 Transistor size scaling rate has slowed down

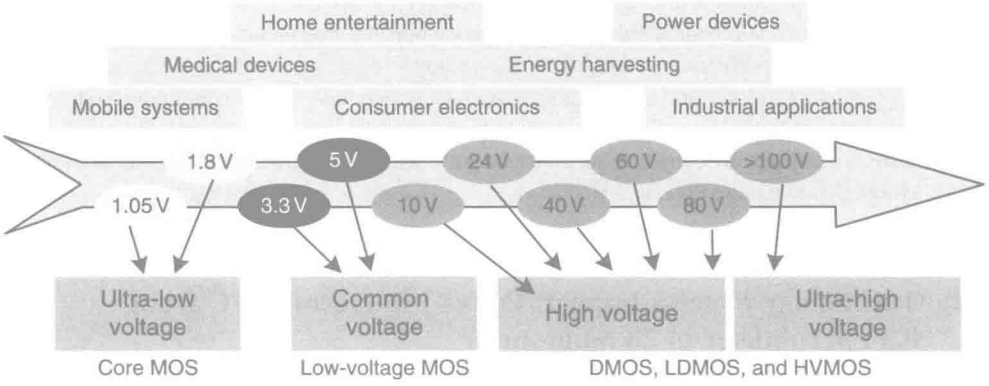

Figure 1.2 Evolution of MOSFETs and applications with different input supply voltages

double-diffused metal–oxide–semiconductors (VDMOSs), and laterally diffused metal–oxide–semiconductors (LDMOSs) are applied to bear a high V_{DS}. However, the gate-to-source voltage, V_{GS} of such MOSFETs cannot endure a high voltage, which will also damage the MOSFET. A high-voltage metal–oxide–semiconductor (HVMOS) solves the problem here, because its structure can tolerate a high voltage of both V_{DS} and V_{GS}.

The structures and characteristics of low-voltage MOSFETs, core MOSFETs, DMOSs, VDMOSs, LDMOSs, and HVMOSs are introduced in the following subsections, followed by a comparison of these MOSFETs.

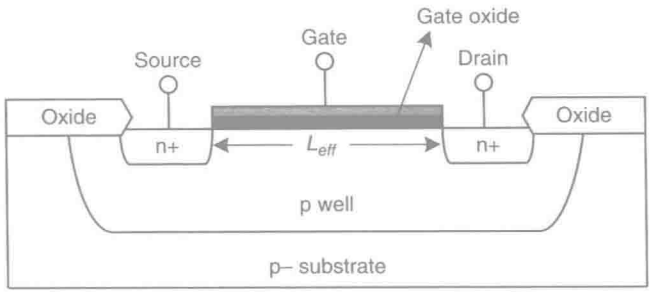

Figure 1.3 Structure of typical n-channel low-voltage MOSFET

1.2.1.1 Low-Voltage MOSFET

The structure of a typical n-channel low-voltage MOSFET is shown in Figure 1.3. Compared with LDMOSs and HVMOSs, the simple structure of a low-voltage MOSFET has the advantages of small silicon area and longest effective channel length (L_{eff}), which is defined as the contact area between the p well and the gate in the n-channel low-voltage MOSFET. Moreover, a thin-gate oxide is designed to achieve the high-speed on-and-off switching of the MOSFET. However, this thin-gate oxide cannot bear the high voltage stress of the V_{GS}. Moreover, the V_{DS} only operates in low-voltage stress conditions, because the drift region of drain is too small to tolerate a high voltage of V_{DS}.

1.2.1.2 Core MOSFET

The integrated technique of system-on-chip (Soc) has improved. A core MOSFET with small silicon size reduces the silicon area and increases the operating speed of the Soc [1, 2]. Moreover, the supply voltage evaluates to 1.8 V, 1.05 V, or lower voltages to reduce the system's power dissipation. Therefore, the voltage stress of a core MOSFET cannot bear a conventional supply voltage, such as 3.3 or 5 V, because the oxide layer of the core MOSFET is thinner than that of a low-voltage MOSFET. Conventional supply voltages damage the thinner oxide layer.

1.2.1.3 Double-Diffused MOSFET

Figure 1.4 shows a DMOS structure [3, 4]. The effective channel length is produced by p-type diffusion and gate oxide. Moreover, the n-type substrate is very lightly doped in this structure. Light doping provides enough space for expansion of the depleted region between the p-type diffusion and the n+ drain contact regions. Therefore, the breakdown voltage between drain and source is enlarged. This structure can endure a high voltage of V_{DS} but not a high voltage of V_{GS}, because of its thin gate oxide.

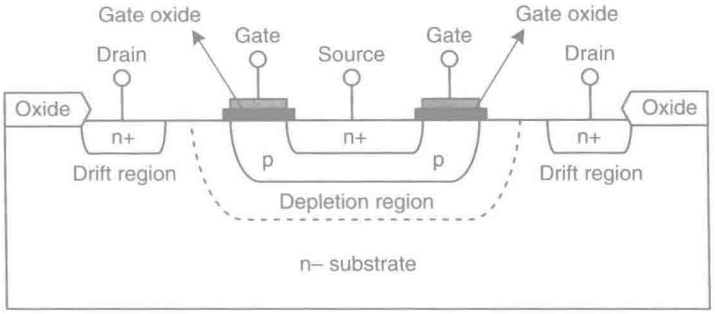

Figure 1.4 Structure of DMOS

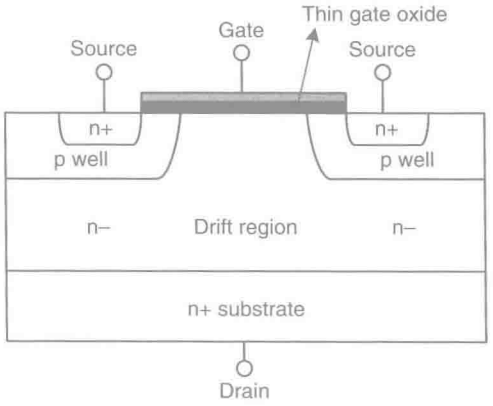

Figure 1.5 Structure of VDMOS

1.2.1.4 Vertical Double-Diffused MOSFET

The VDMOS structure combines the concepts of vertical power structures and lateral double diffusion (Figure 1.5) [5]. The drain voltage is vertically supported by the n– layer. Moreover, current flows laterally from the source through the channel, which is parallel to the silicon surface, and then turns at a right angle to flow vertically down through the n– drain layer to the n+ substrate and the drain contact. An effective channel is formed, if a sufficiently positive gate voltage is applied, and the extra drift region of the n– layer can tolerate a high voltage of V_{DS}. However, the thin gate oxide cannot bear a high voltage of V_{GS}.

1.2.1.5 Laterally Diffused MOSFET

LDMOS is also applied to solve the problem of high voltage V_{DS}. The structure of a typical n-channel LDMOS is similar to that of a low-voltage MOSFET, as shown in Figure 1.6 [6, 7]. The difference is that the LDMOS extends the drain drift region by adding an n-well